

2013 Conference on Design and Architectures for Signal and Image Processing

(DASIP 2013)

**Cagliari, Italy
8-10 October 2013**



**IEEE Catalog Number: CFP13DAS-POD
ISBN: 978-1-4799-1357-2**

Table of Contents



dasip

Welcome

General Chairs

Keynote Speakers

Program Chairs

Steering Committee

Program Committee

Conference Program

Session 1: Vision and Image Processing Architectures 1

High Performance Multi-Standard Architecture for DCT Computation in H.264/AVC High Profile and HEVC Codecs 2

Tiago Dias, Nuno Roma, and Leonel Sousa

Architecture and Programming Model Support for Efficient Heterogeneous Computing on Tightly-Coupled Shared-Memory Clusters 10

Paolo Burgio, Andrea Marongiu, Robin Danilo, Philippe Coussy, Luca Benini

A Neural Model for Hardware Plasticity in Artificial Vision Systems 18

Laurent Rodriguez, Laurent Fiack, and Benoît Miramond

A Novel Graphics Processor Architecture Based on Partial Stream Rewriting 26

Lars Middendorf and Christian Haubelt

Session 2: Tools for DSP Algorithm Implementation 34

TURNUS: a Unified Dataflow Design Space Exploration Framework for Heterogeneous Parallel Systems 35

Simone Casale-Brunet, Claudio Alberti, Marco Mattavelli, and Jorn W Janneck

System-Level PMC-driven Energy Estimation Models in RVC-CAL Video Codec Specifications 43

Rong Ren, Eduardo Juarez Martinez, Cesar Sanz Alvaro, Mickaël Raulet, Fernando Pescador Del Oso

Dataflow Program Analysis and Refactoring Techniques for Design Space Exploration: MPEG-4 AVC/H.264 Decoder Implementation Case Study 51

Ab Al-Hadi Ab Rahman, Simone Casale Brunet, Claudio Alberti, and Marco Mattavelli

Modeling Control Tokens for Composition of CAL Actors 59

Johan Ersfolk, Ghislain Roquier, Johan Lilius, and Marco Mattavelli

Table of Contents

Session 3 (SS): Visual Scene Analysis in 2D and 3D 67

A Resource-Aware Nearest Neighbor Search Algorithm for K-Dimensional Trees 68

Johny Paul, Walter Stechele, Manfred Kröhnert, and Tamim Asfour, Benjamin Oechslein, Christoph Erhardt, Jens Schedel, Daniel Lohmann, and Wolfgang Schröder-Preikschat

Accuracy and Performance Analysis of Harris Corner Computation on Tightly-Coupled Processor Arrays 76

Éricles Rodrigues Sousa, Alexandru Tanase, Frank Hannig, and Jürgen Teich

Real-Time RGB-D Data Processing on GPU Architecture 84

Massimo Camplani, Antonio Blasco, Daniel Berjón, Luis Salgado, and Francisco Morán

Real-Time Covariance Tracking Algorithm for Embedded Systems 92

Andrés Romero Mier Y Teran, Lionel Lacassagne, Ali Hassan Zahraee, and Michèle Gouiffès

Session 4 (SS): Modern Localisation Techniques 100

A Linear State Model for PDR+WLAN Positioning 101

Matti Raitoharju, Henri Nurminen, and Robert Piché

Constrained Non-linear Fitting for Stochastic Modeling of Inertial Sensors 107

Alex Garcia Quinchia, Gianluca, Fabio DAVIS, and Carles Ferrer

Effects of Colored Noise in Linear Adaptive Filters Applied to GNSS Multipath Detection 114

Sabrina Ugazio and Letizia Lo Presti

Session 5: Image Processing Applications and Systems 122

SiPM Based Smart Pixel for Photon Counting Integrated Streak Camera 123

Imane Malass, Wilfried Uhring, Jean-Pierre Le Normand, Norbert Dumas, Virginie Zint, and Foudil Dadouche

A Coarse-Grained Reconfigurable Wavelet Denoiser exploiting the Multi-Dataflow Composer tool 129

Nicola Carta, Carlo Sau, Francesca Palumbo, Danilo Pani, and Luigi Raffo

A Runtime Adaptive H.264 Video-Decoding MPSoC Platform 137

Giuseppe Tuveri, Simone Secchi, Paolo Meloni, Emanuele Cannella, and Luigi Raffo

Foreground Object Features Extraction with GLCM Texture Descriptor in FPGA 145

Mateusz Komorkiewicz and Marek Gorgoń

Table of Contents

Session 6: Smart and Adaptive Devices **153**

A Hierarchical Ant-Colony Heuristic for Architecture Synthesis for On-Chip Communication **154**
Wei Tang and Forrest Brewer

Smart Sensor Architectures for Embedded Biosignal Analysis **162**
Benjamin Pfundt, Marc Reichenbach, Björn Eskofier, and Dietmar Fey

Noise-agnostic Adaptive Image Filtering without Training References on an Evolvable Hardware Platform **170**
Javier Mora, Ángel Gallego, Andrés Otero, Eduardo de La Torre, and Teresa Riesgo

FPGA Accelerator of Quasi Cyclic EG-LDPC Codes Decoder for NAND Flash Memories **178**
Syed Azhar Ali Zaidi, Muhammad Awais, Carlo Condo, Maurizio Martina, and Guido Masera

Session 7 (SS): Advanced Image Processing for Space Applications **184**

Airport Markings Recognition for Automatic Taxiing **185**
Federico Francesco and Walter Allasia (EURIXGroup)

Stereo Vision System for Capture and Removal of Space Debris **189**
Francesco Rosso, Francesco Gallo, and Walter Allasia, Enrico Licata, Paolo Prinetto, Daniele Rolfo, and Pascal Trotta, Alain Favetto, Marco Paleari, and Paolo Ariano

Session 8: 3D Vision Systems and Applications **196**

Real-Time GPU-based Local Stereo Matching Method **197**
Jinglin Zhang, Jean-Francois Nezan, and Jean-Gabriel Cousin

New 3D-Integrated Burst Image Sensor Architectures with in-situ A/D conversion **203**
Rémi Bonnard, Fabrice Guellec, Josep Segura Puchades, Antoine Dupret, and Wilfried Uhring

Extension and FPGA Architecture of the Generalized Hough Transform for Real-Time Stereo Correspondence **211**
Frank Schumacher and Thomas Greiner

Session 9 (SS): Software Defined Radio **218**

An Efficient GPU Implementation of an Arbitrary Resampling Polyphase Channelizer **219**
Scott Kim, William Plishker, Shuvra Bhattacharyya

Low-Cost Guaranteed-Throughput Communication Ring for Real-Time Streaming MPSoCs **227**
Berend Dekens, Marco Bekooij, Philip Wilmanns, and Gerard Smit

Design of a Matched Filter for Timing Synchronization **235**
Roberto Airoldi and Jari Nurmi

Table of Contents

Poster Session 240

- A 3D Reconstruction from Real-time Stereoscopic Images using GPU* 241
Jose Gomez-Balderas and Dominique Houzet
- Accelerating a Modified Gaussian Pyramid with a Customized Processor* 247
Diana Gil, Pierre Langlois, and Yvon Savaria
- Communication Cost Reduction for Hardware Tasks Placed on Homogeneous Reconfigurable Resource* 253
Quang-Hai Khuat and Daniel Chillet
- Design and Analysis of an FPGA based Encoder SoC for Locally Stationary Image Source* 259
Yuhui Bai, Syed Zahid, and Bertrand Granado
- Efficient Bit Decoding Implementation for Mass Market Multi-Constellation GNSS Receivers* 267
Tommi Paakki, Jussi Raasakka, Francescantonio Della Rosa, and Jari Nurmi
- Embedded Vision-based SLAM: A Model-driven Approach* 272
Jonathan Piat, David Marquez, and Michel Devy
- Evaluation of an RTOS on top of a Hosted Virtual Machine System* 278
Mehdi Aichouch, Jean-Christophe Prévotet, and Fabienne Nouvel
- Exploring Frequency Tuning Policies for USRP-N210 SDR Platform and GNU Radio* 286
Islam Galal and Mostafa Ibrahim
- Memory Access Analysis and Optimization of a Parallel H.264/SVC Decoder for an Embedded Multi-Core Platform* 292
Jens Brandenburg and Benno Stabernack
- A Novel Inter-Layer Intra Prediction Architecture for Real-Time SVC Video Codecs* 300
Yeray Hernandez, Sebastian Lopez, Gustavo Callico, Jose Lopez, and Roberto Sarmiento
- Particle Filters and Resampling Techniques: Importance in Computational Complexity Analysis* 307
Biruk Getachew Sileshi, Carles Ferrer, and Joan Oliver
- Task Migration of DSP Application Specified with a DFG and Implemented with the BSP Computing Model on a CPU-GPU Cluster* 314
Farouk Mansouri, Sylvain Huet, Vincent Fristo, and Dominique Houzet
- Tetrahedral Volume Reconstruction in X-Ray Tomography using GPU Architecture* 322
Michele A. Quinto, Dominique Houzet, and Fanny Buyens

Table of Contents

Demo Night 328

- Design Space Exploration and Implementation of RVC-CAL Applications using the TURNUS framework* **329**
Simone Casale Brunet, Endri Bezati, Claudio Alberti, Ghislain Roquier, Marco Mattavelli, Jorn W Janneck and Jani Boutellier
- Dynamic Source Code Analysis for Memory Hierarchy Optimization in Multimedia Applications* **331**
Christakis Lezos, Grigoris Dimitroulakos, Angeliki Freskou, and Konstantinos Masselos
- Evaluation of Driver Assistance Systems with a Car Simulator using a Virtual and a Real FPGA Platform* **333**
Philipp Wehner and Diana Goehringer
- Framework for Fast Prototyping of Applications Running on Reconfigurable System on Chip* **335**
Jan Viktorin, Pavol Korcek, Vlastimil Kosar and Jan Korenek
- Networked Embedded Acoustic Processing System for Smart Building Applications* **337**
Sebastian Uziel, Thomas Elste, Wolfram Kattaneck, Danilo Hollosi, Stephan Gerlach, and Stefan Goetze
- A Noise-Agnostic Self-Adaptive Image Processing Application Based on Evolvable Hardware* **339**
Javier Mora, Ángel Gallego, Andrés Otero, Eduardo de La Torre and Teresa Riesgo
- A Prototype of an Adaptive Computer Vision Algorithm on MPSoC Architecture* **341**
Éricles Rodrigues Sousa, Alexandru Tanase, Frank Hannig, and Jürgen Teich
- Prototype of a novel Steady-State Load Identification Technique for Digitally Controlled DC-DC Power Supplies* **343**
Andrea Congiu, Massimo Barbaro, Andrea Picciau, Emanuele Bodano, and Dirk Hammerschmidt
- Spatial Edge Directed Video Deinterlacing* **345**
Prateek Murgai and Maria Trocan