

2013 IEEE High Performance Extreme Computing Conference

(HPEC 2013)

**Waltham, Massachusetts, USA
10 – 12 September 2013**



IEEE Catalog Number: CFP13HPE-POD
ISBN: 978-1-4799-1363-3

TABLE OF CONTENTS

An Improved Eigensolver for Quantum-dot Cellular Automata Simulations	1
<i>A. Baldwin, J. Will, D. Tougaw</i>	
Exploiting Free Silicon for Energy-Efficient Computing Directly in NAND Flash-based Solid-State Storage Systems	7
<i>P. Li, K. Gomez, D. Lilja</i>	
D4M 2.0 Schema: A General Purpose High Performance Schema for the Accumulo Database	13
<i>J. Kepner, C. Anderson, W. Arcand, D. Bestor, B. Bergeron, C. Byun, M. Hubbell, P. Michaleas, J. Mullen, D. O'Gwynn, A. Prout, A. Reuther, A. Rosa, C. Yee</i>	
PAKCK: Performance and Power Analysis of Key Computational Kernels on CPUs and GPUs	19
<i>J. Mullen, M. Wolf, A. Klein</i>	
A Novel Fast Modular Multiplier Architecture for 8,192-bit RSA Cryposystem	25
<i>W. Wang, X. Huang</i>	
Block Processor: A Resource-distributed Architecture	30
<i>Z. Wang, F. Yu, X. Liu</i>	
A Mechanism To Improve The Performance Of Hybrid MPI-OpenMP Applications In Grid	36
<i>S. Mehrotra, K. Shamjith, P. Pandey, A. Sridharan</i>	
GPU Accelerated Elevation Map based Registration of Aerial Images	44
<i>J. French, W. Turri, J. Fernando, E. Balster</i>	
GPU Accelerated Blood Flow Computation using the Lattice Boltzmann Method	50
<i>C. Nita, L. Itu, C. Suci, C. Suci</i>	
Software-Defined IDS for Securing Embedded Mobile Devices	56
<i>R. Skowyra, S. Bahargam, A. Bestavros</i>	
Instruction Set Extensions for Photonic Synchronous Coalesced Accesses	63
<i>P. Keltcher, D. Whelihan, J. Hughes</i>	
SIMD Acceleration of Modular Arithmetic on Contemporary Embedded Platforms	67
<i>K. Pabbuleti, D. Mane, A. Desai, C. Albert, P. Schaumont</i>	
Adaptive Routing in Hexagonal Torus Interconnection Networks	73
<i>A. Shamaei, B. Bose, M. Flahive</i>	
LLSuperCloud: Sharing HPC Systems for Diverse Rapid Prototyping	79
<i>A. Reuther, J. Kepner, W. Arcand, D. Bestor, B. Bergeron, C. Byun, M. Hubbell, P. Michaleas, J. Mullen, A. Prout, A. Rosa</i>	
Understanding Query Performance in Accumulo	85
<i>S. Sawyer, B. O'Gwynn, A. Tran, T. Yu</i>	
FPGA-based Hyperspectral Covariance Coprocessor for Size, Weight, and Power Constrained Platforms	91
<i>D. Kusinsky, M. Leeser</i>	
Biquad Implementation of an IIR Filter for IQ Mismatch Correction in an SoC RF Receiver	97
<i>K. Gettings, A. Bolstad, M. Ericson, X. Wang</i>	
A Nested Dissection Partitioning Method for Parallel Sparse Matrix-Vector Multiplication	102
<i>E. Boman, M. Wolf</i>	
Task Scheduling for Reconfigurable Systems in Dynamic Fault-Rate Environments	108
<i>A. Jacobs, N. Wulf, A. George</i>	
Vendor Agnostic, High Performance, Double Precision Floating Point Division for FPGAs	114
<i>X. Fang, M. Leeser</i>	
Accelerating Sparse Matrix-Matrix Multiplication with 3D-Stacked Logic-in-Memory Hardware	119
<i>Q. Zhu, T. Graf, H. Sumbul, L. Pileggi, F. Franchetti</i>	
Miniature Radar for Mobile Devices	125
<i>P. Sharma, R. Ouedraogo, B. Perry, D. Aubin, T. Levy, D. Souza, J. Kitchens, J. Peabody</i>	
Standards for Graph Algorithm Primitives	133
<i>T. Mattson, D. Bader, J. Berry, A. Buluc, J. Dongarra, C. Faloutsos, J. Feo, J. Gilbert, J. Gonzalez, B. Hendrickson, J. Kepner, C. Leiserson, A. Lumsdaine, D. Padua, S. Poole, S. Reinhardt, M. Stonebraker, S. Wallach, A. Yoo</i>	
Integrity Verification for Path Oblivious-RAM	135
<i>L. Ren, C. Fletcher, X. Yu, M. Dijk, S. Devadas</i>	
Robust Graph Traversal: Resiliency Techniques for Data Intensive Supercomputing	141
<i>S. Hukerikar, P. Diniz, R. Lucas</i>	

GPU-Based Space-Time Adaptive Processing (STAP) for Radar	147
<i>T. Benson, R. Hersey, E. Culpepper</i>	
A Clustered Manycore Processor Architecture for Embedded and Accelerated Applications.....	153
<i>B. Dinechin, R. Ayrignac, P. Beaucamps, P. Couvert, B. Ganne, P. Massas, F. Jacquet, S. Jones, N. Chaisemartin, F. Riss, T. Strudel</i>	
High Throughput Energy Efficient Parallel FFT Architecture on FPGAs.....	159
<i>R. Chen, N. Park, V. Prasanna</i>	
3D FFT for FPGAs	165
<i>B. Humphries, M. Herbordt</i>	
Evaluating Energy Efficiency of Floating Point Matrix Multiplication on FPGAs.....	167
<i>K. Matam, H. Le, V. Prasanna</i>	
Dynamically Configurable Online Statistical Flow Feature Extractor on FPGA	173
<i>D. Tong, V. Prasanna</i>	
Novel Algebras for Advanced Analytics in Julia.....	179
<i>V. Shah, A. Edelman, S. Karpinski, J. Bezanson, J. Kepner</i>	
CrowdCL: Web-Based Volunteer Computing with WebCL	183
<i>T. MacWilliam, C. Cecka</i>	
Big Snapshot Stitching with Scarce Overlap	189
<i>A. Iliopoulos, J. Hu, N. Pitsianis, X. Sun, M. Gehm, D. Brady</i>	
Real-Time Traffic Sign Detection Using SURF Features on FPGA	195
<i>J. Zhao, S. Zhu, X. Huang</i>	
Accelerating a Novel Particle-based Fluid Simulation on the GPU.....	201
<i>Z. Chen, J. Kingsley, X. Huang, E. Tuzel</i>	
Re-Introduction of Communication-Avoiding FMM-Accelerated FFTs with GPU Acceleration	207
<i>M. Langston, M. Baskaran, B. Meister, N. Vasilache, R. Lethin</i>	
Author Index	