

2013 IEEE 22nd Conference on Electrical Performance of Electronic Packaging and Systems

(EPEPS 2013)

**San Jose, California, USA
27-30 October 2013**



**IEEE Catalog Number: CFP13EPP-POD
ISBN: 978-1-4799-0708-3**

TABLE OF CONTENTS

Millimeter Wave and RF Technologies I

Electrical Characterization of Low-Cost glass epoxy laminates at Millimeter Wave Frequencies	7
A Method for Modeling the Impact of Conductor Surface Roughness on Waveguiding Properties of Interconnects	11
A Perturbation Technique to Analyze the Influence of Fiber Weave Effects on Differential Signaling	15

Millimeter Wave and RF Technologies II

Insertion Loss Characterization of Tightly Spaced Interconnects with an Embedded Patterned Layer	21
Modeling I/O Buffers Using X-Parameters	25
Design and Fabrication of Geometrically Complicated Multiband Microwave Devices Using A Novel Integrated 3D Printing Technique	29

EM K.....

Parallel Processing Improvements for Full-Wave Electromagnetic Solvers	35
A Generalized Modeling Method for Signal/Power Integrity Analysis of 3D Coupled Interconnects In Finite Cavity Based on 1D Technology	39
New Simulation Procedure for Accurate Package Modeling Considering Chip-Package Interaction	43
Optimum Implementation of a Locally Implicit Leapfrog Scheme for Fast Simulation of Inhomogeneously-Meshed Plane Structures	47
Memory Efficient Laguerre-FDTD Scheme for Dispersive Media	51

EM KK.....

O qf grpi 'O gj qf qmqi kgu'hqt'O wnk'NgxgrRED/'Rcenci g'Eg/Uko wrcvqp'('Eq/F guki p.....	79
--	----

EM KKK.....

Ceegrctcv'J ki j 'Ur ggf 'KQ'F guki p'Enquwtg'y kj 'F kwtldwgf 'Ej kr 'KQ'Kpvgteqppge'v'O qf gn.....	83
--	----

3-D Packaging.....

Applying a Physics-Based Via Model for the Simulation of Through Silicon Vias	65
Timing Analysis for Thermally Robust Clock Distribution Network Design for 3D ICs	69
Mitigation of TSV-Substrate Noise Coupling in 3-D CMOS SOI Technology	73

Power Integrity and Wireless Power Transfer

Power Integrity Analysis for Core Logic Blocks	79
Power Integrity of a 4.8Gbps-per-link Low-swing Single-ended-I/O Server Memory Interface	83

Power Distribution Network Design Optimization with On-Die Voltage-Dependent Leakage Path	87
Design, Implementaion and Measurement of Board-to-Board Wireless Power Transfer (WPT) for Low Voltage Applications.....	91

Advanced CAD Techniques

SPICE-Based Statistical Assessment of Interconnects Terminated by Nonlinear Loads with Polynomial Characteristics	99
Cost Effective Modeling Methodologies and Evaluating Electrical Interaction in FCBGA Packages	103
Electrical-Thermal Co-Simulation for DC IR-Drop Analysis of Large-Scale Integrated Circuits.....	107
Reliable Detection of Causality Violations in Tabulated Scattering Parameters through Filtered Dispersion Relations.....	111
A Parallel, Adaptive, Multi-Point Model Order Reduction Algorithm	115
Multiple and Non-Existent Barnes-Hut Center-of-Charge (CoC) Solution in Lossy Layered Substrates: Half Space Analytic and Numerical Study	119

Macromodeling.....

An iterative reweighting process for macromodel extraction of power distribution networks.....	125
Noise compliant macromodel synthesis for RF and Mixed-Signal applications.....	129
Connecting vector fitting to barycentric interpolation and the Loewner matrix	133
A Novel Algorithm for Optimum Order Estimation of Nonlinear Reduced Macromodels	137
Fixed-Order Parametric Macromodeling of Interconnects from S-parameter Data using Loewner Matrix based Method	141

High Speed Links I.....

On-die Supply-induced Jitter Behavioral Modeling	147
Mitigating the Impact of Sinusoidal Jitter and Duty Cycle Distortion on Random Jitter estimation by Tailfit Algorithm	151
A Novel Flexible On-Die Decoupling Scheme Using Package Interconnects	155
Robust PoP Probing Solutions for High-Performance Application Processor Developments....	159

High Speed Links II

High-speed DIMM-in-a-Package (DIAP) Memory Module	165
Peak Distortion Analysis of Nonlinear Links	169
A Low-Frequency Enhanced S-Parameter Handling Scheme for Time Domain Simulation of High Speed Interconnects	173

Poster Session

A package-level implementation of traveling-wave switch using PIN-diodes.....	179
Implementation of a RF Front-end Module by Embedding ICs in Molding Package.....	183
Accurate Characterization of Lossy Interconnects from TDR Waveforms.....	187
Per-Unit-Length Parameter Extraction for Lossy Multi-conductor Power Cables.....	191
Differential Through-Silicon-Vias Modeling and Design Optimization to Benefit 3D IC Performance	195
On-line Real-time Temperature and Power Estimation of an IC Using Time-domain Thermal Filters.....	199
Modeling Broadband Equivalent Circuit of Interconnects with Full Wave Electromagnetic Solver.....	203
Efficient performance evaluation of high-speed differential interconnect lines with via discontinuities	207
In-Depth Analysis of Power Noise Coupling Between	211
Analysis and Verification of Board Power Delivery Network Impact on DDR3L Memory Interface in ARM SoC Application	215
Minimal-Order Circuit Model Based Fast Electromagnetic Simulation	219
Characterization and Analysis of Vertical Coupling Impact on Receiver Performance in High Speed Serial Interface	223
Some Internal Crosstalk Reduction Schemes	227
Crosstalk Mitigation in Dense Microstrip Wiring Using Stubby Lines	231
Simulation of the TSV-to-Device Coupling in 3D ICs for Short-Channel Strained Silicon Transistors	235
Efficient Adaptive Mesh Refinement for MoM-based Package-Board 3D Full-wave Extraction.....	239
A Novel EBG Structure with Super-Wideband Suppression of Simultaneous Switching Noise in High Speed Circuits.....	243
Application of Qualitative Imaging Methods to Electrical Performance-Aware Package Board Design	247
Characterization of TSVs by Cascaded Daisy Chains.....	251
Design and Verification of SMT MMIC Package using a 20 GHz LNA, a 40 GHz LNA and a 40GHz Digital Attenuator	255
A Novel Common-Mode Filter for Multiple Differential Pairs with Low Crosstalk and Low Mode Conversion Level	259
Tests for Time Domain EM Solvers for Stability and Towards Passivity.....	263