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(ReConFig 2013)

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2013 International Conference on ReConFigurable Computing and FPGAs (ReConFig)

Papers by Sessions

General Sessions

"FPGA?: An Open Source Framework for FPGA-GPU PCIe Communication"
Yann Thoma, Alberto Dassatti, Daniel Molla ^{WWW} ^{FA}

"Improving Calibration Precision of Signal-Delay-Based Time Measurement Systems in FPGAs"
Ralf Joost, Matthias Hinkfoth, Ralf Salomon ^{WWW} ^{WWW}

"Leakage Power Reduction in FPGA DSP Circuits Through Algorithmic Noise Tolerance"
Edgar Mora-Sanchez, Jason H. Anderson ^{WWW} ^{FH}

"Processor Arrays Generation for Matrix Algorithms Used in Embedded Platforms"
Roberto Perez-Andrade, Cesar Torres-Huitzil, Rene Cumplido, Juan M. Campos ^{WWW} ^{FJ}

"A Framework for PC Applications with Portable and Scalable FPGA Accelerators"
Markus Weinhardt, Alexander Krieger, Thomas Kinder ^{WWW} ^{KG}

"Optimal Mapping of Multiple Packet Lookup Schemes onto FPGA"
Swapnil Haria, Viktor Prasanna ^{WWW} ^F

"SoC Self-Integration Mechanism for Dynamic Reconfigurable Systems based on Collaborative Macro-Function Units"
Victor Dumitriu, Lev Kirischian ^{WWW} ^U

"A robust and low resource FPGA-based stereoscopic vision algorithm"
Ibarra-Delgado, S., Hernandez Calviño, M., Guil Mata, N., Gómez-Luna, J. ^{WWW} ^Î

"Energy-Efficient Architecture for Stride Permutation on Streaming Data"
Ren Chen, Viktor K. Prasanna ^{WWW} ^G

"Improving FPGA Placement with a Self-Organizing Map"
Timm Bostelmann, Sergei Sawitzki ^{WWW} ^J

"A Flexible Implementation of the PSO Algorithm for Fine- and Coarse-Grained Reconfigurable Embedded Systems"
Michael Rueckauer, Daniel M. Muñoz, Timo Stripf, Oliver Oey, Carlos H. Llanos, Juergen Becker ^{WWW} ^Í

"A Scalable Evolvable Hardware Processing Array"
Ángel Gallego, Javier Mora, Andrés Otero, Eduardo de la Torre, Teresa Riesgo ^{WWW} ^F

“Automated Design Flow for No-Cost Configuration Error Detection in SRAM-based FPGAs”

M. Ben Jrad, R. Leveugle ¹

“FPGA Prototyping of Large Reconfigurable ADPLL Network for Distributed Clock Generation”

Chuan Shan, Eldar Zianbetov, Weiqiang Yu, Francçois Anceau, Olivier Billoint, Dimitri Galayko ¹

“Max-Hashing Fragments for Large Data Sets Detection”

Jean Pierre David ¹

“Energy-Efficient Large-Scale Matrix Multiplication on FPGAs”

Kiran Kumar Matam, Viktor K. Prasanna ¹

“Alternative Implementations of a Fractional Order Control Algorithm on FPGAs”

Cristina I. Muresan, George Mois, Silviu Folea, Clara Ionescu ¹

“Dynamic Simulation of Direct Torque Control of Induction Motors with FPGA Based Accelerators”

Hamed S. Kia, Mohammad A. Zare, Rejesh G. Kavasseri, Cristinel Ababei ¹

“A Hierarchical Parallel Evolvable Hardware Based on Network on Chip”

JunRong Wang, Dan Wang, JinMei Lai ¹

“Very low resource table-based FPGA evaluation of elementary functions”

Horácio C. Neto, Mário P. Véstias ¹

“Energy-Efficient Median Filter on FPGA”

Andrea Sanny, Viktor K. Prasanna ¹

“Performance Modeling of Reconfigurable Distributed Systems based on the OpenSPARC FPGA Board and the SIRC Communication Framework”

Kevin L. Thomas, Michael S. Thompson ¹

“Numerically Efficient and Biophysically Accurate Neuroprocessing Platform”

Juan Carlos Moctezuma, Joseph P. McGeehan, Jose Luis Nunez-Yanez ¹

“A VLSI Architecture for the QR Decomposition based on the MCGR Algorithm”

Pedro Cervantes-Lozano, Luis F. González-Pérez, Andrés D. García-García ¹

“Design of Asynchronous Systems on FPGA using Direct Mapping and Synchronous Specification”

Duarte L. Oliveira, Diego Bompean, Lester A. Faria, João Luis V. Oliveira ¹

“An Effective Window Based Legalization Algorithm for FPGA Placement”

Yu Wang, Hyunchul Shin ¹

“Dynamic and partial reconfiguration of Zynq 7000 under Linux”

Muhammed Al Kadi, Patrick Rudolph, Diana Göhringer, Michael Hübner ¹

High Performance Reconfigurable Computing

“BSW: FPGA-Accelerated BLAST-Wrapped Smith-Waterman Aligner”
Bryant C. Lam, Carlo Pascoe, Scott Schaecher, Herman Lam, Alan D. George ^{AWM}€

“Online Heavy Hitter Detector on FPGA”
Da Tong, Viktor Prasanna ^{AWM}İ

“Range Tree-Linked List Hierarchical Search Structure for Packet Classification on FPGAs”
Oguzhan Erdem, Aydin Carus ^{AWM}İ H

“Performance modeling and optimization of 3-D stencil computation on a stream-based FPGA accelerator”
Keisuke Dohi, Kota Fukumoto, Yuichiro Shibata, Kiyoshi Oguri ^{AWM}İ J

“Tree-less Huffman Coding Algorithm for Embedded Systems”
Marco Antonio Soto Hernández, Oscar Alvarado-Nava, Eduardo Rodríguez-Martínez, Francisco J. Zaragoza Martínez ^{AWM}J

“A High Performance Architecture for Computing Burrows-Wheeler Transform on FPGAs”
Umer I. Cheema, Ashfaq A. Khokhar ^{AWM}GF

“FPGA-Based Reconfigurable Unit for Image Filtering in Frequency Domain”
Luis M. Ledesma-Carrillo, Misael Lopez-Ramirez, Ana L. Martinez-Herrera, Eduardo Cabal-Yepez, Arturo Garcia-Perez ^{AWM}GE

“An Efficient Application-Specific Instruction-Set Processor for Packet Classification”
Omar Ahmed, Shawki Areibi ^{AWM}GFH

“A Reconfigurable Architecture for Searching Optimal Software Code to Implement Block Cipher Permutation Matrices”
Elif Bilge Kavun, Gregor Leander, Tolga Yalçın ^{AWM}GFJ

“Power Efficiency Benchmarking of a Partially Reconfigurable, Many-Tile System Implemented on a Xilinx Virtex-6 FPGA”
Raymond J. Weber, Justin A. Hogan, Brock J. LaMeres ^{AWM}GD

Multiprocessor Systems and Networks on Chip

“The Hamiltonian-based Odd-Even Turn Model for Adaptive Routing in Interconnection Networks”
Poona Bahrebar, Dirk Stroobandt ^{AWM}GF

“Rerouting: Scalable NoC self-optimization by distributed hardware-based connection reallocation”
Jan Heisswolf, Maximilian Singh, Martin Kupper, Ralf König and Jürgen Becker ^{AWM}GH

“ReCompAc: Reconfigurable Compute Accelerator”
Milovan Duric, Oscar Palomar, Aaron Smith ^{WWW} I

“Distributed Execution of Transmural Electrophysiological Imaging with CPU, GPU, and FPGA”
Sam Skalicky, Sonia López, Marcin Lukowiak ^{WWW} J

“Video Super Resolution Algorithm Implemented on a Low-cost NoC-based MPSoC Platform”
Garbí Singla, Félix Tobajas, Valentín de Armas ^{WWW} I

“PolyNOC - A Polymorphic thread simulator for NOC communication based embedded systems”
Swamy D. Ponpandi, Zhang Zhang, Akhilesh Tyagi ^{WWW} G

Reconfigurable Computing for Security and Cryptography

“PASC: Physically Authenticated Stable-Clocked SoC Platform on Low-Cost FPGAs”
Aydin Aysu, Patrick Schaumont ^{WWW} E

“A Hardware Pipelined Architecture of a Scalable Montgomery Modular Multiplier over $GF(2^m)$ ”
Guillaume Reymond, Victor Murillo ^{WWW} I

“New Universal Element with Integrated PUF and TRNG Capability”
Michal Varchola, Milos Drutarovsky, Viktor Fischer ^{WWW} G

“A Delay-based PUF Design Using Multiplexer Chains”
Miaoqing Huang, Shiming Li ^{WWW} I

“Countermeasures against EM Analysis for a Secured FPGA-based AES Implementation”
P. Maistri, S. Tiran, P. Maurine, I. Koren, R. Leveugle ^{WWW} J

“A Fault Attack on a Hardware-based Implementation of the Secure Hash Algorithm SHA-512”
Abdulhadi Shoufan ^{WWW} E

“Design of Low Area-overhead Ring Oscillator PUF with Large Challenge Space”
Durga Prasad Sahoo, Debdeep Mukhopadhyay, Rajat Subhra Chakraborty ^{WWW} E

Productivity Environments and High Level Languages

“Programming FPGA Based NoCs with Java”
Gary Plumbridge, Neil C. Audsley ^{WWW} FH

“Loopy - An Open-Source TCP/IP Rapid Prototyping and Validation Framework”
Christian de Schryver, Philipp Schäfer, Norbert Wehn, Thomas Fischer, Arnd Poetzsch-Heffter ^{WWW} FJ

“Enhancing Productivity with Back-End Similarity Matching of Digital Circuits for IP Reuse”

Kevin Zeng, Peter Athanas  

“modHDL: A modular and expandable language for developing synchronous hardware”

Fabian May, Friedrich Mayer-Lindenberg  

“High Level Synthesis: Where Are We? A Case Study on Matrix Multiplication”

Sam Skalicky, Christopher Wood, Marcin Lukowiak, Matthew Ryan  

“Exploiting Architecture Description Language for Diverse IP Synthesis in Heterogeneous MPSoC”

Zoltán Endre Rákossy, Axel Acosta Aponte, Anupam Chattopadhyay  

“Optimization Techniques for a High Level Synthesis Implementation of the Sobel Filter”



Josh Monson, Mike Wirthlin, Brad L Hutchings   €

Reconfigurable Computing for DSP and Communications



“A Low Complexity H.264/AVC 4x4 Intra Prediction Architecture with Macroblock/Block Reordering”

Milica Orlandić, Kjetil Svarstad   Î

“Real-Time Range Image Preprocessing on FPGAs”

Moritz Schmid, Markus Blocherer, Frank Hannig, Jürgen Teich   G



“Extracting Memory-Level Parallelism through Reconfigurable Hardware Traces”

Mingjie Lin, Shaoyi Cheng, John Wawrzynek   €


“Parallel and Configurable Turbo Decoder Implementation for 3GPP-LTE”

Luis F. Gonzalez-Perez, Lennin C. Yllescas-Calderon, R. Parra-Michel   ì

“Fast Fixed-Point Divider based on Newton-Raphson Method and piecewise polynomial approximation”



Rodríguez-García, L. Pizano-Escalante, R. Parra-Michel, O. Longoria-Gandara, J. Cortez   I

“NoC-Based Hardware Function Libraries for Running Multiple DSP Algorithms”

B. I. Gea-Garcia, J. L. Vazquez-Avila, R. Sandoval-Arechiga, J. L. Pizano-Escalante, R. Parra-Michel, Mario-Siller   U €

Reconfiguration Techniques

“A Single-chip Solution for the Secure Remote Configuration of FPGAs using Bitstream Compression”

Jo Vliegen, Nele Mentens, Ingrid Verbauwhede   U Î

“Towards the Generic Reconfigurable Accelerator: Algorithm Development, Core Design, and Performance Analysis”

Byron Navas, Johnny Öberg, Ingo Sander ^{XXXX} €G

“A Platform for Secure IP Integration in Xilinx Virtex FPGAs”

Ali Ebrahim, Khaled Benkrid, Jalal Khalifat, Chuan Hong ^{XXXX} €I

Techniques and Tools for Resilient Computing

“Dynamic Reliability Management: Reconfiguring Reliability-Levels of Hardware Designs at Runtime”

Jahanzeb Anwer, Sebastian Meisner, Marco Platzner ^{XXXX} FI

“Improving Memory Performance in Reconfigurable Computing Architecture through Hardware-Assisted Dynamic Graph”

Bai Yu, Mohammed Alawad, Michael Riera, Mingjie Lin ^{XXXX} €E

Interconnect architectures for reconfigurable computing systems

“RALP:Reconvergence-Aware Layer Partitioning For 3D FPGAs”

Qingyu Liu, Yuchun Ma, Yu Wang, Wayne Luk, Jinian Bian ^{XXXX} G

“Efficient Multilevel Interconnect Topology for Cluster-based Mesh FPGA Architecture”

Emna Amouri, Adrien Blanchardon, Roselyne Chotin-Avot, Habib Mehrez, Zied Marrakchi ^{XXXX} H

“Design and implementation of a modular, low latency, fault-aware, FPGA-based Network Interface”

Roberto Ammendola , Andrea Biagioni , Ottorino Frezza , Francesca Lo Cicero , Alessandro Lonardo, Pier Stanislao Paolucci , Davide Rossetti , Francesco Simula, Laura Tosoratto, Piero Vicini ^{XXXX} I €

“Exploration Environment for 3D Heterogeneous Tree-based FPGA Architectures (3D HT-FPGA)”

Vinod Pangracious, Habib Mehrez, Nizar Beltaief, Zied Marrakchi, Umer Farooq ^{XXXX} I Î

Coarse- Grained Reconfigurable Computing

“A Restricted Dynamically Reconfigurable Architecture for Low Power Processors”

Takeshi Hirao, Dahoo Kim, Itaru Hida, Tetsuya Asai, Masato Motomura ^{XXXX} Í G

“Timing Error Handling on CGRAs”

Thomas Schweizer, Wolfgang Rosenstiel, Luigi Vaz Ferreira, Marcus Ritt ^{XXXX} Í J

“Mixed-grained reconfigurable architecture supporting flexible reliability and C-based design”

Hiroaki Konoura , Dawood Alnajjar, Yukio Mitsuyama, Hiroyuki Ochi, Takashi Imagawa, Shinichi Noda, Kazutoshi Wakabayashi, Masanori Hashimoto, Takao Onoye ^{XXXX} Î Í

“MCMA: A modular processing elements array based low-power coarse-grained reconfigurable accelerator”

Remi Chaintreuil, Rie Uno, Hideharu Amano ~~AAAA~~ Ì F

PhD Forum

“Accuracy, Cost, and Performance Tradeoffs for Floating-Point Accumulation”

Krishna K. Nagar, Jason D. Bakos ~~AAAA~~ Ì Ì

“Improved Method for Parallel AES-GCM Cores Using FPGAs”

Karim M. Abdellatif, R. Chotin-Avot, H. Mehrez ~~AAAA~~ Ì F

“Exploring the Problems of Placement and Mapping in NoC-based Reconfigurable Systems”

Jonas Gomes Filho, Wang Jiang Chau ~~AAAA~~ Ì Í

“Lightweight and Compact Solutions for Secure Reconfiguration of FPGAs”

Karim M. Abdellatif, R. Chotin-Avot, H. Mehrez ~~AAAA~~ Ì J