2013 9th International Workshop on Electromagnetic Compatibility of Integrated Circuits

(EMC Compo 2013)

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Session Program

Date: Sunday, 15/Dec/2013

JW1: Joint Workshop 1

Time: Sunday, 15/Dec/2013: 9:00am - 10:30am · *Location:* Kinsho Hall

JW1-1: Devices, Circuits, Packages and Systems Understanding their Interplay for Managing Signal, Power and Thermal Integrity

Madhavan Swaminathan
Georgia Institute of Technology, Atlanta, USA

JW1-2: The Pathways to Cost-Effective Power/Signal Integrity Designs for High-Performance Mobile Systems

Woong Hwan Ryu
Samsung Electronics, Korea, Republic of (South Korea)

JW2: Joint Workshop 2

Time: Sunday, 15/Dec/2013: 10:50am - 12:10pm · *Location:* Kinsho Hall

JW2-1: Transition from 2D to 3D IC design: Advantage, Challenge and Solutions

William Wu Shen
TSMC Corp., Taiwan

JW2-2: Introduction of JEITA LPB WG

Yoshinori Fukuba
JEITA EDA technical committee LSI-Package-Board Interoperable Design Working Group, Japan

TU1: LPB:

Time: Sunday, 15/Dec/2013: 2:00pm - 3:00pm · *Location:* Kinsho Hall

TU1: JEITA LSI-Package-Board (LPB) Standard Format

Yoshinori Fukuba
JEITA EDA technical committee LSI-Package-Board Interoperable Design Working Group, Japan

TU2: SEISME:

Time: Sunday, 15/Dec/2013: 3:20pm - 4:20pm · *Location:* Kinsho Hall

TU2: Simulation of Emission and Immunity of Systems and Modules Electronics

Christian MAROT[1], Andre DURIER[2], Etienne SICARD[3], Alain SAUVAGE[4], Zouhair RIAH[5], Olivier Crepel[6], Olivier MAURICE[7], Genevieve DUCHAMP[8]
[1]EADS IW, France; [2]CONTINENTAL Corporation; [3]INSA Toulouse; [4]AIRBUS SAS; [5]ESIGELEC; [6]EADS IW, France; [7]GERAC; [8]IMS-Bordeaux, France

Date: Monday, 16/Dec/2013

SI: Signal Integrity

Time: Monday, 16/Dec/2013: 8:50am - 10:10am · *Location:* Kinsho Hall

SI-1: A Technique for Estimating Signal Waveforms at Inaccessible Points in High Speed Digital Circuits **pp. 1-4**

Tomohiro Kinoshita, Shoichi Hara, Eiji Takahashi, Kazuhide Uriu, Panasonic Corporation, Japan

SI-2: Design and Measurement of a Compact On-interposer Passive Equalizer for Chip-to-chip High-speed Differential Signaling **pp. 5-9**

Heegon Kim[1], Jonghyun Cho[1], Daniel Hyunsuk Jung[1], Jonghoon Jay Kim[1], Sumin Choi[1], Junho Lee[2], Kunwoo Park[2], Joungho Kim[1]
[1]KAIST, Korea, Republic of (South Korea); [2]SK Hynix Semiconductor Inc., Korea, Republic of (South Korea)

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SI-3: Signal Integrity and EMC Performance Enhancement using 3D Integrated Circuits – A Case Study **pp. 10-14**

Etienne SICARD[1], Jianfei WU[2], Jian-cheng LI[2]
[1]INSA, France; [2]National University of Defense Technology, China

SI-4: Kron Simulation of Field-to-line Coupling using a Meshed and a Modified Taylor Cell **pp. 15-20**

Sjoerd Op 't Land[1], Richard Perdriau[1], Mohamed Ramdani[1], Olivier Maurice[2], M'hamed Drissi[3]
[1]Groupe ESEO, France; [2]GERAC, France; [3]INSA de Rennes, France

WS: APD and Near-field Measurement

Time: Monday, 16/Dec/2013: 10:40am - 12:00pm · *Location:* Kinsho Hall

WS-1: Measurement of amplitude probability distribution of an EM noise for analyzing its impact on wireless systems

Yasushi Matsumoto
National Institute of Information and Communications Technology, Japan

WS-2: Developing a Multi-channel Near-field Measurement System to Detect Electromagnetic Noise on Electronic Devices Using APD Measurement Method

Hiroshi Tsutagaya
Peritec Corporation, Japan

WS-3: Binocular analysis for RF Cross Domain Analyzer

Yasunori Hirai
Advantest Corporation, Japan

KS: Keynote Speech

Time: Monday, 16/Dec/2013: 1:50pm - 2:35pm · *Location:* Kinsho Hall

KS: Semiconductor Innovation for Smart Society and Its EMC Solutions

Toru Shimizu
Renesas Electronics Corp., Japan

EMI: Emission Measurement and Control

Time: Monday, 16/Dec/2013: 2:35pm - 3:35pm · *Location:* Kinsho Hall

EMI-1: Extraction of Deterministic and Random LSI Noise Models with the Printed Reverberation Board **pp. 21-26**

Umberto Paoletti, Takashi Suga
Hitachi, Ltd., Yokohama Research Laboratory, Japan

EMI-2: Broadband Detection of Radiating Moments using the TEM-cell and a Phase-calibrated Oscilloscope **pp. 27-32**

Renaud Gillon[1], Niko Bako[2], Adrijan Baric[2]
[1]ON Semiconductor Belgium BVBA, Belgium; [2]Faculty of Electrical Engineering, University of Zagreb, Croatia

EMI-3: Substrate Noise Reduction Based on Impedance Balance using Tunable Resistances **pp. 33-36**

Atsushi Nakamura[1], Masaaki Maeda[2], Tohlu Matsushima[2], Osami Wada[2]
[1]Renesas Electronics; [2]Kyoto University, Japan

SS: [Special Session] Tackling EMC in Real IC Chips

Time: Monday, 16/Dec/2013: 4:00pm - 6:00pm · *Location:* Kinsho Hall

SSI-1: Different IC Radiated-emission Models to Analyze Far-field Radiation of a Test PCB

Jingnan Pan, Yaojiang Zhang, Jun Fan
Missouri University of Science and Technology, United States of America

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SSI-2: An Integrated Simulation Approach for Addressing the Chip-Package-Board Power Noise Challenge
Dian Yang
Apache Design Inc. Subsidiary of ANSYS, Inc.

SS-3: Measurement-based Diagnosis of Wireless Communication Performance in the Presence of In-band Interferers in RF ICs pp. 37-41
Makoto Nagata[1], Shunsuke Shimazaki[1], Naoya Azuma[1], Satoru Takahashi[2], Motoki Murakami[3], Kazuaki Hori[3], Satoshi Tanaka[4], Masahiro Yamaguchi[4]
[1]Kobe-univ., Japan; [2]Renesas Mobile Corp, Japan; [3]Renesas Electronics Corp., Japan; [4]Tohoku Univ., Japan

SS-4: Measurements and Simulation of Substrate Noise Coupling in RF ICs with CMOS Digital Noise Emulator pp. 42-46
Naoya Azuma[1], Shunsuke Shimazaki[1], Noriyuki Miura[1], Makoto Nagata[1], Tomomitsu Kitamura[2], Satoru Takahashi[2], Motoki Murakami[3], Kazuaki Hori[3], Atsushi Nakamura[3], Kenta Tsukamoto[4], Mizuki Iwanami[4], Eiji Hankui[4], Sho Muroga[5], Yasushi Endo[5], Satoshi Tanaka[5], Masahiro Yamaguchi[5]
[1]Kobe-univ., Japan; [2]Renesas Mobile Corp, Japan; [3]Renesas Electronics Corp., Japan; [4]NEC Corporation, Japan; [5]Tohoku Univ., Japan

SS-5: In-Band Spurious Attenuation in LTE-Class RFIC Chip using a Soft Magnetic Thin Film pp. 47-52
Sho Muroga[1], Yutaka Shimada[1], Yasushi Endo[1], Satoshi Tanaka[1], Naoya Azuma[2], Makoto Nagata[2], Motoki Murakami[3], Satoru Takahashi[4], Kazuaki Hori[3], Masahiro Yamaguchi[1]
[1]Tohoku University, Japan; [2]Kobe Universiy, Japan; [3]Renesas Electronics Corporation, Japan; [4]Renesas Mobile Corporation, Japan

Date: Tuesday, 17/Dec/2013

STD: Standards for Semiconductor EMC

Time: Tuesday, 17/Dec/2013: 8:30am - 10:10am · *Location:* Kinsho Hall

STD-1: Conducted immunity of three Op-Amps using the DPI measurement technique and VHDL-AMS modeling pp. 53-58
Siham HAIROUD AIRIEAU, Tristan DUBOIS, Angelique TETELIN, Geneviève DUCHAMP
Univ. Bordeaux, IMS, UMR 5218, France

STD-2: Improvement of Reproducibility of DPI Method to Quantify RF Conducted Immunity of LDO Regulator pp. 59-62
Tohlu Matsushima, Nobuaki Ikehara, Takashi Hisakado, Osami Wada
Kyoto University, Japan

STD-3: A Generalized Accurate Modelling Method for Automotive Bulk Current Injection (BCI) Test Setups up to 1 GHz pp. 63-68
Sergey Miropolsky, Alexander Sapadinsky, Stephan Frei
AG Bordsysteme, Technische Universität Dortmund, Dortmund, Germany

STD-4: IC-Stripline Design Optimization using Response Surface Methodology pp. 69-73
Tvrtko Mandic[1], Renaud Gillon[2], Adrijan Baric[1]
[1]University of Zagreb, Faculty of Electrical Engineering and Computing, Croatia; [2]ON Semiconductors BVBA, Belguim

STD-5: Study of radiated immunity of an electronic system in a reverberating chamber pp. 74-77
Laurent GUIBERT[1], Patrick MILLOT[1], Xavier FERRIÈRES[1], Etienne SICARD[2]
[1]ONERA Centre de Toulouse, France; [2]INSA Toulouse, France

DSN: EMC-aware IC Design

Time: Tuesday, 17/Dec/2013: 10:40am - 12:00pm · *Location:* Kinsho Hall

DSN-1: Transient Analysis of EM Radiation Associated with Information Leakage from Cryptographic ICs pp. 78-82
Yuichi Hayashi[1], Naofumi Homma[1], Takafumi Aoki[1], Yuichiro Okugawa[2], Yoshiharu Akiyama[2]
[1]Tohoku University, Japan; [2]Nippon Telegraph and Telephone Corporation, Japan

DSN-2: Noise-immune Design of Schmitt Trigger Logic Gate using DTMOS for Sub-threshold Circuits pp. 83-88
KyungSoo Kim, Wansoo Nah, SoYoung Kim
SungKyunKwan University, Korea, Republic of (South Korea)

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DSN-3: Reliability Analysis of an On-chip Watchdog for Embedded Systems Exposed to Radiation and EMI pp. 89-94
Chri'stofer Oliveira[1], Juliano Benfica[1], Leti'cia BolzaniPoehls[1], Fabian Vargas[1], Jose' Lipovetzky[2], Ariel Lutenberg[2], Edmundo Gatti[3], Fernando Hernandez[4], Alexandre Boyer[5]
[1]Catholic University - PUCRS, Brazil; [2]Universidad de Buenos Aires, Buenos Aires, Argentina; [3]Instituto Nacional de Tecnologia Industrial - INTI, Buenos Aires, Argentina; [4]Universidad ORT, Montevideo, Uruguay; [5]LAAS-CNRS / Universite' de Toulouse, Toulouse, France

DSN-4: An Optimizing Technique to Lower Both Phase Noise and Susceptibility of a Voltage Controlled Oscillator pp. 95-100
Jeremy Raoult, Amable Blain, Sylvie Jarrix
IES, France

PDE: Power Device EMC

Time: Tuesday, 17/Dec/2013: 2:00pm - 3:00pm · *Location:* Kinsho Hall

PDE-1: EMC Analysis of Current Source Gate Drivers pp. 101-106
Alexis Schindler[1], Bernhard Wicht[1], Benno Koeppl[2]
[1]Reutlingen University, Germany; [2]Infineon Technologies AG

PDE-2: EMI Resisting LDO Voltage Regulator with Integrated Current Monitor pp. 107-112
Philipp Schröter[1], Stefan Jahn[1], Frank Klotz[1], Fabio Ballarin[2], Fabio Gini[2], Marco Piselli[2]
[1]Infineon Technologies AG, Germany; [2]Infineon Technologies Italia

PDE-3: A Study on Gate Voltage Fluctuation of MOSFET Induced by Switching Operation of Adjacent MOSFET in High Voltage Power Conversion Circuit pp. 113-118
Tsuyoshi Funaki
Osaka University, Japan

Poster Session

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Wei-li Sun[1], Feng-Chang Chuang[2,3], Yu-Lin Song[4], Chwen Yu[5], Tzyh-Ghuang Ma[1], Tzong-Lin Wu[2], Luh-Maan Chang[3]
[1]Communication and Electromagnetic Engineering, National Taiwan University of Science and Technology, Taipei, Taiwan; [2]Department of Electrical Engineering, National Chung Hsing University, Taichung, Taiwan.; [3]Department of Civil Engineering, National Taiwan University, Taipei, Taiwan; [4]High Technology Research Center, Yen Tjing Ling Industrial Research Institute, Taipei, Taiwan; [5]Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu, Taiwan.

PP-02: Spread Spectrum Clocking for Emission Reduction of Charge Pump Applications pp. 123-128
Bernd Deutschmann
Infineon Technologies, Germany

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Marco Cazzaniga[1,2], Patrice Joubert Doriol[1], Aurora Sanna[1], Emmanuel Blanc[3], Valentino Liberali[2], Davide Pandini[1]
[1]Central CAD and Design Solutions, STMicroelectronics, Agrate Brianza, Italy; [2]Dipartimento di Fisica, Università degli Studi di Milano, Milano, Italy; [3]Apache Design Inc., Grenoble, France

PP-04: Impedance Balance Control for Suppression of Fluctuation on Ground Voltage in LSI Package pp. 134-137
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Kyoto University, Japan

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Feng Chia University, Taiwan, Republic of China

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Shibaura Institute of Technology, Japan

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Universitat Politècnica de Catalunya (UPC), Spain

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Andre Durier[1], Olivier Crepel[2], Christian Marot[3]
[1]CONTINENTAL AUTOMOTIVE FRANCE, France; [2]EADS IW, France; [3]EADS IW, France

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Jonghoon J. Kim[1], Heegon Kim[1], Sukjin Kim[1], Bumhee Bae[1], Daniel H. Jung[1], Sunkyu Kong[1], Junho Lee[2], Kunwoo Park[2], Joungho Kim[1]
[1]KAIST, Korea, Republic of (South Korea); [2]SK Hynix Semiconductor Inc., Republic of (South Korea)

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Daniel H. Jung[1], Heegon Kim[1], Jonghoon J. Kim[1], Hyun-Cheol Bae[2], Kwang-Seong Choi[2], Joungho Kim[1]
[1]KAIST, Korea, Republic of (South Korea); [2]ETRI, Korea, Republic of (South Korea)

PP-11: The Direct RF Power Injection Method up to 18 GHz for Investigating IC's Susceptibility pp. 167-170
Yin-Cheng Chang[1], Shawn S. H. Hsu[2], Yen-Tang Chang[3], Chiu-Kuo Chen[3], Hsu-Chen Cheng[1], Da-Chiang Chang[1]
[1]National Chip Implementation Center, National Applied Research Laboratories, Hsinchu, Taiwan; [2]Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan; [3]Bureau of Standards, Metrology and Inspection, M.O.E.A, Taipei, Taiwan

Date: Wednesday, 18/Dec/2013

MDL: Power Integrity and Conducted Emission Modeling

Time: Wednesday, 18/Dec/2013: 8:50am - 10:30am · *Location:* Kinsho Hall

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Shibaura Institute of Technology, Japan

MDL-02: Estimation of Data-dependent Power Voltage Variations of FPGA by Equivalent Circuit Modeling from On-board Measurements pp. 175-179
Kengo Iokibe, Yoshitaka Toyota
Okayama Univ, Japan

MDL-03: Microcontroller Emission Simulation based on Power Consumption and Clock System pp. 180-185
Thomas Steinecke
Infineon Technologies AG, Germany

MDL-04: A Microcontroller Conducted EMI Model Building for Software-level Effect pp. 186-189
Shih-Yi Yuan
Feng Chia University, Taiwan, Republic of China

MDL-05: Characterization and Modeling of Electrical Stresses on Digital Integrated Circuits Power Integrity and Conducted Emission pp. 190-195
Alexandre BOYER, Sonia BEN DHIA
LAAS-CNRS, France

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ERE: ESD and Robustness Evaluation in IC-level

Time: Wednesday, 18/Dec/2013: 11:00am - 12:00pm · *Location:* Kinsho Hall

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Thomas Steinecke[1], Markus Unger[1], Stanislav Scheier[2], Stephan Frei[2], Josip Bačmaga[3], Adrijan Barić[3]
[1]Infineon Technologies AG, Germany; [2]Technical University of Dortmund, Germany; [3]University of Zagreb, Croatia

ERE-2: Automatic Verification of EMC Immunity by Simulation **pp. 202-207**
Bertrand Vrignon[1], Pascal Caunegre[1], John Shepherd[1], Jianfei Wu[2]
[1]Freescale, France; [2]National University of Defense Technology, China

ERE-3: Electro-Magnetic Robustness of Integrated Circuits: from statement to prediction **pp. 208-213**
Sonia Ben Dhia, Alexandre Boyer
INSA - LAAS, France

IM1: Chip Level Immunity

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IM1-1: EMC Immunity of Integrated Smart Power Transistors in a non-50Ω Environment **pp. 214-219**
Hermann Nzalli[1], Wolfgang Wilkening[1], Rolf H. Jansen[2]
[1]Robert Bosch GmbH, Germany; [2]Chair of EM Theory (RWTH Aachen University), Germany

IM1-2: Discrete Low-frequency Transistors Subjected to High-frequency CW and Pulse-modulated Sine Signals **pp. 220-225**
Sylvie JARRIX[1], Jeremy RAOULT[1], Adrien DORIDANT[1], Clovis POUANT[2], Patrick HOFFMANN[2]
[1]Institut d 'Electronique du Sud, France; [2]CEA Gramat, France

IM1-3: Noise Analysis using On-chip Waveform Monitor in Bandgap Voltage References **pp. 226-231**
Akitaka Murata[1], Shuji Agatsuma[1], Daisaku Ikoma[1], Kouji Ichikawa[1], Takahiro Tsuda[1], Makoto Nagata[2], Kumpei Yoshikawa[2], Yuuki Araga[2], Yuji Harada[2]
[1]DENSO CORPORATION, Japan; [2]Kobe University, Japan

IM1-4: Immunity Evaluation of Inverter Chains against RF Power on Power Delivery Network **pp. 232-237**
Kumpei Yoshikawa[1], Yuji Harada[1], Noriyuki Miura[1], Noriaki Takeda[2], Yoshiyuki Saito[2], Makoto Nagata[1,3]
[1]Kobe University, Japan; [2]Panasonic Corporation, Japan; [3]CREST, JST

IM2: Automotive Immunity

Time: Wednesday, 18/Dec/2013: 3:50pm - 4:50pm · *Location:* Kinsho Hall

IM2-1: Magnetic Field Coupling on Analog-to-digital Converter from Wireless Power Transfer System in Automotive Environment **pp. 238-242**
Bumhee Bae, Sunkyu Kong, Joonghoon J Kim, Sukjin Kim, Joungho Kim
KAIST, Korea, Republic of (South Korea)

IM2-2: Immunity Simulation Method for Automotive Power Module using Electromagnetic Analysis **pp. 243-248**
Yosuke Kondo, Kei Tsunada, Norimasa Oka, Masato Izumichi
DENSO CORPORATION, Japan

IM2-3: Translation of Automotive Module RF Immunity Test Limits into Equivalent IC Test Limits using S-parameter IC Models **pp. 249-253**
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[1]Melexis Technologies, Tessenderlo, Belgium; [2]Continental Automotive France, Toulouse, France; [3]Ghent University, INTEC, Gent, Belgium