

2014 27th International Conference on VLSI Design and 2014 13th International Conference on Embedded Systems

**Mumbai, India
5 – 9 January 2014**



**IEEE Catalog Number: CFP14041-POD
ISBN: 978-1-4799-2514-8**

**2014 27th International Conference
on VLSI Design and 2014 13th
International Conference on Embedded
Systems**

VLSID 2014

Table of Contents

| | |
|---|--------|
| Message from the Steering Committee Chair..... | xv |
| Welcome Message..... | xvi |
| Welcome Message from the General Chair..... | xvii |
| Welcome Message from the Program Chairs..... | xix |
| Message from the President, VLSI Society of India..... | xxi |
| Message from the Tutorial Co-Chairs..... | xxii |
| Message from the User/Designer Track Chair..... | xxiii |
| VLSI Design Conference Steering Committee (2013)..... | xxiv |
| VLSI Design 2013 Conference Committee..... | xxv |
| Program Committee..... | xxviii |
| Plenary Talk Abstracts..... | xxxiv |
| About the Cover from the Publication Co-Chairs..... | xliv |
| VLSI Design Conference History..... | xlvi |
| Embedded Systems Design Conference History..... | xlvii |
| Conference Program..... | xlviii |
| Call for Papers — VLSI Design and Test Symposium (VDAT 2014)..... | li |

Tutorials

| | |
|--|---|
| Tutorial T1: Ambient Intelligence through Internets-of-Things—An Application Development Approach | 1 |
| <i>Anil Kumar Gupta, Anand Singh, and Vineeta Yadav</i> | |
| Tutorial T2A: Scheduling Issues in Embedded Real-Time Systems | 2 |
| <i>Parmesh Ramanathan</i> | |
| Tutorial T2B: Cost / Application / Time to Market Driven SoC Design and Manufacturing Strategy | 3 |
| <i>Barun Kumar De, Anupam Chattopadhyay, and Ansuman Banerjee</i> | |

| | |
|--|----|
| Tutorial T3A: Testing Low-Power Integrated Circuits: Challenges, Solutions, and Industry Practices | 5 |
| <i>Srivaths Ravi, Vivek Chickermane, and Krishna Chakravadhanula</i> | |
| Tutorial T3B: Engineering Change Order (ECO) Phase Challenges and Methodologies for High Performance Design | 7 |
| <i>Sridhar Rangarajan, Pinaki Chakrabarti, Sourav Sahais, Ayan Datta, and Adarsh Subramanya</i> | |
| Tutorial T4: All You Need to Know about Hardware Trojans and Counterfeit ICs | 9 |
| <i>Mohammad Tehranipoor and Domenic Forte</i> | |
| Tutorial T5: Microfluidic Biochips: Connecting VLSI and Embedded Systems to the Life Sciences | 11 |
| <i>Krishnendu Chakrabarty and Tsung-Yi Ho</i> | |
| Tutorial T6A: Pedagogy of Negative Feedback Circuits | 13 |
| <i>Nagendra Krishnapura</i> | |
| Tutorial T6B: Embedded Memory Design for Future Technologies: Challenges and Solutions | 14 |
| <i>Swaroop Ghosh</i> | |
| Tutorial T7A: Techniques for Network-on-Chip (NoC) Design and Test | 16 |
| <i>Santanu Chattopadhyay</i> | |
| Tutorial T7B: Network on Chips—The Journey Overview | 18 |
| <i>Joycee Mekie and Sneha N. Ved</i> | |
| Tutorial T8A: Realization of RF Front-End for a Cognitive Radio | 19 |
| <i>B. Ravi Kishore and B. Kameswara Rao</i> | |
| | |
| Session A1: 3D Test | |
| A Test Partitioning Technique for Scheduling Tests for Thermally Constrained 3D Integrated Circuits | 20 |
| <i>Spencer K. Millican and Kewal K. Saluja</i> | |
| Analytical Modeling of 3D Stacked IC Yield from Wafer to Wafer Stacking with Radial Defect Clustering | 26 |
| <i>Eshan Singh</i> | |
| Process-Variation Aware Multi-temperature Test Scheduling | 32 |
| <i>Nima Aghaee, Zebo Peng, and Petru Eles</i> | |
| Reliability Aware Gate Sizing Combating NBTI and Oxide Breakdown | 38 |
| <i>Subhendu Roy and David Z. Pan</i> | |

Session A2: SAT Application

| | |
|--|----|
| Debug Automation for Synchronization Bugs at RTL | 44 |
| <i>Mehdi Dehbashi and Görschwin Fey</i> | |
| Techniques to Improve the Efficiency of SAT Based Path Delay Test Generation | 50 |
| <i>Kun Bian, D.M.H. Walker, and Sunil P. Khatri</i> | |
| SAT-Based Test Pattern Generation with Improved Dynamic Compaction | 56 |
| <i>Alexander Czutro, Sudhakar M. Reddy, Ilia Polian, and Bernd Becker</i> | |
| Efficient SAT-Based Circuit Initialization for Larger Designs | 62 |
| <i>Matthias Sauer, Sven Reimer, Sudhakar M. Reddy, and Bernd Becker</i> | |

Session A3: Design Verification

| | |
|---|----|
| A Coverage Guided Mining Approach for Automatic Generation of Succinct Assertions | 68 |
| <i>David Sheridan, Lingyi Liu, Hyungsul Kim, and Shobha Vasudevan</i> | |
| Effective Liveness Verification Using a Transformation-Based Framework | 74 |
| <i>Pradeep Kumar Nalla, Raj Kumar Gajavelly, Hari Mony, Jason Baumgartner, and Robert Kanzelman</i> | |
| Formal Verification and Debugging of Array Dividers with Auto-correction Mechanism | 80 |
| <i>M.H. Hagbayan, B. Alizadeh, P. Behnam, and S. Safari</i> | |
| All-SAT Using Minimal Blocking Clauses | 86 |
| <i>Yinlei Yu, Pramod Subramanyan, Nestan Tsiskaridze, and Sharad Malik</i> | |

Session A4: Test Generation

| | |
|--|-----|
| CryptIP: An Approach for Encrypting Intellectual Property Cores with Simulation Capabilities | 92 |
| <i>Spencer Millican, Parameswaran Ramanathan, and Kewal Saluja</i> | |
| A Cube-Aware Compaction Method for Scan ATPG | 98 |
| <i>Sharada Jha, Kameshwar Chandrasekar, Weixin Wu, Ramesh Sharma, Sanjay Sengupta, and Sudhakar M. Reddy</i> | |
| Scalable Test Generation by Interleaving Concrete and Symbolic Execution | 104 |
| <i>Xiaoke Qin and Prabhat Mishra</i> | |
| Application of Test-View Modeling to Hierarchical ATPG | 110 |
| <i>Rahul Shukla, Phong Loi, Ken Pham, Arie Margulis, Kathy Yang, and Nagesh Tamarapalli</i> | |

Session A5: Reliable Circuits

| | |
|---|-----|
| A New Sensitivity-Driven Process Variation Aware Self-Repairing Low-Power SRAM Design | 116 |
| <i>Nandakishor Yadav, Sunil Dutt, and G.K. Sharma</i> | |
| Timing Variation Adaptive Pipeline Design: Using Probabilistic Activity Completion Sensing with Backup Error Resilience | 122 |
| <i>Jayaram Natarajan, Sahil Kapoor, Debesh Bhatta, Abhijit Chatterjee, and Adit Singh</i> | |
| A Novel Low Power Error Detection Logic for Inexact Leading Zero Anticipator in Floating Point Units | 128 |
| <i>B. Naveen Kumar Reddy, M. Chandra Sekhar, Sreehari Veeramachaneni, and M.B. Srinivas</i> | |
| Better-than-Worst-Case Timing Design with Latch Buffers on Short Paths | 133 |
| <i>Ravi Kanth Uppu, Ravi Tej Uppu, Adit D. Singh, and Ilia Polian</i> | |

Session A6: Memory

| | |
|--|-----|
| Pipelined Non-strobed Sensing Scheme for Lowering BL Swing in Nano-scale Memories | 139 |
| <i>Sudhanshu Khanna, Satyanand V. Nalam, and Benton H. Calhoun</i> | |
| Energy Efficient Memory Decoder Design for Ultra-low Voltage Systems | 145 |
| <i>K.R. Viveka and Bharadwaj Amrutur</i> | |
| A 500 mV to 1.0 V 128 Kb SRAM in Sub 20 nm Bulk-FinFET Using Auto-adjustable Write Assist | 150 |
| <i>Prashant Dubey, Gaurav Ahuja, Vaibhav Verma, Sanjay Kumar Yadav, and Amit Khanuja</i> | |
| Minimizing Power and Skew in VLSI-SoC Clocking with Pulsed Resonance Driven De-skewing Latches | 156 |
| <i>Ignatius Bezzam and Shoba Krishnan</i> | |

Session B1: Real-Time Systems

| | |
|--|-----|
| Efficient Two-Phase Approaches for Branch-and-Bound Style Resource Constrained Scheduling | 162 |
| <i>Mingsong Chen, Fan Gu, Lei Zhou, Geguang Pu, and Xiao Liu</i> | |
| Inserting Placeholder Slack to Improve Run-Time Scheduling of Non-preemptible Real-Time Tasks in Heterogeneous Systems | 168 |
| <i>Hsiang-Kuo Tang, Parmesh Ramanathan, and Katherine Morrow</i> | |
| Hardware Implementation of Real-Time, High Performance, RCE-NN Based Face Recognition System | 174 |
| <i>Santu Sardar and K. Ananda Babu</i> | |

Session B2: Embedded Platform

| | |
|---|-----|
| EME Electric Supervision Embedded on Gas Panel with Microshock Dangerousness Degree | 180 |
| <i>Marcelo Trindade Rebonatto, Fabiano Passuelo Hessel, and Luiz Eduardo Schardong Spalding</i> | |
| Design of AFE and PWM Drive for Lithium-Ion Battery Management System for HEV/EV System | 186 |
| <i>Sudhakar Singamala, Manfred Brandl, Sandeep Vernekar, Veereshbabu Vulligadala, Ravikumar Adusumalli, and Vijay Ele</i> | |
| Process Disturbance Analyzer for Nuclear Reactors | 192 |
| <i>E.M.T. Sirisha, T. Sridevi, and D. Thirugnana Murthy</i> | |
| Design and Implementation of Safety Logic with Fine Impulse Test System for a Nuclear Reactor Shutdown System | 198 |
| <i>Manoj Kumar Misra, N. Sridhar, and D. Thirugnana Murthy</i> | |

Session B3: Architectures

| | |
|--|-----|
| Performance and Power Benefits of Sharing Execution Units between a High Performance Core and a Low Power Core | 204 |
| <i>Rance Rodrigues, Israel Koren, and Sandip Kundu</i> | |
| Process Synchronization in Multi-core Systems Using On-Chip Memories | 210 |
| <i>Arun Joseph and Nagu R. Dhanwada</i> | |
| TECS: Temperature- and Energy-Constrained Scheduling for Multicore Systems | 216 |
| <i>Xiaoke Qin and Prabhat Mishra</i> | |
| Challenges in Implementing Cache-Based Side Channel Attacks on Modern Processors | 222 |
| <i>Jyoti Gajrani, Pooja Mazumdar, Sampreet Sharma, and Bernard Menezes</i> | |

Session B4: Network-on-Chip

| | |
|--|-----|
| Tiny NoC: A 3D Mesh Topology with Router Channel Optimization for Area and Latency Minimization | 228 |
| <i>César Marcon, Ramon Fernandes, Rodrigo Cataldo, Fernando Grando, Thais Webber, Ana Benso, and Leticia B. Poehls</i> | |
| NoC Scheduling for Improved Application-Aware and Memory-Aware Transfers in Multi-core Systems | 234 |
| <i>Tejasi Pimpalkhute and Sudeep Pasricha</i> | |
| CARM: Congestion Adaptive Routing Method for On Chip Networks | 240 |
| <i>Manoj Kumar, Vijay Laxmi, Manoj Singh Gaur, Seok-Bum Ko, and Mark Zwolinski</i> | |

| | |
|---|-----|
| Knowledge-Guided Methodology for Third-Party Soft IP Analysis | 246 |
| <i>Bhanu Singh, Arunprasath Shankar, Francis Wolff, Daniel Weyer,</i> | |
| <i>Christos Papachristou, and Bhanu Negi</i> | |

Session B5: MPSoCs

| | |
|---|-----|
| Pre-mapping Algorithm for Heterogeneous MPSoCs | 252 |
| <i>César Marcon, Thais Webber, Leticia B. Poehls, and Igor K. Pinotti</i> | |
| Efficient QR Decomposition Using Low Complexity Column-wise Givens Rotation (CGR) | 258 |
| <i>Farhad Merchant, Anupam Chattopadhyay, Ganesh Garga, S.K. Nandy,</i> | |
| <i>Ranjani Narayan, and Nandhini Gopalan</i> | |
| Temperature Minimization Using Power Redistribution in Embedded Systems | 264 |
| <i>Rehan Ahmed, Parameswaran Ramanathan, and Kewal K. Saluja</i> | |
| Process Variation Aware Synthesis of Application-Specific MPSoCs to Maximize Yield | 270 |
| <i>Nishit Kapadia and Sudeep Pasricha</i> | |

Session B6: Embedded Systems

| | |
|---|-----|
| Hard versus Soft Software Defined Radio | 276 |
| <i>Wim Meeus, Tom Vander Aa, Praveen Raghavan, and Dirk Stroobandt</i> | |
| Interfacing Synchronous and Asynchronous Domains for Open Core Protocol | 282 |
| <i>Vikas S. Vij, Raghu Prasad Gudla, and Kenneth S. Stevens</i> | |
| Control Mechanism to Solve False Blocking Problem at MAC Layer in Wireless Sensor Networks | 288 |
| <i>Brajendra K. Singh, Kemal E. Tepe, and Mohammed A.S. Khalid</i> | |
| Architecture for Blocking Detection in Wireless Video Source Authentication | 294 |
| <i>Amit Pande, Shaxun Chen, Prasant Mohapatra, and Gaurav Pande</i> | |

Session C1: FPGA

| | |
|---|-----|
| A Novel Architecture for FPGA Implementation of Otsu's Global Automatic Image Thresholding Algorithm | 300 |
| <i>J.G. Pandey, A. Karmakar, C. Shekhar, and S. Gurunarayanan</i> | |
| Accelerating Genome Assembly Using Hard Embedded Blocks in FPGAs | 306 |
| <i>B. Sharat Chandra Varma, Kolin Paul, and M. Balakrishnan</i> | |
| A Hardware Intensive Approach for Efficient Implementation of Numerical Integration for FPGA Platforms | 312 |
| <i>Burhan Khurshid and Roohie Naz Mir</i> | |
| Embedded Complex Floating Point Hardware Accelerator | 318 |
| <i>Amin Ghasemazar, Mehran Goli, and Ali Afzali-Kusha</i> | |

Session C2: Low-Power Design

| | |
|--|-----|
| A Power Efficient Video Encoder Using Reconfigurable Approximate Arithmetic Units | 324 |
| <i>Arnab Raha, Hrishikesh Jayakumar, and Vijay Raghunathan</i> | |
| QUICKRECALL: A Low Overhead HW/SW Approach for Enabling Computations across Power Cycles in Transiently Powered Computers | 330 |
| <i>Hrishikesh Jayakumar, Arnab Raha, and Vijay Raghunathan</i> | |
| Configurable Systolic Matrix Multiplication | 336 |
| <i>Parastoo Kamranfar, S. Ali Shahabi, Ghazaleh Vazhbakht, and Zainalabedin Navabi</i> | |
| ProCA: Progressive Configuration Aware Design Methodology for Low Power Stochastic ASICs | 342 |
| <i>Neel Gala, V.R. Devanathan, Karthik Srinivasan, V. Visvanathan, and V. Kamakoti</i> | |

Session C3: Digital Design

| | |
|---|-----|
| Hardware Efficient VLSI Architecture for 3-D Discrete Wavelet Transform | 348 |
| <i>Anand Darji, Saurabh Shukla, S.N. Merchant, and A.N. Chandorkar</i> | |
| Design and Implementation of High Throughput and Area Efficient Hard Decision Viterbi Decoder in 65nm Technology | 353 |
| <i>Narayan V. Sugur, Saroja V. Siddamal, and Samba Sivam Vemala</i> | |
| Scalable Low Power FFT/IFFT Architecture with Dynamic Bit Width Configurability | 359 |
| <i>Sundarajan Rangachari, Jaiganesh Balakrishnan, and Nitin Chandrachoodan</i> | |
| A Decimal/Binary Multi-operand Adder Using a Fast Binary to Decimal Converter | 365 |
| <i>Ch. Santosh Varma, Syed Ershad Ahmed, and M.B. Srinivas</i> | |

Session C4: Physical Design

| | |
|--|-----|
| Global Routing Using Monotone Staircases with Minimal Bends | 369 |
| <i>Bapi Kar, Susmita Sur-Kolay, and Chittaranjan Mandal</i> | |
| Delete and Correct (DaC): An Atomic Logic Operation for Removing Any Unwanted Wire | 375 |
| <i>Xing Wei, Tak-Kei Lam, Xiaoqing Yang, Wai-Chung Tang, Yi Diao, and Yu-Liang Wu</i> | |
| On Manufacturing Aware Physical Design to Improve the Uniqueness of Silicon-Based Physically Unclonable Functions | 381 |
| <i>Raghavan Kumar, Siva Nishok Dhanuskodi, and Sandip Kundu</i> | |
| Obstacle Avoiding Rectilinear Clock Tree Construction with Skew Minimization | 387 |
| <i>Partha Pratim Saha and Tuhina Samanta</i> | |
| Layout-Aware Delay Variation Optimization for CNTFET-Based Circuits | 393 |
| <i>Matthias Beste, Saman Kiamehr, and Mehdi B. Tahoori</i> | |

Session C5: Modeling and Simulation

| | |
|---|-----|
| Leakage Modeling for Devices with Steep Sub-threshold Slope Considering Random Threshold Variations | 399 |
| <i>Ayan Paul, Chaitanya Kshirsagar, Sachin S. Sapatnekar, Steven Koester, and Chris H. Kim</i> | |
| Small Signal Nonquasi-static Model for Common Double-Gate MOSFETs Adapted to Gate Oxide Thickness Asymmetry | 405 |
| <i>Neha Sharan and Santanu Mahapatra</i> | |
| Analytical Modeling of Sub-onset Current of Tunnel Field Effect Transistor | 411 |
| <i>Parmanand Singh, Vivek Asthana, Radhakrishnan Sithanandam, Anand Bulusu, and Sudeb Das Gupta</i> | |
| Statistical Modeling of Glitching Effects in Estimation of Dynamic Power Consumption | 415 |
| <i>Michael Meixner and Tobias G. Noll</i> | |

Session C6: Modeling and Analysis

| | |
|--|-----|
| BSIM6—Benchmarking the Next-Generation MOSFET Model for RF Applications | 421 |
| <i>Anupam Dutta, Saurabh Sirohi, Tamilmani Ethirajan, Harshit Agarwal, Yogesh Singh Chauhan, and Richard Q. Williams</i> | |
| Analysis of Nanoscale Strained-Si/SiGe MOSFETs including Source/Drain Series Resistance through a Multi-iterative Technique | 427 |
| <i>Amrita Kumari and Subindu Kumar</i> | |
| An ABCD Parameter Based Modeling and Analysis of Crosstalk Induced Effects in Multiwalled Carbon Nanotube Bundle Interconnects | 433 |
| <i>Manodipan Sahoo, Prasun Ghosal, and Hafizur Rahaman</i> | |
| Performance Optimization and Parameter Sensitivity Analysis of Ultra Low Power Junctionless MOSFETs | 439 |
| <i>Mukta Singh Parihar and Abhinav Kranti</i> | |

Session D1: RF Circuits

| | |
|--|-----|
| Improvements to Negative-C Compensation Based Amplifiers for Broadband Applications | 444 |
| <i>Rajesh Cheeranthodi, Santhosh Madhavan, Umesh K. Shukla, and Giri N. Rangan</i> | |
| An Adaptive Inductorless Continuous Time Equalizer for Gigabit Links in 0.13 um CMOS | 450 |
| <i>Sushrant Monga and Shouri Chatterjee</i> | |
| On Dependence of Amplitude Noise versus Offset Frequency in LC Oscillators | 455 |
| <i>R. Sivaramakrishna and Shalabh Gupta</i> | |

| | |
|--|-----|
| A 1 V, Sub-mW CMOS LNA for Low-Power 1 GHz Wide-Band Wireless Applications | 460 |
| <i>Arunkumar Salimath, Pradeep Karamcheti, and Achintya Halder</i> | |

Session D2: LP Circuits

| | |
|---|-----|
| Low Power Single Amplifier Voltage Regulator | 466 |
| <i>Sanjay Kumar Wadhwa, Jaideep Banerjee, and Rakesh Kumar Gupta</i> | |
| Forward Body Biased Adiabatic Logic for Peak and Average Power Reduction in 22nm CMOS | 470 |
| <i>Matthew Morrison and Nagarajan Ranganathan</i> | |
| FinFET Logic Circuit Optimization with Different FinFET Styles: Lower Power Possible at Higher Supply Voltage | 476 |
| <i>Sourindra Chaudhuri and Niraj K. Jha</i> | |
| Operand Isolation with Reduced Overhead for Low Power Datapath Design | 483 |
| <i>Lokesh Siddhu, Amit Mishra, and Virendra Singh</i> | |
| High-Speed, Low-Power Quasi Delay Insensitive Handshake Circuits Based on FinFET Technology | 489 |
| <i>Mohammad Yousef Zarei, Mahdi Mosaffa, and Siamak Mohammadi</i> | |

Session D3: MEMS/Biochips

| | |
|--|-----|
| Active Cooling Technique for Efficient Heat Mitigation in 3D-ICs | 495 |
| <i>Pramod Kaddi, Basireddy Karunakar Reddy, and Shiv Gobind Singh</i> | |
| Improved Design Methodology for the Development of Electrically Actuated MEMS Structures | 499 |
| <i>AVSS Prasad, K.P. Venkatesh, Rudra Pratap, and Navakanta Bhat</i> | |
| Correctness Checking of Bio-chemical Protocol Realizations on a Digital Microfluidic Biochip | 504 |
| <i>Sukanta Bhattacharjee, Ansuman Banerjee, Krishnendu Chakrabarty, and Bhargab B. Bhattacharya</i> | |
| A Novel Wire Planning Technique for Optimum Pin Utilization in Digital Microfluidic Biochips | 510 |
| <i>Pranab Roy, Samadrita Bhattacharya, Rupam Bhattacharyay, Firdousi Jamil Imam, Hafizur Rahaman, and Parthasarathi Dasgupta</i> | |

Session D4: Analog Circuits I

| | |
|---|-----|
| Output Impedance as Figure of Merit to Predict Transient Performance for Embedded Linear Voltage Regulators | 516 |
| <i>Saurabh Kumar Singh and Nitin Bansal</i> | |
| A Time-Based Low Voltage Body Temperature Monitoring Unit | 522 |
| <i>Karthik Ramkumar Jeyashankar, Makrand Mahalley, and Bharadwaj Amrutur</i> | |

| | |
|--|-----|
| Trimless, PVT Insensitive Voltage Reference Using Compensation of Beta and Thermal Voltage | 528 |
| <i>Hande Vinayak Gopal and Maryam Shojaei Baghini</i> | |
| A Low Power CMOS Imager Based on Distributed Compressed Sensing | 534 |
| <i>Bhuvanankaliannan and Vijaya Sankara Rao Pasupureddi</i> | |
| Session D5: Emerging Technologies | |
| All Optical Reversible Multiplexer Design Using Mach-Zehnder Interferometer | 539 |
| <i>Kamalika Datta and Indranil Sengupta</i> | |
| Circuit for Reversible Quantum Multiplier Based on Binary Tree Optimizing Ancilla and Garbage Bits | 545 |
| <i>Saurabh Kotiyal, Himanshu Thapliyal, and Nagarajan Ranganathan</i> | |
| Design of Dedicated Reversible Quantum Circuitry for Square Computation | 551 |
| <i>H.V. Jayashree, Himanshu Thapliyal, and Vinod Kumar Agrawal</i> | |
| An Optimized Design of Reversible Quantum Comparator | 557 |
| <i>P. Sai Phaneendra, Chetan Vudadha, V. Sreehari, and M.B. Srinivas</i> | |
| Session D6: Analog Circuits II | |
| Light Load Efficiency Improvement in High Frequency DC-DC Buck Converter Using Dynamic Width Segmentation of Power MOSFET | 563 |
| <i>N.J. Metilda Sagaya Mary, Ashis Maity, and Amit Patra</i> | |
| Histogram Based Deterministic Digital Background Calibration for Pipelined ADCs | 569 |
| <i>Chithira Ravi, T. Rahul, and Bibhudatta Sahoo</i> | |
| A Power Efficient Fully Differential Back Terminated Current-Mode HDMI Source | 575 |
| <i>R. Gopikrishnan, Vijaya Sankara Rao Pasupureddi, and Govindarajulu Regeti</i> | |
| An Adaptive Body-Biased Clock Generation System in 28nm CMOS | 580 |
| <i>Makarand Shirasgaonkar, Roxanne Vu, Deborah Dressler, Nhat Nguyen, Kambiz Kaviani, and Yueyong Wang</i> | |
| Author Index | 584 |