

2013 IEEE 26th International SQC Conference

(SOCC 2013)

**Erlangen, Germany
4-6 September 2013**



**IEEE Catalog Number: CFP13ASI-POD
ISBN: 978-1-4799-1165-3**

TABLE OF CONTENTS

Welcome

Norbert Schuhmann, Fraunhofer IIS, General Chair

Technical Program

Kaijian Shi, Cadence Design Systems, Technical Program Chair

Keynote: "The Roadway to Innovation"

Ron Martino, Vice President, Automotive MCU Product Group, Freescale Semiconductor

Plenary: "The pig in the poke? – Strategies to avoid unpleasant surprises with IP on your SoC"

Carsten Elgert, Product Marketing Director IP-Group, Cadence Design Systems

Plenary: "Visions of future SoC Design: Why heterogeneous Architectures and Power matter"

Volker Politz, Vice President of Business Development, Imagination, Inc., USA

Session WA1A: Design for Testability, and Manufacturability

Chair: Andrew Marshall, University Dallas at Texas

WA1A.1 Design OF 2xVDD logic gates with only 1xVDD devices in nanoscale CMOS technology

*Po-Yen Chiu and Ming-Dou Ker
National Chiao Tung University, Taiwan*

WA1A.2 An Optimal Design of a Fault Tolerant Reversible Multiplier

*Lafifa Jamal, Md. Mushfiqur Rahman, Hafiz Md Hasan Babu
University of Dhaka, Bangladesh*

WA1A.3 Layout regularity metric as a fast indicator of high variability circuits

*Esraa Swillam¹, Kareem Madkour², Mohab Anis³
¹Mentor Graphics, ²Mentor Graphics, University of Waterloo, ³American University in Cairo*

Session WA1B: Biomedical Circuits and Systems

Chair: Ken Hsu, Rochester Institute of Technology

WA1B.1 Architecture and Circuit design of parallel processing elements for De Novo sequence assembly

*Yu-Long Huang, Chun-Shen Liu, Yu-Cheng Li, Yi-Chang Lu
National Taiwan University*

WA1B.2 UWB Receiver for Breast Cancer Detection: Comparison Between Two Different Approaches

*Xiaolu Guo, Mario R. Casu, Mariagrazia Graziano, Maurizio Zamboni
Politecnico di Torino*

WA1B.3 A New Data Acquisition Design for Breast Cancer Detection System

*Dung Nguyen¹, Kui Ren², Janet Roveda¹
¹Univ. of Arizona, ²State University of New York*

Session WP1A: Wireline and Wireless Communication Circuits and Systems

Chair: Abbas Amira, University of the West of Scotland

WP1A.1 A 72dBΩ 11.43mA Novel CMOS Regulated Cascode TIA for 3.125Gb/s Optical Communications

*Young-Ho Kim and Sang-Soo Lee
Electronics and Telecommunications Research Institute(ETRI)*

WP1A.2 PKF: A communication cost reduction schema based on Kalman filter and data prediction for wireless sensor networks

*Yanqiu Huang and Alberto Garcia-Ortiz
University of Bremen*

WP1A.3 A 6Gb/s 40dB Burst-Mode Digitally Adaptive Equalizer with Reference-Calibrated Overshoot Control

*Sheng-Kai You, Po-Hsuan Chang, Chia-Ming Tsai
National Chiao Tung University*

WP1A.4 Adaptive driver with automatic sense and calibration in CMOS 40LP

*Sushrant Monga
IIT Delhi*

Session WP1B - Green Circuits, Systems, and Design Methodologies

Chair: Thomas Büchner, IBM

WP1B.1 Sub-10 μW CMOS wake-up receiver IP for green SoC design

*Heinrich Milosiu and Frank Oehler
Fraunhofer IIS*

WP1B.2 A dual-edged triggered explicit pulsed level converting Flip-Flop with a wide operation range

*Mei-Wei Chen¹, Ming-Hung Chang¹, Pei-Chen Wu¹, Yi-Ping Kuo¹, Chun-Lin Yang¹, Yuan-Hua Chu², Wei Hwang¹
¹National Chiao Tung University, ²Industrial Technology Research Institute*

WP1B.3 An Efficient Approach for Designing a Reversible Fault Tolerant n-Bit Carry Look-Ahead Adder

*Hafiz Md Hasan Babu and Lafifa Jamal
University of Dhaka, Bangladesh*

Session WP2A - Embedded Systems, Multi/Many Core Systems and Embedded Memory Technologies

Chair: Kaiming Ho, Fraunhofer IIS

WP2A.1 Method for Resolving Simultaneous Same Row Access in Dual-Port 8T SRAM with Asynchronous Dual-Clock Operation

*Nan-Chun Lien, Ching-Te Chuang, Wen-Rong Wu
National Chiao Tung University*

WP2A.2 A 40nm 1.0Mb 6T Pipeline SRAM with Digital-Based Bit-Line Under-Drive, Three-Step-Up Word-Line, Adaptive Data-Aware Write-Assist with VCS Tracking and Adaptive Voltage Detector for Boosting Control

*Wei-Nan Liao¹, Nan-Chun Lien¹, Chi-Shin Chang¹, Li-Wei Chu¹, Hao-I Yang¹, Ching-Te Chuang¹, Shyh-Jye Jou¹, Wei Hwang¹, Ming-Hsien Tu², Huan-Shun Huang², Jian-Hao Wang², Paul-Sen Kan², Yong-Jyun Hu²
¹National Chiao Tung University, ²Faraday Technology Corporation*

WP2A.3 A BCH decoding architecture with mixed parallelization degrees for flash controller applications

*Jens Spinner¹, Jürgen Freudenberger¹, Christoph Baumhof², Axel Mehner², Richard Willems²
¹University of Applied Sciences, Konstanz, Germany, ²Hyperstone GmbH, Konstanz, Germany*

Session WP2B - Digital Signal Processing (DSP) Circuits and Systems

Chair: Andrew Marshall, University of Dallas at Texas

WP2B.1 Development of Advanced Diagnostic Functions in Very High Volume Automotive Sensor Applications

*Martin Krey, Daniel Sabotta, Fabian Zahn, Karl-Ragmar Riemschneider, Rasmus Rettig
Hamburg University of Applied Sciences*

WP2B.2 Light field data processor design for depth estimation using confidence-assisted disparities

*Shih-Chieh Fan Chiang, Po-Hsiang Hsu, Yi-Chang Lu
National Taiwan University*

WP2B.3 Analysis and implementation of Discrete Wavelet Transform for compressing four-dimensional light field data

*Chun-Liang Kuo, Yang-Yao Lin, Yi-Chang Lu
National Taiwan University*

H YAD' GtcfmUbX'AcfY. DYfWdli U'5 i X]c'7 cX]b['Zca]]tg'6 Y[]bb]b[g'Hc'h YDfYgYbh**% -

*"Lwt i gp'J gtt g
"Wpkgtukf 'Gtrcpi gp/Pwgtpdgti
"Kvgt pc vkpci' Cwf kq'Ncdu'Gtrcpi gp*

Session TT1A - **Embedded Tutorial**

Chair: Thomas Büchner, IBM

Methodology for Designing Reliable Clock Networks

Prof. Dr. Taewhan Kim, Seoul National Univ., Korean

Session TT1B - **Embedded Tutorial**

Chair: Yuejian Wu, Infinera

The Uncertain End to Silicon

Prof. Dr. Andrew Marshall, The University of Texas at Dallas and Dr. Karan Bhatia, Texas Instruments

Session TPL1 - **Plenary Session**

Chair: Kaijian Shi, Cadence Design Systems

Processor-To-Memory Interface Design Methodologies for Energy and Performance Efficiencies

Bill Huffman, Chief Architect, Tensilica

Session TA1A - System Level Design Methodology and tools

Chair: Gerd Ascheid, University Aachen RWTH

TA1A.1 Multiple Terminal Reduction Method

*Goro Suzuki
University of Kitakyu-shu, Japan*

TA1A.2 High-level TSV Resource Sharing and Optimization for TSV Based 3D IC Designs

*Byunghyun Lee¹ and Taewhan Kim²
¹Samsung Electronics Co. Ltd, ²Seoul National University*

TA1A.3 Latency-Optimization Synthesis with Module Selection for Digital Microfluidic Biochips

*Chia-Hung Liu, Kuang-Cheng Liu, Juinn-Dar Huang
National Chiao Tung University*

Session TA1B - Analog and Mixed-Signal Circuits and Systems

Chair: Karan Batia, Texas Instruments

TA1B.1 ViLoCoN - An Ultra Lightweight Lossless VLSI Video Codec

*Ran Manevich, Shani Rehana, Or Turgeman, Avinoam Kolodny
Technion - Israel Institute of Technology*

TA1B.2 Advanced Clock Schemes with Dead Time Techniques for High Voltage Charge Pumps

*Lufei Shen and Klaus Hofmann
TU Darmstadt*

TA1B.3 Power Aware Transformation of Bandlimited Signals

*Prakash Krishnamoorthy and Ramesh Tekumalla
LSI Corporation*

TA1B.4 Treat thy secondary (almost) like thy primary-a fair arbiter in master-slave configuration

*Ballori Banerjee and Jim Vomero
LSI Corporation*

Session TP1A - Reconfigurable and Programmable Circuits and Systems

Chair: Oliver Sander, Karlsruhe Institute of Technology

TP1A.1 A Wide Range Programmable Duty Cycle Corrector

*Ashok Jaiswal, Yuan Fang, Kashif Nawaz, Klaus Hofmann
TU Darmstadt*

TP1A.2 MORPACK CUBE: A portable 3D PORTABLE MORPACK heterogeneous system integration platform for Bluetooth application

*Chun-Chieh Chiu, Chih-Hsing Lin, Chih-Chyau Yang, Chih-Ting Kuo, Gang-Neng Sung,
Chun-Ming Huang, Chien-Ming Wu, National Chip Implementation Center*

TP1A.3 Real-Time efficient FPGA implementation of AES algorithm

*Mazen El Maraghy¹, Salma Hesham¹, Mohamed Abd El Ghany²
¹German University in Cairo, ²German University in Cairo and TU Darmstadt*

Session TP1B Network on Chip (NoC), Interconnects, and 3D-IC

Chair: Sao-Jie Chen, National Taiwan University

TP1B.1 Novel Time-Multiplexing Bidirectional On-chip Network

*Chun-Jen Wei¹, Yi-Yao Weng², Wen-Chung Tsai³, Sao-Jie Chen¹, Yu-Hen Hu⁴
¹Department of Electrical Engineering, National Taiwan University, ²Graduate Institute of Electronics Engineering, National Taiwan University, ³Information and Communications Research Lab., Industrial Technology Research Institute, ⁴Department of Electrical and Computer Engineering, University of Wisconsin, Madison*

TP1B.2 Coding Algorithms for Networks on Chip

*Ayman Salem¹, Mohamed Abd El Ghany¹, Klaus Hofmann²
¹German University in Cairo, TU Darmstadt, ²TU Darmstadt*

TP1B.3 High-Performance Adaption of ARM Processors into Network-on-Chip Architectures

*Xuan-Tu Tran, Tung Nguyen, Duy-Hieu Bui, Hai-Phong Phan, Trong-Trinh Nguyen
Vietnam National University, Hanoi*

Panel Discussion

**Chair: Andrew Marshall, University of Dallas at Texas
and
Yuejian Wu, Infinera**

What is the most important challenge in today's SOC design? B#

Session TPL2 - Plenary Session

Chair: Norbert Schuhmann, Fraunhofer IIS

Power-Centric Timing Optimization for Low Power CPU Hardening ***&-
Jon Young, Director Design Consulting, Synopsys Inc., UK**

Poster session and reception

Chair: Norbert Schuhmann, Fraunhofer IIS

CoChair: Kaijian Shi, Cadence Design Systems

**P1 Effective Signal Region based Analog Mixed Signal Design Considering Variations
and Applications *****& '**

*Janet Roveda¹, Dung Nguyen¹, Linda Powers¹, Kui Ren², Jerie Fairbanks¹
¹Univ. of Arizona, ¹State Univ. of New York*

P2 DLL-Based Programmable Clock Multiplier Using Differential Toggle-Pulsed Latch ***& -**

*Chorng-Sii Hwang¹, Ting-Li Chu¹, Po-Hsun Chen²
¹National Yunlin University of Science and Technology, ²Industrial Technology Research Institute*

P3 Design For Testability automation of mixed-signal integrated circuits ***& (**

*Sergey Mosin
Vladimir State University*

- P5 Scalable system map library for address map and data integrity verification** *****& \$
Prashanth Srinivasa
LSI Corporation India R&D Pvt Ltd
- P6 A novel approach to design a reversible shifter circuit using DNA** *****& *
Tanvir Ahmed and Hafiz Md Hasan Babu
University of Dhaka, Bangladesh
- P7 Sealed Mask ROM Wafer with 5 mm Magnetic Resonant Coupling for Long-term Digital Data Preservation** *****& &
Hiroyuki Ochi¹, Toshihiko Ota², Ataru Yamaoka², Hiromasa Watanabe², Yohei Kondo², Nobuyuki Tokuda², Hiroyuki Taguchi², Taketoshi Matsumoto³, Tomoki Akai³, Hikaru Kobayashi³, Shigeki Imai³
¹Ritsumeikan University, ²Sharp Takaya Electronic Industry Co., Ltd., ³Osaka University
- P8 Implementation and performance analysis of variable latency adders** *****&+
Ali Sayyed, Luciano Lavagno, Shah Khalid, Najeeb Ur Rahman
Electronics Department, Politecnico di Torino, Italy
- P9 Quotient Prediction for Low Power Division** *****&+
Prakash Krishnamoorthy and Ramesh Tekumalla
LSI Corporation
- P10 Sleep Transistor design in 28 nm CMOS Technology** *****&+,
Kaijian Shi
Cadence Design Systems
- P11 SOSoC, a Linux framework for System Optimization using System on Chip** *****& (,
Olivier Nasrallah, Wolfram Luithardt, Daniel Rossier, Alberto Dassatti, Jérôme Stadelmann, Xavier Blanc, Nuria Pazos Escudero, Florian Sauser, Serge Monnerat
University of Applied Science – Western Switzerland
- P12 An analytical, dynamic, power-performance router model for run-time NoC optimizations** *****&- \$
Davide Zoni, Federico Terraneo, William Fornaciari
Politecnico di Milano
- P13 Rapid Prototyping of a Portable HW/SW-Co-Design on the Virtual Zynq Platform using SystemC** *****&- *
Philipp Wehner, Max Ferger, Michael Hübner
Ruhr-Universität Bochum, Germany
- P14 A Generic, Scalable Reconfiguration Infrastructure for Sensor Networks Functionality Adaption** *****& \$%
Alexander Biedermann, Boris Dreyer, Sorin Huss
TU Darmstadt
- P15 A Formalism of the specifications for library development** *****& \$+
Jung Kyu CHAE¹, Roselyne CHOTIN-AVOT², Habib MEHREZ², Paul MOUGEAT¹, Jean-Arnaud FRANCOIS¹
¹STMicroelectronics, ²University of Marie Curie

Session FT1A - Embedded Tutorial

Chair: Yuejian Wu, Infinera

FT1A Macro-Modeling for Solving SOC Physical Design Automation Problems

*Prof. Dr. Roman Bazylevych, Lviv Polytechnic National University, Ukraine, and
Dr. Lubov Bazylevych, Ukrainian National Academy of Sciences*

Session FT1B - Embedded Tutorial

Chair: Andrew Marshall, University of Dallas at Texas

FT1B Digital Microfluidic Biochips: Towards Hardware/Software Co-Design and Cyberphysical System Integration

Prof. Dr. Tsung-Yi Ho, Dr. Juinn-Dar Huang and Dr. Paul Pop, National Cheng Kung University

Session FA1A - Green Circuits, Systems, and Design Methodologies

Chair: Thomas Büchner, IBM

FA1A.1 Low-power Signal Integrity Trainings For Multi-clock Source-Synchronous Memory System

*Yuan Fang, Ashok Jaiswal, Klaus Hofmann
TU Darmstadt*

FA1A.2 A Disturb-Free Subthreshold 9T SRAM Cell With Improved Performance and Variation Tolerance

*Chien-Yu Lu and Ching-Te Chuang
National Chiao Tung University*

Session FA1B - System Level Design Methodology and tools

Chair: Yuejian Wu, Infinera

FA1B.1 Equal Length Routing

*Gerard M Blair
LSI Corporation*

FA1B.2 Finding Ground Traces using the Laplacian of the Meshes of the Associated Graph

*Cristian Onete¹ and Maria-Cristina Onete²
¹NXP Semiconductors, ²TU Darmstadt*

Session FA2A - Green Circuits, Systems, Design Methodologies and Design Verification

Chair: Gururaj Shamanna, Intel Corporation

FA2A.1 Design Automation Flow for Voltage Adaptive Optimum Granularity LITHE for Sequential Circuits

*Venkat Krishnan Balasubramanian¹, Hao Xu², Ranga Vemuri³
¹Nvidia Corporation, ²Apache Design Solutions, ³University of Cincinnati*

FA2A.2 A Comprehensive Operand-Aware Dynamic Clock Gating Scheme for Low-Power Domino Logic

*Salim Farah and Magdy Bayoumi
University of Louisiana at Lafayette*

FA2A.3 Noise immunity improvement in the RESET signal of DDR3 SDRAM memory module

*Seung Mo Jung¹, Ho Jin Yoo², Do Hyung Kim², Woo Seop Kim², Joo Sun Choi², Jun Dong Cho³, Jong Hyun Seok², You Keun Han²
¹Sungkyunkwan university, ²Samsung Electronics, ³Sungkyunkwan university*

Session FA2B - Network on Chip (NoC), Interconnects, and 3D-IC

Chair: Danella Zhao, University of Louisiana at Lafayette

FA2B.1 A Robust Medium Access Mechanism for Millimeter-Wave Wireless Network-on-Chip Architectures

*Naseef Mansoor, Manoj Yuvaraj, Amlan Ganguly
Rochester Institute of Technology*

FA2B.2 Integrated Routing and Channel Arbitration in Overlaid Mesh WiNoC

*Ruizhe Wu and Dan Zhao
University of Louisiana at Lafayette*

FA2B.3 A Low Cost Method to Tolerate Soft Errors in the NoC Router Control Plane

*Changlin Chen and Sorin Cotofana
Delft University of Technology*