

2013 8th International Workshop on Reconfigurable and Communication-Centric Systems-on-Chip

(ReCoSoC 2013)

**Darmstadt, Germany
10 – 12 July 2013**



**IEEE Catalog Number: CFP1326P-POD
ISBN: 978-1-4799-4642-6**

TABLE OF CONTENTS

| | |
|---|------------|
| Dynamically Reconfigurable FIR Filter Architectures with Fast Reconfiguration | 1 |
| <i>Martin Kumm, Konrad Moller, Peter Zipf</i> | |
| An Efficient On-Chip Configuration Infrastructure for a Flexible Multi-ASIP Turbo Decoder Architecture | 9 |
| <i>Vianney Lapotre, Michael Hubner, Guy Gogniat, Purushotham Murugappa, Amer Baghdadi, Jean-Philippe Diguët</i> | |
| Simulation Framework for Cycle-Accurate RTL Modeling of Partial Run-Time Reconfiguration in VHDL | 17 |
| <i>Simen Gimle Hansen, Dirk Koch, Jim Torresen</i> | |
| CoEx: A Novel Profiling-Based Algorithm/Architecture Co-Exploration for ASIP Design | 25 |
| <i>Juan Fernando Eusse, Christopher Williams, Rainer Leupers</i> | |
| SoC Performance Evaluation with ArchC and TLM-2.0 | 33 |
| <i>Jorg Walter, Jorg Lenhardt, Wolfram Schiffmann</i> | |
| Register Allocation for High-Level Synthesis of Hardware Accelerators Targeting FPGAs | 41 |
| <i>Gerald Hempel, Jan Hoyer, Thilo Pionteck, Christian Hochberger</i> | |
| Centralized Traffic Monitoring for Online-Resizable Clusters in Networks-on-Chip | 47 |
| <i>Philipp Gorski, Dirk Timmermann</i> | |
| Improving Parallel MPSoC Simulation Performance by Exploiting Dynamic Routing Delay Prediction | 55 |
| <i>Christoph Roth, Harald Bucher, Simon Reder, Oliver Sander, Jurgen Becker</i> | |
| Measuring Memory Access Latency for Software Objects in a NUMA System-on-Chip Architecture | 63 |
| <i>Daniela Genius</i> | |
| Dynamic Task Remapping For Power and Latency Performance Improvement In Priority-Based Non-Preemptive Networks On Chip | 71 |
| <i>James Harbin, Leandro Soares Indrusiak</i> | |
| Among Slow Dwarfs and Fast Giants: A Systematic Design Space Exploration of KECCAK | 78 |
| <i>Bernhard Jungk, Marc Stottinger</i> | |
| A Programmable FPGA-Based Cryptoprocessor for Bilinear Pairings Over F2m | 86 |
| <i>Eduardo Cuevas-Farfan, Miguel Morales-Sandoval, Rene Cumplido, Claudia Feregrino-Uribe, Ignacio Algreto-Badillo</i> | |
| Exploiting FPGA Block Memories for Protected Cryptographic Implementations | 94 |
| <i>Shivam Bhasin, Wei He, Sylvain Guilley, Jean-Luc Danger</i> | |
| On a FPGA-based Method for Authentication Using Edwards Curves | 102 |
| <i>Andre Himmighofen, Bernhard Jungk, Steffen Reith</i> | |
| A New Model for Estimating Bit Error Probabilities of Ring-Oscillator PUFs | 109 |
| <i>Matthias Hiller, Georg Sigl, Michael Pehl</i> | |
| ACMA: Accuracy-Configurable Multiplier Architecture for Error-Resilient System-on-Chip | 117 |
| <i>Kartikeya Bhardwaj, Pravin S. Mane</i> | |
| Flexible, Ultra-Low Power Sensor Nodes Through Configurable Finite State Machines | 123 |
| <i>Juan Carlos Peña Ramos, Marian Verhelst</i> | |
| An FPGA Design and Implementation Framework Combined with Commercial VLSI CADs | 130 |
| <i>Qian Zhao, Motoki Amagasaki, Masahiro Iida, Morihiro Kuga, Toshinori Sueyoshi</i> | |
| A Framework for Effective Exploitation of Partial Reconfiguration in Dataflow Computing | 137 |
| <i>Riccardo Cattaneo, Xinyu Niu, Christian Pilato, Tobias Becker, Wayne Luk, Marco D. Santambrogio</i> | |
| The HeartBeat Model: A Platform Abstraction Enabling Fast Prototyping of Real-Time Applications on NoC-Based MPSoC on FPGA | 145 |
| <i>Francesco Robino, Johnny Oberg</i> | |
| Memory Allocation and Optimization in System-Level Architectural Synthesis | 153 |
| <i>Shuo Li, Ahmed Hemani</i> | |
| Hardware/Software Co-Compilation with the Nymble System | 160 |
| <i>Jens Huthmann, Bjorn Liebig, Julian Oppermann, Andreas Koch</i> | |
| Reconciling Application Power Control and Operating Systems for Optimal Power and Performance | 168 |
| <i>Dominic Hillenbrand, Yuuki Furuyama, Akihiro Hayashi, Hiroki Mikami, Keiji Kimura, Hironori Kasahara</i> | |
| Energy-Aware Dynamic Reconfiguration of Communication-Centric Applications for Reliable MPSoCs | 176 |
| <i>Anup Das, Amit Kumar Singh, Akash Kumar</i> | |
| Component Based Design using Constraint Programming for Module Placement on FPGAs | 183 |
| <i>Alexander Wold, Dirk Koch, Jim Torresen</i> | |

| | |
|--|-----|
| An Exploration of Heterogeneous Systems | 191 |
| <i>Jesús Carabaño, Francisco Dios, Masoud Daneshlab, Masoumeh Ebrahimi</i> | |
| Addigation: Exploring Configuration Behavior of Spartan-3 Devices | 198 |
| <i>Michael Dreschmann, Oliver Sander, Alexander Klimm, Christoph Roth, Juergen Becker</i> | |
| Bitfile Preservation - Generation Of Reusable Out Of Context Modules | 204 |
| <i>Christian Stullein, Norbert Abel, Udo Keschull</i> | |
| Approximation of Hyperbolic Tangent Activation Function Using Hybrid Methods | 210 |
| <i>Maicon A. Sartin, Alexandre C. R. Da Silva</i> | |
| A Parallelization Methodology for Reconfigurable Systems Applied to Edge Detection | 216 |
| <i>Juan M. Campos, Rene Cumplido, Claudia Feregrino-Urbe, Roberto Perez-Andrade</i> | |
| RecMIN: a Reconfiguration Architecture for Network on Chip | 223 |
| <i>Alexander Logvinenko, Carsten Gremzow, Dietmar Tutsch</i> | |
| Towards a Configurable Many-Core Accelerator for FPGA-based Embedded Systems | 229 |
| <i>Marco Ramirez, Masoud Daneshlab, Pasi Liljeberg, Juha Plosila</i> | |
| Shared Hardware Accelerator Architectures for Heterogeneous MPSoCs | 233 |
| <i>Damak Bouthaina, Mouna Baklouti, Smail Niar, Mohamed Abid</i> | |
| D-RECS: A Complete Methodology to Implement Self Dynamic Reconfigurable FPGA-Based Systems | 239 |
| <i>F. Cancare, C. Pilato, A. Cazzaniga, D. Sciuto, Marco D. Santambrogio</i> | |
| Practical Measurements of Data Path Delays for IP Authentication & Integrity Verification | 245 |
| <i>Ingrid Exurville, Jacques Fournier, Jean-Max Dutertre, Bruno Robisson, Assia Tria</i> | |
| Author Index | |