

2014 IEEE COOL Chips XVII

**Yokohama, Japan
14 – 16 April 2014**



**IEEE Catalog Number: CFP14COL-POD
ISBN: 978-1-4799-3811-7**

TABLE OF CONTENTS

SESSION VI: MULTI/MANY CORE

Establishing A Standard Interface Between Multi-Manycore And Software Tools – SHIM	1
<i>M. Gondo, F. Arakawa, M. Edahiro</i>	
Parallel Design of Control Systems Utilizing Dead Time for Embedded Multicore Processors	4
<i>Y. Suzuki, K. Sata, J. Kako, K. Yamaguchi, F. Arakawa, M. Edahiro</i>	

SESSION VII: PANEL DISCUSSIONS

Toward Wearable Computing Era, How COOL Chip Architecture and Tools will Evolve?	7
<i>M. McCool, S. Ryu, S. Kawasaki, H. Tobia, F. Arakawa</i>	

SESSION IX: MEMORIES

Language Runtime Support for NVM/DRAM Hybrid Main Memory	9
<i>G. Nakagawa, S. Oikawa</i>	
A Low Power DRAM Refresh Control Scheme for 3D Memory Cube	12
<i>Y. Wang, Y. Han, H. Li</i>	
A Flexibly Fault-Tolerant FU Array Processor and its Self-Tuning Scheme to Locate Permanently Defective Unit	15
<i>J. Yao, Y. Nakashima, M. Saito, Y. Hazama, R. Yamanaka</i>	
A Globally Asynchronous Locally Synchronous DMR Architecture for Aggressive Low-Power Fault Toleration	18
<i>Y. Yuttakonki, J. Yao, Y. Nakashima</i>	
Kernel Data Race Detection using Debug Register in Linux	21
<i>Y. Jiang, Y. Yang, T. Xiao, T. Sheng, W. Chen</i>	

SESSION XII: LOW-POWER CIRCUIT TECHNIQUES

A Perpetuum Mobile 32bit CPU with 13.4pJ/cycle, 0.14μA Sleep Current using Reverse Body Bias Assisted 65nm SOTB CMOS Technology	24
<i>K. Ishibashi, N. Sugii, K. Usami, H. Amano, K. Kobayashi, C. Pham, H. Makiyama, Y. Yamamoto, H. Shinohara, T. Iwamatsu, Y. Yamaguchi, H. Oda, T. Hasegawa, S. Okanishi, H. Yanagita, S. Kamohara, M. Kadoshima, K. Maekawa, T. Yamashita, D. Le, T. Yomogita, M. Kudo, K. Kitamori, S. Kondo, Y. Manzawa</i>	
Embedded SRAM and Cortex-M0 Core with Backup Circuits Using a 60-nm Crystalline Oxide Semiconductor for Power Gating	27
<i>H. Tamura, K. Kato, T. Ishizu, T. Onuki, W. Uesugi, T. Ohmaru, K. Ohshima, H. Kobayashi, S. Yoneda, A. Isobe, N. Tsutsui, S. Hondo, Y. Suzuki, Y. Okazaki, T. Atsumi, Y. Shionoiri, Y. Maehashi, G. Goto, M. Fujita, J. Myers, P. Korpinen, J. Koyama, Y. Yamamoto, S. Yamazaki</i>	

SESSION XIII: POWER OPTIMIZATION

Aggressive Use of Deep Sleep Mode in Low Power Embedded Systems	30
<i>J. Segawa, Y. Shirota, K. Fujisaki, T. Kimura, T. Kanai</i>	
An Energy Optimization Method for Vector Processing Mechanisms	33
<i>Y. Gao, M. Sato, R. Egawa, H. Takizawa, H. Kobayashi</i>	
A Fine Grained Power Management supported by Just-In-Time Compiler	36
<i>M. Wada, M. Sato, M. Namiki</i>	

SESSION XIV: NOV

A Task-level Pipelined Many-SIMD Augmented Reality Processor with Congestion-aware Network-on-Chip Scheduler 39
G. Kim, S. Park, K. Lee, Y. Kim, I. Hong, K. Bong, D. Shin, S. Choi, J. Park, H. Yoo

A Low Power Noc Router Using The Marching Memory Through Type..... 42
R. Yasudo, T. Kagami, H. Amano, Y. Nakase, M. Watanebe, T. Oishi, T. Shimizu, T. Nakamura

Author Index