

2014 15th Latin American Test Workshop

(LATW 2014)

**Fortaleza, Brazil
12-15 March 2014**



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15th IEEE Latin-American Test Workshop

TECHNICAL PROGRAM

Wednesday, 12th March 2014

08:00 - 08:30 Registration

08:30 - 09:00 **Opening Session**

General Chairs: Fabian VARGAS - Catholic University of Rio Grande do Sul (PUCRS), Brazil,
Yervant ZORIAN - Synopsys, USA

Program Chairs: Leticia BOLZANI PÖHLS - Catholic University of Rio Grande do Sul (PUCRS),
Brazil, Vishwani AGRAWAL - Auburn University, USA

Local Chair: Helano CASTRO - Federal University of Ceará (UFC), Brazil

09:00 - 09:40 **TTEP Tutorial**

Title: Hierarchical Test: Trends, Challenges, Solutions

Presenter: Yervant ZORIAN - Synopsys, USA

Chair: Fabian VARGAS - Catholic University of Rio Grande do Sul (PUCRS), Brazil

09:40 - 10:40 **SESSION 01: FAULT TOLERANT ARCHITECTURES**

Session Chair: Raoul VELAZCO - TIMA, France

**DESIGN DIVERSITY REDUNDANCY WITH SPATIAL-TEMPORAL VOTING
APPLIED TO DATA ACQUISITION SYSTEMS**

Cristiano CHENET, Alisson LANOT, Tiago BALEN
Federal University of Rio Grande do Sul (UFRGS), Brazil

IMPROVING THE ROBUSTNESS OF A SWITCH BOX IN A MESH OF CLUSTERS FPGA

Arwa BEN DHIA, Mariem SLIMANI, Lirida NAVINER
Institut TELECOM, TELECOM ParisTech, LTCI-CNRS, France

FAULT TOLERANCE EVALUATION OF RFID TAGS

Omar ABDELMALEK, David HELY, Vincent BEROULLE
LCIS, Grenoble Institute of Technology, France

10:40 - 11:10 **COFFEE BREAK**

CEITEC Master's Thesis Award – Poster Evaluation Session

11:10 - 12:30 **SESSION 02: DESIGN VERIFICATION AND VALIDATION**

Session Chair: Vishwani AGRAWAL - Auburn University, USA

ON THE REUSE OF RTL ASSERTIONS IN SYSTEMC TLM VERIFICATION

Nicola BOMBIERI* **, Franco FUMMI* **, Valerio GUARNIERI*, Graziano PRAVADELLI* **,
Francesco STEFANNI*, Tara GHASEMPOURI**, Michele LORA**, Giovanni AUDITORE***,
Mirella NEGRO MARCIGAGLIA***

*EDALab s.r.l., Italy **University of Verona, Italy ***STMicroelectronics s.r.l., Italy

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SIMPLIFIED STIMULI GENERATION FOR SCENARIO AND ASSERTION BASED VERIFICATION

Graziano PRAVADELLI, Luca PICCOLBONI
University of Verona, Italy

A UNIFIED SEQUENTIAL EQUIVALENCE CHECKING APPROACH TO VERIFY HIGH-LEVEL FUNCTIONALITY AND PROTOCOL SPECIFICATION IMPLEMENTATIONS IN RTL DESIGNS

Carlos Ivan CASTRO MARQUEZ, Marius STRUM, Wang CHAU
University of São Paulo, Brazil

OPTIMIZED HYBRID VERIFICATION OF EMBEDDED SOFTWARE

Joerg BEHREND*, Alexander GRUENHAGE*, Douglas SCHROEDER**, Djones LETTNIN**, Juergen RUF*, Thomas KROPF*, Wolfgang ROSENSTIEL*
* University of Tübingen, Germany **Federal University of Santa Catarina (UFSC), Brazil

12:30 - 14:00 LUNCH

14:00 - 14:40 INVITED TALK 01

Title: IC Reliable and Quality Challenges and Forthcomming Technology Nodes
Presenter: Said HAMDIOUI - Delft University of Technology, Netherlands
Chair: Jaan RAIK - Tallinn University of Technology, Estonia

14:40 - 16:00 SESSION 03: FAULT MODELING AND SIMULATION

Session Chair: Djones LETTNIN - Federal University of Santa Catarina (UFSC), Brazil

SEU FAULT-INJECTION AT SYSTEM LEVEL: METHOD, TOOLS AND PRELIMINARY RESULTS

Wassim MANSOUR*, Pablo RAMOS*, Rafic AYOUBI**, Raoul VELAZCO*
*TIMA, INPG, France **University of Balamand, Lebanon

ANALYSIS OF THE EFFECTS OF SINGLE EVENT TRANSIENTS ON AN SAR-ADC BASED ON CHARGE REDISTRIBUTION

Alisson LANOT, Tiago BALEN
Federal University of Rio Grande do Sul (UFRGS), Brazil

POSSIBILITIES OF DEFECT-SIZE MAGNIFICATION FOR TESTING RESISTIVE-OPENS IN NANOMETER TECHNOLOGIES

Jose GARCIA-GERVACIO*, Jaime MARTINEZ*, Victor CHAMPAC*
*University of Veracruz, Mexico **INAOE, Mexico

SOFT ERROR INJECTION METHODOLOGY BASED ON QEMU SOFTWARE PLATFORM

Filipe GEISSLER, Fernanda KASTENSMIDT
Federal University of Rio Grande do Sul (UFRGS), Brazil

TECHNICAL PROGRAM

Wednesday, 12th March 2014

16:00 - 16:30 **COFFEE BREAK**

CEITEC Master's Thesis Award – Poster Evaluation Session

16:30 - 17:30 **SESSION 04: SYSTEM RELIABILITY**

Session Chair: Leticia BOLZANI PÖHLS - Catholic University of Rio Grande do Sul (PUCRS), Brazil

A NOVEL CONTROL STRATEGY FOR FAIL-SAFE CYCLIC DATA EXCHANGE IN WIRELESS SENSOR NETWORKS

Pablo BRIFF*, Ariel LUTENBERG*, Leonardo REY VEGA*, Fabian VARGAS**, Mohammad PATWARY*

*Universidad de Buenos Aires, Argentina **Catholic University of Rio Grande do Sul (PUCRS), Brazil

LOW COST FAULT DETECTOR GUIDED BY PERMANENT FAULTS AT THE END OF FPGA LIFE CYCLE

Victor MARTINS, Frederico FERLINI, Djones LETTNIN, Eduardo BEZERRA
Federal University of Santa Catarina (UFSC), Brazil

IMPLEMENTATION AND EXPERIMENTAL EVALUATION OF A CUDA CORE UNDER SINGLE EVENT EFFECTS

Jose Rodrigo AZAMBUJA*, Werner NEDEL**, Fernanda KASTENSMIDT**

*Federal University of Rio Grande (FURG) **Federal University of Rio Grande do Sul (UFRGS), Brazil

17:30 - 18:30 **SESSION 05: FAULT TOLERANCE IN HARDWARE AND SOFTWARE**

Session Chair: Célia LÓPEZ-ONGIL - Carlos III University of Madrid, Spain

FAULT TOLERANT LINEAR STATE MACHINES

Stefan WEIDLING, Michael GOESSEL
University of Potsdam, Germany

IDSM: AN IMPROVED DISJOINT SIGNATURE MONITORING SCHEME FOR PROCESSOR BEHAVIORAL CHECKING

Salma BERGAOUI, Pierre VANHAUWAERT, Regis LEVEUGLE
CNRS, TIMA Laboratory, France

METHODOLOGY FOR ACHIEVING BEST TRADE-OFF OF AREA AND FAULT MASKING COVERAGE IN ATMR

Iuri GOMES*, Mayler MARTINS*, Fernanda KASTENSMIDT*, André REIS*, Sylvain NOVALÈS**

*Federal University of Rio Grande do Sul (UFRGS), Brazil **ENSEIRB-MATMECA, France

20:30

WELCOME COCKTAIL

CEITEC Master's Thesis Award – Ceremony

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Thursday, 13th March 2014

09:00 - 09:40 KEYNOTE TALK

Presenter: Jacob ABRAHAM - University of Texas, USA
Chair: Yervant ZORIAN - Synopsys, USA

09:40 - 10:40 TTTC Ph.D. THESIS AWARD

Oral Presentation Session

10:40 - 11:10 COFFEE BREAK

11:10 - 12:10 SPECIAL SESSION

Title: Analog Mixed Signal Test

Organizer: Florence AZAIS - LIRMM, France

Session Chair: Victor CHAMPAC - INAOE, Mexico

SPECIFICATION TEST MINIMIZATION FOR GIVEN DEFECT LEVEL

Suraj SINDIA, Vishwani AGRAWAL
Auburn University, USA

HARMONIC DISTORTION CORRECTION FOR 8-BIT DELAY LINE ADC USING GRAY CODE

Hsun-Cheng LEE, Jacob ABRAHAM
University of Texas, USA

**DEVELOPMENT OF A DIGITAL TOOL FOR THE SIMULATION OF A READOUT SYSTEM
DEDICATED FOR NEUTRON DISCRIMINATION**

Sabrine BEN KRIT*, Wenceslas RAHAJANDRAIBE*, Karine COULIÉ-CASTELLANI*, Gilles
MICOLAU**, A. LEVISSE*, A. LYOUSSI***

*IM2NP-UMR CNRS / Aix-Marseille University, France **UMR 1114 EMMAH (INRA-UAPV) /
Université d'Avignon, France ***CEA/DEN/DER/SPEX, France

12:10 - 13:30 LUNCH

13:30 - 14:00 SESSION 06: PROJECT IN PROGRESS

Session Chair: Helano CASTRO - Federal University of Ceará (UFC), Brazil

THE IEEE STD 1149.6-2003 OVERVIEW

Francisco RUSSI
Synopsys, USA

14:45 SOCIAL EVENT

Boat Trip

19:30 SOCIAL EVENT

Gala Dinner

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09:00 - 10:20 SESSION 07: RADIATION AND ELECTROMAGNETIC INTERFERENCE

Session Chair: José LIPOVETZKY - UBA, Argentina

IMPROVEMENT OF A VCO CONCEPT FOR LOW ENERGY PARTICULE DETECTION AND RECOGNITION

Karine COULIE-CASTELLANI*, Wenceslas RAHAJANDRAIBE*, Gilles MICOLAU**, Hassen AZIZA*, Jean Michel PORTAL*

*IM2NP-UMR CNRS / Aix-Marseille University, France **UMR 1114 EMMAH (INRA-UAPV) / Université d'Avignon, France

THE EFFECTS OF TOTAL IONIZING DOSE ON THE NEUTRON SEU CROSS SECTION OF A 130 NM 4 MB SRAM MEMORY

Odair GONCALEZ*, Evaldo C. F. PEREIRA JUNIOR*, Rafael VAZ*, Claudio FEDERICO*, Gilson WIRTH**, Thiago BOTH**

* Instituto de Estudos Avançados São José dos Campos, Brazil **Federal University of Rio Grande do Sul (UFRGS), Brazil

SOFT ERROR RATE IN SRAM-BASED FPGAS UNDER NEUTRON-INDUCED AND TID EFFECTS

Lucas TAMBARA*, Jorge TONFAT*, Ricardo REIS*, Fernanda KASTENSMIDT*, Evaldo C. F. PEREIRA JUNIOR**, Rafael VAZ**, Odair GONCALEZ**

*Federal University of Rio Grande do Sul (UFRGS), Brazil ** Instituto de Estudos Avançados São José dos Campos, Brazil

PERFORMANCE ANALYSIS OF A CLOCK GENERATOR PLL UNDER TID EFFECTS

Alan ROSSETTO, Gilson WIRTH, Ricardo DALLASEN

Federal University of Rio Grande do Sul (UFRGS), Brazil

10:20 - 10:50 COFFEE BREAK

10:50 - 11:30 INVITED TALK 02

Title: Design of On-Chip Sensors to Monitor Electromagnetic Activity in ICs: Towards Online Diagnosis and Self-Healing

Presenter: Sonia BEN DHIA - LAAS/INSA, Toulouse, France

Chair: Maksim JENIHHIN -Tallinn University of Technology, Estonia

11:30 - 12:30 PANEL 01

Title: Regaining Hardware Trust: Security Challenges during Reliable System Design

Organizers: Vishwani AGRAWAL - Auburn University, USA and Fabian VARGAS - Catholic University of Rio Grande do Sul (PUCRS), Brazil

Panelists: David HELY, Jennifer DWORAK, Ozgur SINANOGLU, Ramesh KARRI

12:30 - 14:00 LUNCH

TECHNICAL PROGRAM

Friday, 14th March 2014

14:00 - 15:00 **PANEL 02**

Title: Radiation Facilities in South America and Expected Reliability for Space Applications

Organizers: Raoul VELAZCO - TIMA, France and Fernanda KASTENSMIDT - Federal University of Rio Grande do Sul, Brazil

Panelists: Oliver SANDER, Claudio FEDERICO, Nilberto MEDINA, José LIPOVETZKY, Pablo FERREYRA, Juan FRAIRE

15:00 - 15:40 **INVITED TALK 03**

Recent Progress of Software-Related Electromagnetic Interference

Presenter: Shih-Yi YUAN - Feng Chia University, Taiwan

Chair: Ozgur SINANOGLU - New York University Abu Dhabi, United Emirates

15:40 - 16:10 **COFFEE BREAK**

16:10 - 16:50 **SESSION 08: SOFTWARE FAULT-TOLERANCE AND TESTING**

Session Chair: Francisco RUSSI - Synopsys, USA

EFFICIENT METRIC FOR REGISTER FILE CRITICALITY IN PROCESSOR-BASED SYSTEMS

Felipe RESTREPO-CALLE*, Sergio CUENCA-ASENSI*, Antonio MARTÍNEZ-ÁLVAREZ*, Eduardo CHIELLE**, Fernanda KASTENSMIDT**

*University of Alicante, Spain **Federal University of Rio Grande do Sul (UFRGS), Brazil

SOFTWARE-BASED SELF-TEST GENERATION FOR MICROPROCESSORS WITH HIGH-LEVEL DECISION DIAGRAMS

Raimund UBAR, Anton TSERTOV, Artjom JASNETSKI, Marina BRIK
Tallinn University of Technology, Estonia

16:50 - 17:50 **SESSION 09: HARDENING TECHNIQUES**

Session Chair: Jacob ABRAHAM - University of Texas, USA

REDUCING SEU SENSITIVITY IN LIN NETWORKS: SELECTIVE AND COLLABORATIVE HARDENING TECHNIQUES

Anna VASKOVA*, Fabregat AROA*, Marta PORTELA-GARCIA*, Mario GARCIA-VALDERAS*, Celia LÓPEZ-ONGIL*, Matteo SONZA REORDA**

*Carlos III University of Madrid, Spain **Politecnico di Torino, Italy

SCHMITT TRIGGER ON OUTPUT INVERTERS OF NCL GATES FOR SOFT ERROR HARDENING: IS IT ENOUGH?

Matheus MOREIRA, Ricardo GUAZZELLI, Ney CALAZANS
Catholic University of Rio Grande do Sul (PUCRS), Brazil

HIERARCHICAL IDENTIFICATION OF NBTI-CRITICAL GATES IN NANOSCALE LOGIC

Jaan RAIK*, Sergei KOSTIN*, Maksim JENIHHIN*, Raimund UBAR*, Fabian VARGAS**, Letícia BOLZANI PÖHLS**, Thiago COPETTI**

* Tallinn University of Technology, Estonia ** Catholic University of Rio Grande do Sul (PUCRS), Brazil

17:50 - 18:40 **CLOSING REMARKS**