

2014 IEEE 44th International Symposium on Multiple-Valued Logic

(ISMVL 2014)

**Bremen, Germany
19-21 May 2014**



**IEEE Catalog Number: CFP14034-POD
ISBN: 978-1-4799-3536-9**

2014 IEEE 44th International Symposium on Multiple-Valued Logic

ISMVL 2014

Table of Contents

Message from the Symposium Chair.....	ix
Message from the Program Chair.....	x
Committee Members.....	xi
Additional Reviewers.....	xii

Logic Design and Switching Functions

An Update Method for a CAM Emulator Using an LUT Cascade Based on an EVMDD (K)	1
<i>Hiroki Nakahara, Tsutomu Sasao, and Munehiro Matsuura</i>	
A Lower Bound on the Number of Variables to Represent Incompletely Specified Index Generation Functions	7
<i>Tsutomu Sasao, Yuta Urano, and Yukihiko Iguchi</i>	
On the Number of S-Threshold Functions on Not Necessarily Binary Input	13
<i>Jovanka Pantović, Silvia Ghilezan, and Joviša Žunić</i>	
The Maiorana Method to Generate Multiple-Valued Bent Functions Revisited	19
<i>C. Moraga, M. Stanković, R. Stanković, and S. Stojković</i>	

Problem Solvers and Fuzzy Logic

Multiple-Valued Problem Solvers—Comparison of Several Approaches	25
<i>Bernd Steinbach and Christian Posthoff</i>	
Many-Valued MinSAT Solving	32
<i>Josep Argelich, Chu Min Li, Felip Manyà, and Zhu Zhu</i>	
Semantic Games with Backtracking for Fuzzy Logics	38
<i>Christian G. Fermüller</i>	
Neural Spike Compression Using Feature Extraction and a Fuzzy C-Means Codebook	44
<i>Russell Dodd, Bruce F. Cockburn, and Vincent Gaudet</i>	

Algebra and Logic I

Concrete Dualities and Essential Arities	49
<i>Sebastian Kerkhoff</i>	
Maximal and Minimal Closed Classes in Multiple-Valued Logic	55
<i>Tamás Waldhauser</i>	
On Key Relations Preserved by a Weak Near-Unanimity Function	61
<i>Dmitriy Zhuk</i>	

Hardware Improvement and Exploitation

Design of a Quaternary Single-Ended Current-Mode Circuit for an Energy-Efficient Inter-chip Asynchronous Communication Link	67
<i>Akira Mochizuki, Hirokatsu Shirahama, and Takahiro Hanyu</i>	
Non-binary Successive Approximation Analog-to-Digital Converters: A Survey	73
<i>Takao Waho</i>	
Constant Geometry Algorithms for Galois Field Expressions and Their Implementation on GPUs	79
<i>Radomir S. Stanković, Jaakko Astola, Claudio Moraga, and Dušan Gajić</i>	

Investigations on Types of Clones

Polynomially Closed Co-clones	85
<i>Victor Lagerkvist and Magnus Wahlström</i>	
Partial R-Clones	91
<i>Boris A. Romov and Karsten Schölzel</i>	
Essentially Minimal Clones of Rank 3 on a Three-Element Set	97
<i>Hajime Machida and Ivo G. Rosenberg</i>	

Synthesis and Fault Analysis for Reversible Circuits

Efficient Reversible Logic Synthesis via Isomorphic Subgraph Matching	103
<i>Mridul Krishna and Anupam Chattopadhyay</i>	
A Cube Pairing Approach for Synthesis of ESOP-Based Reversible Circuit	109
<i>Chandan Bandyopadhyay, Hafizur Rahaman, and Rolf Drechsler</i>	
Analysis of Faults in Reversible Computing	115
<i>Martin Lukac, Michitaka Kameyama, Marek Perkowski, Pawel Kerntopf, and Claudio Moraga</i>	

Algebra and Logic II

Lukasiewicz Negation and Many-Valued Extensions of Constructive Logics	121
<i>Thomas Macaulay Ferguson</i>	
Four New Construction Methods on Residuated Monoids	128
<i>Sándor Jenei</i>	

First-Order Logic Based on Set Approximation: A Partial Three-Valued Approach	132
<i>Tamás Mihálydeák</i>	

Coding

Evaluation of High-Speed Interfaces for VLSI Systems Using Tomlinson-Harashima Precoding	138
<i>Yosuke Iijima and Yasushi Yuminaka</i>	
An Efficient Approach to Verifying Galois-Field Arithmetic Circuits of Higher Degrees and Its Application to ECC Decoders	144
<i>Rei Ueno, Kotaro Okamoto, Naofumi Hommam, and Takafumi Aoki</i>	
Comparison of Spectrally Efficient Coding Techniques for High-Speed Serial Links	150
<i>Yasushi Yuminaka, Yuki Takada, Tomonao Okada, and Yosuke Iijima</i>	

Investigations on Properties of Clones

Countable Intervals of Partial Clones	155
<i>Lucien Haddad and Karsten Schölzel</i>	
Relation Graphs and Partial Clones on a 2-Element Set	161
<i>Miguel Couceiro, Lucien Haddad, Karsten Schölzel, and Tamás Waldhauser</i>	
Minimal Cut Vectors and Logical Differential Calculus	167
<i>Miroslav Kvassay, Elena Zaitseva, Vitaly Levashenko, and Jozef Kostolny</i>	

Advances for Quantum Computation

The Decomposition of $U(n)$ into $XU(n)$ and $ZU(n)$	173
<i>Alexis De Vos and Stijn De Baerdemacker</i>	
On Some Basic Aspects of Ternary Reversible and Quantum Computing	178
<i>Claudio Moraga</i>	
Synthesis of Ternary Grover's Algorithm	184
<i>Sudhindu Bikash Mandal, Amlan Chakrabarti, and Susmita Sur-Kolay</i>	

Decision Diagrams and Other Function Representations

Analysis Methods of Multi-state Systems Partially Having Dependent Components Using Multiple-Valued Decision Diagrams	190
<i>Shinobu Nagayama, Tsutomu Sasao, Jon T. Butler, Mitchell A. Thornton, and Theodore W. Manikas</i>	
System Probability Distribution Modeling Using MDDs	196
<i>M.A. Thornton, T.W. Manikas, S.A. Szygenda, and Shinobu Nagayama</i>	
On Submodular and Supermodular Functions on Lattices and Related Structures	202
<i>Dan A. Simovici</i>	

Design and Evaluation of Memories

Associative Memories Based on Multiple-Valued Sparse Clustered Networks	208
<i>Hooman Jarollahi, Naoya Onizawa, Takahiro Hanyu, and Warren J. Gross</i>	
Design of a Logic-in-Memory Multiple-Valued Reconfigurable VLSI Based on a Bit-Serial Packet Data Transfer Scheme	214
<i>Shintaro Harada, Xu Bai, Michitaka Kameyama, and Yoshichika Fujioka</i>	
Soft-Delay-Error Evaluation in Content-Addressable Memory	220
<i>Naoya Onizawa, Shoun Matsunaga, Noboru Sakimura, Ryusuke Nebashi, Tadahiko Sugibayashi, and Takahiro Hanyu</i>	

Algebra and Logic III

Online Monitoring of Distributed Systems with a Five-Valued LTL	226
<i>Ming Chai and Bernd-Holger Schlingloff</i>	
Ternary Parametron Based on Subharmonic Oscillation of Order Three by Forcing	232
<i>Takako Soma and Takashi Soma</i>	
Inadmissible Class of Boolean Functions under Stuck-at Faults	237
<i>Debesh K. Das, Debabani Chowdhury, Bhargab B. Bhattacharya, and Tsutomu Sasao</i>	

Hardware Components

Variation-Effect Analysis of MTJ-Based Multiple-Valued Programmable Resistors	243
<i>Masanori Natsui and Takahiro Hanyu</i>	
Differential-Time and Pulse-Amplitude Modulation Signaling for Serial Link Transceivers	248
<i>Mostafa Rashdan and James W. Haslett</i>	
An Algorithm for Constructing a Minimal Register with Non-linear Update Generating a Given Sequence	254
<i>Nan Li and Elena Dubrova</i>	
Author Index	260