

2014 IEEE 17th International Symposium on Design and Diagnostics of Electronic Circuits & Systems

(DDECS 2014)

**Warsaw, Poland
23 – 25 April 2014**



IEEE Catalog Number: CFP14DDE-POD
ISBN: 978-1-4799-4557-3

Table of Contents

Keynote Talks

- Detection & Diagnostics in Today's Advanced Technology Nodes 9
Yervant Zorian
- Automatic Architecture Exploration of Massively Parallel MPSoCs for Modern Cyber-physical Systems 10
Lech Józwiak
- Design and Testing of Integrated Circuit of Pixel Architecture for Fast X-ray Imaging Applications 11
Paweł Gryboś, Piotr Kmon, Piotr Maj, Robert Szczygiel

Embedded Tutorials

- SiP Design Flow and 3D DRC for MEMS 12
A. Mehdaoui, J. Pagazani, G. Schröpfer, G. Lissorgues
- Development of 3D Space Partitioning and Design Rule Check for Smart System Solutions 14
Stefano Pettazzi, Andrew Plews, Anatoly Rudenko, Ahmed Nejim

Session 1A: Advanced Systems

- Studying DAC Capacitor-Array Degradation in Charge-Redistribution SAR ADCs 15
Muhammad Aamir Khan, Hans G. Kerkhoff
- Automatically Connecting Hardware Blocks via Light-Weight Matching Techniques 21
Jan Malburg, Niklas Krafczyk, Görschwin Fey
- A Double-Path Intra Prediction Architecture for the Hardware H.265/HEVC Encoder 27
Andrzej Abramowski, Grzegorz Pastuszek

Session 1B: Built-In Self-Test

- Online Test Vector Insertion: A Concurrent Built-In Self-Testing (CBIST) Approach for Asynchronous Logic 33
Jürgen Maier, Andreas Steininger
- Quality Assurance in Memory Built-In Self-Test Tools 39
Albert Au, Artur Pogiel, Janusz Rajski, Piotr Sydow, Jerzy Tyszer, Justyna Zawada
- Generic Built-in Self-Repair Architectures for SoC Logic Cores 45
Marcel Balaz, Stefan Kristofik, Maria Fischerova

Session 2A: RF Design

- A 64-MHz~640-MHz 64-Phase Clock Generator 51
Hong-Yi Huang, Jen-Chieh Liu, Shi-Jia Sun and Cheng-Hao Fu, Kuo-Hsing Cheng
- A Design of an Area-Efficient 10-GHz Phase-Locked Loop for Source-Synchronous, Multi-Channel Links in 90-nm CMOS Technology 55
Woorham Bae and Deog-Kyoon Jeong, Byoung-Joo Yoo
- Burst-Pulse Generator Based on Transmission Line Toward Sub-MMW 59
Parit Kanjanavirojkul, Nguyen Ngoc Mai Khanh, Toru Nakura and Kunihiro Asada
- A 120V High Voltage DAC Array for A Tunable Antenna in Communication System 65
Jing Ning, Klaus Hofmann

Session 2B: RTL & High Level Design

- Fast Time-Parallel C-based Event-Driven RTL Simulation 71
Tariq Bashir Ahmad, Maciej Ciesielski

Lower Bounds of the Size of Shared Structurally Synthesized BDDs <i>Raimund Ubar, Dmitri Mironov</i>	77
BuildMaster: Efficient ASIP Architecture Exploration Through Compilation and Simulation Result Caching <i>Roel Jordans, Erkan Diken, Lech Jóźwiak, Henk Corporaal</i>	83
Session 3A: Analog IC Design & Simulation	
Analysis of Current Conveyor Non-Idealities for Implementation as Integrator in Delta Sigma Modulators <i>Harish Balasubramaniam, Klaus Hofmann</i>	89
Multistage Low Ripple Charge Pump <i>Andrzej Grodzicki and Witold Pleskacz</i>	93
A Novel Impedance Calculation Method and its Time Efficiency Evaluation <i>Juraj Brenkuš, Viera Stopjaková, Daniel Arbet, Gábor Gyepes and Libor Majer</i>	99
Session 3B: Compression & ATPG	
Test-Data Compression with Low Number of Channels and Short Test Time <i>Ondřej Novák, Jiří Jeníček, Martin Rozkovec</i>	104
Test Data Compression based on Reuse and Bit-Flipping of Parts of Dictionary Entries <i>Panagiotis Sismanoglou, Dimitris Nikolos</i>	110
Timing-aware ATPG for Critical Paths with Multiple TSVs <i>C. Metzler, A. Todri-Sanial, A. Bosio, L. Dilillo, P. Girard, A. Virazel</i>	116
Session 4A: Emerging Technologies	
A Layout Based Customized Testing Technique for Total Microfluidic Operations in Digital Microfluidic Biochips <i>Pranab Roy, Hafizur Rahaman, Parthasarathi Dasgupta</i>	122
Optimizing DD-based Synthesis of Reversible Circuits using Negative Control Lines <i>Eleonora Schönborn, Kamalika Datta, Robert Wille, Indranil Sengupta, Hafizur Rahaman, Rolf Drechsler</i>	129
Evolutionary Design of Approximate Multipliers Under Different Error Metrics <i>Zdenek Vasicek and Lukas Sekanina</i>	135
Session 4B: On-line Test & Fault Tolerance	
Online Testing of Many-Core Systems in the Dark Silicon Era <i>Mohammad-Hashem Haghbayan, Amir-Mohammad Rahmani, Pasi Liljeberg, Juha Plosila, Hannu Tenhunen</i>	141
Reliable Execution of Statechart-Generated Correct Embedded Software under Soft Errors <i>Ronaldo R. Ferreira, Thomas Klotz, Thilo Vörtler, Jean da Rolt, Gabriel L. Nazar, Álvaro F. Moreira, Luigi Carro, Karsten Einwich</i>	147
Combining Fault Tolerance and Self Repair at Minimum Cost in Power and Hardware <i>Tobias Koal, Mario Schölzel, Heinrich T. Vierhaus</i>	153
Session 5A (Student Session): Analog & Architecture	
Self-Managing Power Management Unit <i>Dominik Macko, Katarína Jelemenská</i>	159
A Low Supply Voltage Synchronous Mirror Delay with Quadrature Phase Output <i>Yo-Hao Tu, Kuo-Hsing Cheng, Chih-Hsun Hsu, Hong-Yi Huang</i>	163
High Throughput Architecture for the Advanced Encryption Standard Algorithm <i>Salma Hesham, Mohamed A. Abd El Ghany and Klaus Hofmann</i>	167

Session 5B (Student Session): Digital

Generic Partial Dynamic Reconfiguration Controller for Transient and Permanent Fault Mitigation in Fault Tolerant Systems Implemented Into FPGA <i>Lukas Miculka, Zdenek Kotasek</i>	171
Low Latency Book Handling in FPGA for High Frequency Trading <i>Milan Dvořák, Jan Kořenek</i>	175
CRC Based Hashing in FPGA Using DSP Blocks <i>Tomáš Závodník, Lukáš Kekely, Viktor Puš</i>	179

Session 6A: FPGA & Reconfigurable Systems

The LSI Implementation of a Memory Based Field Programmable Device for MCU Peripherals <i>Tetsuya Matsumura, Naoya Okada, Yoshifumi Kawamura, Koji Nii, Kazutami Arimoto, Hiroshi Makino, Yoshio Matsuda</i>	183
Design Methodology of Configurable High Performance Packet Parser for FPGA <i>Viktor Puš, Lukáš Kekely, Jan Kořenek</i>	189
A Study on Fast Pipelined Pseudo-Random Number Generator Based on Chaotic Logistic Map <i>Paweł Dąbal, Ryszard Pelka</i>	195

Session 6B: Delay & Embedded Test

Modeling Timing Constraints for Automatic Generation of Embedded Test Instruments <i>S. Ostendorff, J.-H. Meza Escobar, H.-D. Wuttke, T. Sasse, S. Richter</i>	201
Path Delay Test in the Presence of Multi-Aggressor Crosstalk, Power Supply Noise and Ground Bounce <i>A. Asokan, A. Todri-Sanial, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel</i>	207
Test and Diagnosis of Power Switches <i>M. Valka, A. Bosio, L. Dilillo, A. Todri, A. Virazel, P. Girard, P. Debaud, S. Guilhot</i>	213

Poster Session 1

Fast Lookup for Dynamic Packet Filtering in FPGA <i>Lukáš Kekely, Martin Žádník, Jiří Matoušek, Jan Kořenek</i>	219
Protecting Combinational Logic in Pipelined Microprocessor Cores Against Transient and Permanent Faults <i>I. Wali, A. Virazel, A. Bosio, L. Dilillo, P. Girard, A. Todri</i>	223
Stabilization Methods for Integrated High Voltage Charge Pumps <i>Lufei Shen, Ferdinand Keil, Klaus Hofmann</i>	226
FPGA Design of the Computation Unit for the Semi-Global Stereo Matching Algorithm <i>Mikołaj Roszkowski, Grzegorz Pastuszek</i>	230
System Design for Enhanced Forward-Engineering Possibilities of Safety Critical Embedded Systems <i>Martin Krammer, Michael Karner, Anton Fuchs</i>	234
Mismatch Effects and their Correction in Large Area ASICs <i>Piotr Maj</i>	238
A Unified CMOS Inverter Model for Planar and FinFET Nanoscale Technologies <i>Panagiotis Chaourani, Spyridon Nikolaidis</i>	242
A New Architecture for Minimum Mean Square Error Sorted QR Decomposition for MIMO Wireless Communication Systems <i>Victor Tomashevich, Christina Gimmler-Dumont, Christian Fesl, Norbert Wehn, Ilia Polian</i>	246
Dedicated Hardware Architecture for Object Tracking Preprocessing Implemented in FPGA <i>Peter Malik</i>	250

Emulation Based Fault Injection on UHF RFID Transponder <i>Omar Abdelmalek, David Hely, and Vincent Beroulle</i>	254
Sources of Bias in EDA Tools and Its Influence <i>Petr Fišer, Jan Schmidt, Jiří Balcárek</i>	258
Automatic and Reliable Electrical Characterization of MOSFETs <i>Z. Stamenković, N. D. Vasović and G. S. Ristić</i>	262
An Approach Towards Selection of the Oscillation Frequency for Oscillation Test of Analog ICs <i>Martin Kováč, Daniel Arbet, Gabriel Nagy, Viera Stopjaková</i>	266
Customer Return Detection with Features Selection <i>Domenico Bertocelli, Pasquale Caianiello</i>	268
Poster Session 2	
Designing of Test Pattern Generators for Stimulation of Crosstalk Faults in Bus-type Connections <i>Tomasz Garbolino</i>	270
On NFA-Split Architecture Optimizations <i>Vlastimil Košar, Jan Kořenek</i>	274
ADCs in Deep Submicron Technologies for ASICs of Pixel Architecture <i>Piotr Ofinowski, Paweł Gryboś, Robert Szczygiel, Piotr Maj</i>	278
Numerical and Theoretical Analysis on Voltage and Time Domain Dynamic Range of scaled CMOS Circuits <i>Kevin Ngari Muriithi, Toru Nakura, Kunihiro Asada</i>	282
On the In-Field Test of Branch Prediction Units Using the Correlated Predictor Mechanism <i>M. Gaudesi, S. Saleem, E. Sanchez, M. Sonza Reorda, E. Tanowe</i>	286
FPGA Architectures of the Quantization and the Dequantization for Video Encoders <i>Grzegorz Pastuszek</i>	290
An Efficient Hardware Architecture for Inter-Prediction in H.264/AVC Encoders <i>Nam-Khanh Dang, Xuan-Tu Tran, Alain Merirot</i>	294
An Intra-Cell Defect Grading Tool <i>A. Bosio, L. Dilillo, P. Girard, A. Todri-Sanial, A. Virazel, S. Bernabovi, P. Bernardi</i>	298
Heuristic Algorithm of Two-level Minimization of Fuzzy Logic Functions <i>Andrzej Wielgus</i>	302
Verifying Robust Frequency Domain Properties of Non Linear Oscillators using SMT <i>Hafiz ul Asad, Kevin D. Jones, Frederic Surre</i>	306
Modeling and Analysis of Cracked Through Silicon Via (TSV) Interconnections <i>Vasileios Gerakis, Christina Avdikou, Alexandros Liolios, Alkis Hatzopoulos</i>	310
Case Study: BISR for a Processor Multiplier <i>Andrej Kincel, Marcel Balaz</i>	314
Efficient VHDL Implementation of Symbol Synchronization for Software Radio based on FPGA <i>Pavel Fiala, Richard Linhart</i>	318
Author Index	322