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S.-K. Park, N.-Y. Kim, E.-M. Kwon, S.-Y. Kim, I.-W. Cho and K.-D. Yoo, SK hynix Inc., System IC division, Technology Development Team, R&D division, Cheongju-si, Chungbuk, KOREA
- III-43 **Performance analysis of different SRAM cell topologies employing tunnel-FETs**  
S. Strangio<sup>1,2</sup>, P. Palestri<sup>1</sup>, D. Esseni<sup>1</sup>, L. Selmi<sup>1</sup>, and F. Crupi<sup>2</sup>, <sup>1</sup>DIEGM, University of Udine, Udine, ITALY and <sup>2</sup>DIMES, University of Calabria, Cosenza, ITALY
- III-44 **Phase Change Router for Nonvolatile Logic**  
N. H. Kan'an, H. Silva and A. Gokirmak, Electrical & Computer Engineering, University of Connecticut, Storrs, Connecticut, USA
- III-45 **Physical Understanding of Graphene/Metal Hetero-contacts to Enhance MoS<sub>2</sub> Field-effect Transistors Performance**  
Y. Du<sup>1</sup>, L. Yang<sup>1</sup>, J. Zhang<sup>1</sup>, H. Liu<sup>1</sup>, K. Majumdar<sup>2</sup>, P. D. Kirsch<sup>2</sup>, and P. D. Ye<sup>1</sup>, <sup>1</sup>School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana, USA and <sup>2</sup>SEMATECH, Albany, New York, USA
- III-46 **Proposal of a topological insulator based magnetoelectric transistor**  
X. Duan, X. Li, Y. G. Semenov, and K. W. Kim, Department of Electrical Engineering, North Carolina State University, Raleigh, North Carolina, USA

- III-47      **ReRAM Device Performance Study with Transition Metal Disulfide Interfacial Layer** %  
W. Lu, W. Chen, Y. Li, P. Thapaliya, and R. Jha, Department of EECS, University of Toledo,  
Toledo, Ohio, USA
- III-48      **Room Temperature Negative Differential Resistance in a GaN-based Tunneling Hot  
Electron Transistor** %  
Z. C. Yang, D. N. Nath, and S. Rajan, Department of Electrical and Computer Engineering, The  
Ohio State University Columbus, Ohio, USA
- III-49      **Scaling Analysis of In-plane and Perpendicular Anisotropy Magnetic Tunnel Junctions  
Using a Physics-Based Model** % )  
J. Kim, H. Zhao, Y. Jiang, A. Klemm, J.-P. Wang, and C. H. Kim, Department of Electrical and  
Computer Engineering, University of Minnesota, Minneapolis, Minnesota, USA
- III-50      **Surface transport and DC current gain in InGaAs/InP DHBTs for THz applications** % +  
H.-W. Chiang, J. C. Rode, P. Choudhary, and M. J. W. Rodwell Department of ECE, University  
of California, Santa Barbara, California, USA
- III-51      **Terahertz Emission and Detection in Double-Graphene-Layer Structures** % -  
T. Otsuji<sup>1</sup>, V. Y. Aleshkin<sup>2</sup>, A. A. Dubinov<sup>2</sup>, M. Ryzhii<sup>3</sup>, V. Mitin<sup>4</sup>, M. S. Shur<sup>5</sup>, and V. Ryzhii<sup>1,6</sup>,  
<sup>1</sup>Research Institute of Electrical Communication, Tohoku University, Sendai, JAPAN, <sup>2</sup>Institute  
for Physics of Microstructures RAS, Nizhny Novgorod, RUSSIA, <sup>3</sup>Department of Computer  
Science and Engineering, University of Aizu, Aizu-Wakamatsu, JAPAN, <sup>4</sup>Department of  
Electrical Engineering, University at Buffalo, Buffalo, New York, USA, <sup>5</sup>Department of Electrical,  
Electronics, and System Engineering, Rensselaer Polytechnic Institute, Troy, New York, USA,  
and <sup>6</sup>Institute of Ultra-High-Frequency Semiconductor Electronics, RAS, Moscow, RUSSIA
- III-52      **The Influence of NH<sub>3</sub> Plasma Treatment on Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> Gate Dielectrics of TFTs with  
Atmospheric Pressure Plasma Jet Deposited IGZO Channel** % %  
H.-Y. Huang<sup>1</sup>, C.-H. Wu<sup>2</sup>, S.-J. Wang<sup>1</sup>, K.-M. Chang<sup>3</sup>, and H.-Y. Hsu<sup>3</sup>, <sup>1</sup>Institute of  
Microelectronics, Dept. of Electrical Eng., National Cheng Kung Univ., Tainan, Taiwan, R.O.C.,  
<sup>2</sup>Department of Electronics Engineering, Chung Hua University, Hsinchu, Taiwan, R.O.C, and  
<sup>3</sup>Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan,  
R.O.C
- III-53      **The origin of massive nonlinearity in Mixed Ionic Electronic Conduction (MIEC)-based  
Access Devices, as revealed by numerical device simulation** % %  
A. Padilla<sup>1</sup>, G. W. Burr<sup>1</sup>, R. S. Shenoy<sup>1</sup>, K. V. Raman<sup>3</sup>, D. Bethune<sup>1</sup>, R. M. Shelby<sup>1</sup>, C. T.  
Rettner<sup>1</sup>, J. Mohammad<sup>1</sup>, K. Virwani<sup>1</sup>, P. Narayanan<sup>1</sup>, A. K. Deb<sup>3</sup>, R. K. Pandey<sup>4</sup>, M. Bajaj<sup>4</sup>, K.  
V. R. M. Murali<sup>4</sup>, B. N. Kurdi<sup>1</sup>, and K. Gopalakrishnan<sup>2</sup>, <sup>1</sup>IBM Research – Almaden, San Jose,  
California, USA, <sup>2</sup>IBM T. J. Watson Research Center, Yorktown Heights, New York, USA, <sup>3</sup>IBM  
India Research Labs, Bangalore KA, INDIA, and <sup>4</sup>IBM SRDC India, Bangalore KA, INDIA
- III-54      **The Voltage-Triggered SET Mechanism and Self-Compliance Characteristics in Intrinsic  
Unipolar SiO<sub>x</sub>-Based Resistive Switching Memory** % )  
Y.-F. Chang<sup>1</sup>, B. Fowler<sup>2</sup>, Y.-C. Chen<sup>3</sup>, L. Ji<sup>1</sup>, F. Zhou<sup>1</sup>, and J. C. Lee<sup>1</sup>, <sup>1</sup>MRC, The University of  
Texas at Austin, Austin, Texas, USA, <sup>2</sup>PrivaTran, LLC, Austin, Texas, USA and <sup>3</sup>Dept. of EE,  
Natl. Chiao Tung University, Hsinchu, TAIWAN
- III-55      **Topological surface state transport and current saturation in topological insulator  
nanoribbons field effect transistors** % +  
L. A. Jauregui<sup>1</sup>, M. T. Pettes<sup>2</sup>, L. Shi<sup>2</sup>, and Y. P. Chen<sup>1</sup>, <sup>1</sup>Purdue University, West Lafayette,  
Indiana, USA and <sup>2</sup>University of Texas at Austin, Austin, Texas, USA
- III-56      **Vertical heterojunction of MoS<sub>2</sub> and WSe<sub>2</sub>** % -  
S. Xiao, M. Li, A. Seabaugh, D. Jena and H. Xing, Department of Electrical Engineering,  
University of Notre Dame, Notre Dame, Indiana, USA
- III-57      **Multi-Layer MoTe<sub>2</sub> p-Channel MOSFETs with High Drive Current** % %  
Late News      N. Haratipour and S. J. Koester, ECE Department, University of Minnesota-Twin Cities,  
Minneapolis, Minnesota, USA



III-58 Late News	<b>N-polar III-Nitride Tunneling Hot Electron Transfer Amplifier</b> Z. C. Yang, D. N. Nath, Y. Zhang and S. Rajan, The Ohio State University, Department of Electrical and Computer Engineering, Columbus, Ohio, USA
III-59 Late News	<b>Reflection Spectromicroscopy for the Design of Nanopillar Optical Antenna Detectors</b> A. C. Farrell <sup>1</sup> , P. Senanayake <sup>1</sup> , C.-H. Hung <sup>1</sup> , M. Currie <sup>2</sup> , and D. L. Huffaker <sup>1,3</sup> , <sup>1</sup> Electrical Engineering Department, University of California at Los Angeles, Los Angeles, California, USA, <sup>2</sup> Optical Sciences Division, Naval Research Laboratory, Washington, District of Columbia, USA, and <sup>3</sup> California NanoSystems Institute, University of California at Los Angeles, Los Angeles, California, USA
III-60 Late News	<b>Experimental demonstration of strain-clocked Boolean Nanomagnetic Logic and Information Propagation</b> N. D'Souza, M. Salehi-Fashami, S. Bandyopadhyay and J. Atulasimha, Virginia Commonwealth University, Richmond, Virginia, USA

Session IV.A.	<b>ATOMICALLY THIN DEVICES</b>	<b>179-204</b>
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IV.A-1 8:20	<b>What can we really expect from 2D materials for electronic applications?</b> D. Logoteta, Q. Zhang, and G. Fiori, Dipartimento di Ingegneria dell'Informazione, Università di Pisa, Pisa, ITALY
IV.A-2 9:00	<b>Multi-Valley High-Field Transport in 2-Dimensional MoS<sub>2</sub> Transistors</b> A. Y. Serov <sup>1</sup> , V. E. Dorgan <sup>1</sup> , C. D. English <sup>2</sup> and E. Pop <sup>2</sup> , <sup>1</sup> Dept. of Electrical and Computer Eng., University of Illinois Urbana-Champaign, Urbana, Illinois, USA and <sup>2</sup> Dept. of Electrical Engineering, Stanford University, Stanford, California, USA
IV.A-3 9:20 AM	<b>Electrostatically Doped WSe<sub>2</sub> CMOS Inverter</b> S. Das and A. Roelofs, Center for Nanoscale Materials, Argonne National Laboratory, Argonne, Illinois, USA
IV.A-4 9:40 AM	<b>Design and Analysis of MoS<sub>2</sub>-Based MOSFETs for Ultra-Low-Leakage Dynamic Memory Applications</b> C. Kshirsagar, W. Xu, C. H. Kim, and S. J. Koester, University of Minnesota-Twin Cities, Minneapolis, Minnesota, USA
IV.A-5 10:30 AM	<b>Correlating Interface Chemistry and Device Behavior</b> R. M. Wallace, University of Texas at Dallas, Richardson, Texas, USA
IV.A-6 11:10 AM	<b>Defining and Overcoming the Contact Resistance Challenge in Scaled Carbon Nanotube Transistors</b> A. D. Franklin and W. Haensch, IBM T. J. Watson Research Center, Yorktown Heights, New York, USA
IV.A-7 11:30 AM	<b>Improving Contact Resistance in MoS<sub>2</sub> Field Effect Transistors</b> C. D. English <sup>1</sup> , G. Shine <sup>1</sup> , V. E. Dorgan <sup>2</sup> , K. C. Saraswat <sup>1</sup> , and E. Pop <sup>1</sup> , <sup>1</sup> Dept. of Electrical Engineering, Stanford University, Stanford, California, USA and <sup>2</sup> Dept. of Electrical and Computer Eng., University of Illinois, Urbana-Champaign, Urbana, Illinois, USA
IV.A-8 11:50 AM	<b>Evaluating Au and Pd contacts in mono and multilayer MoS<sub>2</sub> transistors</b> N. Kaushik <sup>1</sup> , A. Nipane <sup>1</sup> , F. Basheer <sup>1</sup> , S. Dubey <sup>2</sup> , S. Grover <sup>2</sup> , M. Deshmukh <sup>2</sup> , and S. Lodha <sup>1</sup> , <sup>1</sup> Dept of Electrical Engineering, IIT Bombay, Mumbai, INDIA and <sup>2</sup> Dept. of Condensed Matter Physics and Materials Science, TIFR, Mumbai, INDIA
IV.A-9 1:30 PM	<b>Wafer Scalable Growth and Delamination of Graphene for Silicon Heterogeneous VLSI Technology</b> S. Rahimi <sup>1</sup> , S. R. Na <sup>2</sup> , L. Tao <sup>1</sup> , K. Liechti <sup>2</sup> and D. Akinwande <sup>1</sup> , <sup>1</sup> Department of Electrical and Computer Engineering, and <sup>2</sup> Department of Aerospace Engineering and Engineering Mechanics, Microelectronic Research Center, The University of Texas - Austin, Austin, Texas, USA

- IV.A-10  
1:50 PM  
**Variability of Graphene Mobility and Contacts: Surface Effects, Doping and Strain** -  
E. A. Carrion<sup>1</sup>, J. D. Wood<sup>1</sup>, A. Behman<sup>1</sup>, M. Tung<sup>1,2</sup>, J. W. Lyding<sup>1</sup> and E. Pop<sup>1,2</sup>, <sup>1</sup>Dept. of Electrical and Computer Engineering, University of Illinois, Urbana-Champaign, Illinois, USA and <sup>2</sup>Dept. of Electrical Engineering, Stanford University, Stanford, California, USA
- IV.A-11  
2:10 PM  
**Ambipolar Phosphorene Field-Effect Transistors with Dielectric Capping**  
H. Liu, A. T. Neal, and P. D. Ye, School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana, USA
- IV.A-12  
2:30 PM  
**Voltage Scalability of Double-Gate Ultra-Thin-Body Field-Effect Transistors with Channel Materials from Group IV, III-V to 2D-Materials based on ITRS Metrics for Year 2018 and Beyond**  
K. L. Low, Y.-C. Yeo, and G. Liang, Department of Electrical and Computer Engineering, National University of Singapore (NUS), SINGAPORE

## Session IV.B. III-V FETs

205-228

- IV.B-1  
8:20 AM  
**III-V Gate-Wrap-Around Field-Effect-Transistors with High-k Gate Dielectrics**  
F. Zhou, F. Xue, Y.-F. Chang and J. Lee, Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, Texas, USA
- IV.B-2  
9:00 AM  
**In<sub>0.63</sub>Ga<sub>0.37</sub>As FinFETs Using Selectively Regrown Nanowires with Peak Transconductance of 2.85 mS/μm at V<sub>ds</sub> = 0.5 V**  
C. B. Zota, L.-E. Wernersson and E. Lind, Department of Electrical and Information Technology, Lund University, Lund, SWEDEN
- IV.B-3  
9:20 AM  
**RF Performance of 3D III-V Nanowire T-Gate HEMTs Grown by VLS Method**  
K. D. Chabak<sup>1,2</sup>, X. Miao<sup>1</sup>, C. Zhang<sup>1</sup>, D. E. Walker Jr.<sup>2</sup>, and X. Li<sup>1</sup>, <sup>1</sup>Department of Electrical and Computer Engineering, Micro and Nanotechnology Laboratory, University of Illinois at Urbana-Champaign, Urbana, Illinois, USA and <sup>2</sup>Air Force Research Laboratory, Sensors Directorate, Wright-Patterson Air Force Base, Ohio, USA
- IV.B-4  
9:40 AM  
**InAs Gate-all-around Nanowire MOSFETs by Top-down Approach**  
H. Wu<sup>1</sup>, X. B. Lou<sup>3</sup>, M. Si<sup>1</sup>, J. Y. Zhang<sup>1</sup>, R. G. Gordon<sup>3</sup>, V. Tokranov<sup>2</sup>, S. Oktyabrsky<sup>0</sup>, and P. D. Ye<sup>1</sup>, <sup>1</sup>School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana, USA, <sup>2</sup>SUNY College of Nanoscale Science and Engineering, Albany, New York, USA, and <sup>3</sup>Department of Chemistry and Chemical Biology, Harvard University, Cambridge, Massachusetts, USA
- IV.B-5  
10:30 AM  
**Nanometer InP Electron Devices for VLSI and THz Applications**  
M. J. W. Rodwell<sup>1</sup>, S. Lee<sup>1</sup>, C.-Y. Huang<sup>1</sup>, D. Elias<sup>1</sup>, V. Chobpattanna<sup>2</sup>, J. Rode<sup>1</sup>, H.-W. Chiang<sup>1</sup>, P. Choudhary<sup>1</sup>, R. Maurer<sup>1</sup>, M. Urteaga<sup>3</sup>, B. Brar<sup>3</sup>, A.C. Gossard<sup>2</sup>, and S. Stemmer<sup>2</sup>, <sup>1</sup>ECE and <sup>2</sup>Materials Departments, University of California, Santa Barbara, USA, and <sup>3</sup>Teledyne Scientific and Imaging, Thousand Oaks, California, USA
- IV.B-6  
11:10 AM  
**Ultra-Thin-Body Self-Aligned InGaAs MOSFETs on Insulator (III-V-O-I) by a Tight-Pitch Process**  
J. Lin<sup>1</sup>, L. Czornomaz<sup>2</sup>, N. Daix<sup>2</sup>, D. A. Antoniadis<sup>1</sup>, and J. A. del Alamo<sup>1</sup>, Microsystems Technology Laboratories, <sup>1</sup>Massachusetts Institute of Technology, Cambridge, Massachusetts, USA and <sup>2</sup>IBM Zurich Research Laboratory, Zurich, SWITZERLAND
- IV.B-7  
11:30 AM  
**InGaAs Double-Gate Fin-Sidewall MOSFET**  
A. Vardi, X. Zhao and J. A. del Alamo, Microsystems Technology Laboratories, Massachusetts Institute of Technology (MIT), Cambridge, Massachusetts, USA

- IV.B-8  
11:50 AM  
**Vertical electron transistors with  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  channel and N-polar  $\text{In}_{0.1}\text{Ga}_{0.9}\text{N}/\text{GaN}$  drain achieved by direct wafer-bonding**  
J. Kim, S. Lal, M. A. Laurent, and U. K. Mishra, Department of Electrical and Computer Engineering, University of California, Santa Barbara, California, USA
- IV.B-9  
1:30 PM  
**35 nm-Lg Raised S/D  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  Quantum-well MOSFETs with 81 mV/decade Subthreshold Swing at  $V_{\text{DS}}=0.5\text{ V}$**   
S. Lee<sup>1</sup>, C.-Y. Huang<sup>1</sup>, D. C. Elias<sup>1</sup>, B. J. Thibeault<sup>1</sup>, W. Mitchell<sup>1</sup>, V. Chobpattana<sup>2</sup>, S. Stemmer<sup>2</sup>, A. C. Gossard<sup>2</sup>, and M. J. W. Rodwell<sup>1</sup>, <sup>1</sup>ECE Department and <sup>2</sup>Materials Department, University of California, Santa Barbara, California, USA
- IV.B-10  
1:50 PM  
**Influence of InP Source/Drain Layers upon the DC Characteristics of InAs/InGaAs MOSFETs**  
C.-Y. Huang<sup>1</sup>, S. Lee<sup>1</sup>, D. C. Elias<sup>1</sup>, J. J. M. Law<sup>1</sup>, V. Chobpattana<sup>2</sup>, S. Stemmer<sup>2</sup>, A. C. Gossard<sup>1,2</sup>, and M. J. W. Rodwell<sup>1</sup>, <sup>1</sup>Department of Electrical and Computer Engineering and <sup>2</sup>Materials Department, University of California, Santa Barbara, California, USA
- IV.B-11  
2:10 PM  
**Growth Process for High Performance of InGaAs MOSFETs**  
Y. Miyamoto<sup>1</sup>, T. Kanazawa<sup>1</sup>, Y. Yonai<sup>1</sup>, K. Ohsawa<sup>1</sup>, Y. Mishima<sup>1</sup>, T. Irisawa<sup>2</sup>, M. Oda<sup>2</sup>, and T. Tezuka<sup>2</sup>, <sup>1</sup>Dept. Physical Electronics, Tokyo Institute Technology, Meguro, JAPAN and <sup>2</sup>Collaborative Research Team Green Nanoelectronics Center (GNC), AIST, Tsukuba, JAPAN

## Session V.A CMOS DEVICES AND MEMORY

229-246

- V.A-1  
3:20 PM  
**High Performance Flexible CMOS SOI FinFETs**  
H. Fahad, G. Torres S., M. Ghoneim and M. M. Hussain Integrated Nanotechnology Lab, Electrical Engineering, CEMSE Division, King Abdullah University of Science and Technology, Thuwal, SAUDI ARABIA
- V. A -2  
3:40 PM  
**Measurement and Analysis of Gate-Induced Drain Leakage in Short-Channel Strained Silicon Germanium-on-Insulator pMOS FinFETs**  
K. Balakrishnan, P. Hashemi, J. A. Ott, E. Leobandung, and D.-G. Park, IBM Research, T. J. Watson Research Center, Yorktown Heights, New York, USA
- V. A -3  
4:00 PM  
**Cryogenic implantation for source/drain junctions in Ge p-channel (Fin)FETs**  
P. Bhatt<sup>1</sup>, P. Swarnkar<sup>1</sup>, S. Mittal<sup>1</sup>, F. Basheer<sup>1</sup>, C. Thomidis<sup>2</sup>, C. Hatem<sup>2</sup>, B. Colombeau<sup>2</sup>, N. Variam<sup>2</sup>, A. Nainani<sup>2</sup>, and S. Lodha<sup>1</sup>, <sup>1</sup>CEN, Dept of EE, Indian Institute of Technology Bombay, Mumbai, INDIA and <sup>2</sup>Applied Materials Inc., Santa Clara, California, USA
- V. A -4  
4:20 PM  
**Investigation of Electrostatic Body Control in Accumulated Body MOSFETs**  
M. B. Akbulut<sup>1</sup>, F. Dirisaglik<sup>1</sup>, A. Cywar<sup>1</sup>, A. Faraclas<sup>1</sup>, D. Pence<sup>1</sup>, J. Patel<sup>2</sup>, S. Steen<sup>2</sup>, R. Nunes<sup>2</sup>, H. Silva<sup>1</sup>, and A. Gokirmak<sup>1</sup>, <sup>1</sup>Electrical & Computer Engineering, University of Connecticut, Storrs, Connecticut, USA and <sup>2</sup>IBM Thomas J. Watson Research Center, Yorktown Heights, New York, USA
- V. A -5  
4:40 PM  
**Exploring the Design Space for Resistive Nonvolatile Memory Crossbar Arrays with Mixed Ionic-Electronic-Conduction (MIEC)-based Access Devices**  
P. Narayanan<sup>1</sup>, G. W. Burr<sup>1</sup>, R. S. Shenoy<sup>1</sup>, S. Stephens<sup>1</sup>, K. Virwani<sup>1</sup>, A. Padilla<sup>1</sup>, B. Kurdi<sup>1</sup>, and K. Gopalakrishnan<sup>2</sup>, <sup>1</sup>IBM Research – Almaden, San Jose, California, USA and <sup>2</sup>IBM T. J. Watson Research Center, Yorktown Heights, New York, USA
- V. A -6  
5:00 PM  
**High Performance sub-430°C Epitaxial Silicon PIN Selector for 3D RRAM**  
R. Mandapati<sup>1</sup>, S. Shrivastava<sup>1</sup>, B. Das<sup>1</sup>, Sushama<sup>1</sup>, V. Ostwal<sup>1</sup>, J. Schulze<sup>2</sup>, and U. Ganguly<sup>1</sup>, <sup>1</sup>Indian Institute of Technology, Bombay, INDIA, and <sup>2</sup>University of Stuttgart, Stuttgart, GERMANY

V. A -7  
5:20 PM

**Resistive Switching of SiO<sub>x</sub> with One Diode-One Resistor Nanopillar Architecture Fabricated via Nanosphere Lithography**

L. Ji<sup>1</sup>, Y.-F. Chang<sup>1</sup>, B. Fowler<sup>2</sup>, Y.-C. Chen<sup>4</sup>, T.-M. Tsai<sup>3</sup>, K.-C. Chang<sup>3</sup>, M.-C. Chen<sup>3</sup>, T.-C. Chang<sup>3</sup>, S. M. Sze<sup>4</sup>, E. T. Yu<sup>1</sup> and J. C. Lee<sup>1</sup>, <sup>1</sup>Microelectronics Research Center, The University of Texas at Austin, Austin, Texas, USA, <sup>2</sup>PrivaTran, LLC, Austin, Texas, USA, <sup>3</sup>Department of Materials and Optoelectronic Science, Department of Physics, National Sun Yat-Sen University, Kaohsiung, TAIWAN, and <sup>4</sup>Department of Electronics Engineering, National Chiao Tung University, Hsinchu, TAIWAN

V. A -8  
5:40 PM

**Two-terminal Proton Conducting Devices with Synaptic Behavior and Memory**

M. Rolandi<sup>1</sup>, E. E. Josberger<sup>1,2</sup>, Y. Deng<sup>1</sup>, W. Sun<sup>1</sup>, and R. Kautz<sup>1</sup>, <sup>1</sup>Department of Materials Science and Engineering, University of Washington, Seattle, Washington, USA and <sup>2</sup>Department of Electric Engineering, University of Washington, Seattle, Washington, USA

**Session V.B ENERGY AND WIDE BANDGAP**

**247-260**

V.B-1  
3:20 PM

**Making the Mid-IR Nano with Epitaxial Plasmonic Devices**

S. Law<sup>1</sup>, C. Roberts<sup>2</sup>, S. Inampudi<sup>2</sup>, W. Streyer<sup>1</sup>, A. Rosenberg<sup>1</sup>, V. Podolskiy<sup>2</sup> and D. Wasserman<sup>1</sup>, <sup>1</sup>Department of Electrical and Computer Engineering, University of Illinois, Urbana, Illinois, USA and <sup>2</sup>Department of Physics and Applied Physics, UMass Lowell, Lowell, Massachusetts, USA

V.B-2  
4:00 PM

**Indoor Photovoltaic Energy Harvesting for mm-Scale Systems**

A. Teran<sup>1</sup>, M. Dejarld<sup>2</sup>, J. Hwang<sup>1</sup>, W. Lim<sup>1</sup>, J. Wong<sup>1</sup>, D. Blaauw<sup>1</sup>, Y. Lee<sup>1</sup>, J. Millunchick<sup>2</sup>, and J. Phillips<sup>1</sup>, <sup>1</sup>Electrical Engineering and Computer Science and <sup>2</sup>Materials Science and Engineering, University of Michigan, Ann Arbor, Michigan, USA

V.B-3  
4:40 PM

**Low ON-Resistance and high current GaN Vertical Electron Transistors with buried p-GaN layers**

R. Yeluri<sup>1</sup>, J. Lu<sup>1</sup>, D. Browne<sup>2</sup>, C. A. Hurni<sup>2</sup>, S. Chowdhury<sup>3</sup>, S. Keller<sup>1</sup>, J. S. Speck<sup>2</sup> and U. K. Mishra<sup>1</sup>, <sup>1</sup>Electrical and Computer Engineering Department, University of California Santa Barbara, Santa Barbara, California, USA, <sup>2</sup>Materials Department, University of California Santa Barbara, Santa Barbara, California, USA, and <sup>3</sup>Electrical Engineering, Arizona State University, Tempe, Arizona, USA

V.B-4  
5:00 PM

**Common Emitter operation of III-N HETs using AlGaIn and InGaIn polarizationindipole induced barriers**

G. Gupta<sup>1</sup>, M. Laurent<sup>1</sup>, H. Li<sup>1</sup>, D. J. Suntrup III<sup>2</sup>, E. Acuna<sup>1</sup>, S. Keller<sup>1</sup> and U. Mishra<sup>1</sup>, <sup>1</sup>Department of Electrical and Computer Engineering and <sup>2</sup>Department of Physics, University of California Santa Barbara, Santa Barbara, California, USA

V.B-5  
5:20

**Improvement of the Dynamic On-Resistance Characteristics of GaN-on-Si Power Transistors with A Sloped Field-Plate**

Z. Li, R. Chu, D.I Zehnder, S. Khalil, M. Chen, X. Chen, and K. Boutros, HRL Laboratories, LLC., Malibu, California, USA

V.B-6  
5:40

**First Monolithic Integration of GaN-Based Enhancement Mode n-Channel and p-Channel Heterostructure Field Effect Transistors**

H. Hahn, B. Reuters, S. Kotzea, G. Lükens, S. Geipel, H. Kalisch and A. Vescan  
GaN Device Technology, RWTH Aachen University, Aachen, GERMANY

## RUMP SESSIONS

261-262

R.1  
8:30 PM

### **What Are 2D Devices and Materials Good For?''B#**

Session Organizers: S. Rajan, Ohio State and Max Lemme, U. Siegen

R.2  
8:30 PM

### **Next 10 Years of Wide Bandgap ''B#**

Session Organizers: A. Vescan, RWTH Aachen and M. Higashiwaki, National Institute of Information and Communications Technology

## JOINT DRC/EMC PLENARY SESSION

263-264

8:30 AM

### **Stretchy Electronics That Can Dissolve in Your Body''B#**

J. Rogers, University of Illinois at Urbana/Champaign

## Session VI.A THIN-FILM AND ORGANIC

265-282

VI.A-1  
10:00 AM

### **Tin Disulfide (SnS<sub>2</sub>) Thin-Film Field-Effect Transistors''&\* +**

U. Zschieschang, T. Holzmann, B. V. Lotsch, and H. Klauk, Max Planck Institute for Solid State Research, Stuttgart, GERMANY

VI.A-2  
10:40 AM

### **Double-Gate ZnO TFT Active Rectifier''&\* -**

K. G. Sun<sup>1,2</sup> and T. N. Jackson<sup>1,2</sup>, <sup>1</sup>Center for Thin Film Devices and Materials Research Institute and <sup>2</sup>Department of Electrical Engineering, Penn State University, University Park, Pennsylvania, USA

VI.A-3  
11:00 AM

### **Thin-Film Circuits for Scalable Interfacing Between Large-Area Electronics and CMOS ICs''&+%**

T. Moy, W. Rieutort-Louis, Y. Hu, L. Huang, J. Sanz-Robinson, J. C. Sturm, S. Wagner, and N. Verma, Department of Electrical Engineering, Princeton University, Princeton, New Jersey, USA

VI.A-4  
11:20 AM

### **Current Gain of Amorphous Silicon Thin-Film Transistors Above the Cutoff Frequency''&+'**

W. Rieutort-Louis, L. Huang, Y. Hu, Jo. Sanz-Robinson, T. Moy, Y. Afsar, J. C. Sturm, N. Verma, and S. Wagner, Department of Electrical Engineering, Princeton University, Princeton, New Jersey, USA

VI.A-5  
1:30 PM

### **Electrostatic desalting of micro-droplets to enable novel chemical/biosensing applications''&+)**

P. Dak and M. A. Alam, School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana, USA

VI.A-6  
1:50 PM

### **Low-Power Organic Electronics Based on Gate-tunable Injection Barrier in Vertical Graphene–Organic Semiconductor Heterostructures''&+–**

H. Hlaing<sup>1,2</sup>, F. Carta<sup>2</sup>, R. Barton<sup>1</sup>, C.-Y. Nam<sup>4</sup>, N. Petrone<sup>3</sup>, J. Hone<sup>1,3</sup>, and I. Kymissis<sup>1,2</sup>, <sup>1</sup>Energy Frontier Research Center, <sup>2</sup>Department of Electrical Engineering, <sup>3</sup>Department of Mechanical Engineering, Columbia University, New York, New York, USA and <sup>4</sup>Center for Functional Nanomaterials, Brookhaven National Laboratory, Upton, New York, USA

VI.A-7  
2:10 PM

### **Critical Binding Energy for Exciton Dissociation and its Implications for the Thermodynamic Limit of Organic Photovoltaics ''&, %**

M. R. Khan and M. A. Alam, School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana, USA

VI.A-8  
2:30 PM

**Air-Stable, Low-Voltage Organic Transistors: High-Mobility Thienoacene Derivatives for Unipolar and Complementary Ring Oscillators on Flexible Substrates**\*\*\*& ' U. Kraft<sup>1,2</sup>, M. Sejfić<sup>1</sup>, T. Zaki<sup>4</sup>, F. Letzkus<sup>4</sup>, J. N. Burghartz<sup>4</sup>, K. Takimiya<sup>3</sup>, E. Weber<sup>1,2</sup>, and H. Klauk<sup>1</sup>, <sup>1</sup> Max Planck Institute for Solid State Research, Stuttgart, GERMANY, <sup>2</sup>Technical University Freiberg, Freiberg, GERMANY, <sup>3</sup>RIKEN Advanced Science Institute, Wako, Saitama, JAPAN, and <sup>4</sup>Institute for Microelectronics Stuttgart (IMS CHIPS), Stuttgart, GERMANY

## Session VI.B MAGNETO, FERRO AND RESISTIVE DEVICES

283-300

VI.B-1  
10:00 AM

**SPICE Models for Metallic All---Spin---Logic Devices and Interconnects**\*\*\*& + A. Naeemi, School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, Georgia, USA

VI.B-2  
10:40 AM

**Observation of resonant modes of coupled domain walls**\*\*& - T. Phung, A. Pushp, C. Rettner, B. Hughes, S.-H. Yang, and S. S. P. Parkin, IBM Almaden Research Center, San Jose, California, USA

VI.B-3  
11:00 AM

**The Effect of Electric Field Induced Magnetic Anisotropy in Ferromagnetic Resonance in Magnetic Tunnel Junctions**\*\*\*& % Y. Lv, H. Zhao, X. Chao, and J.-P. Wang, Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, Minnesota, USA

VI.B-4  
11:20 AM

**The Spin Switch Oscillator: A New Approach Based on Gain and Feedback**\*\*\*& ' V. Q. Diep and S. Datta, School of Electrical and Computer Engineering, Purdue University, W. Lafayette, Indiana, USA

VI.B-5  
1:30 PM

**Feasibility Analysis of High-Density STTRAM Designs with Crossbar or Shared Transistor Structures**\*\*\*& ) A. Chen, TD Research, GLOBALFOUNDRIES, Santa Clara, California, USA

VI.B-6  
1:50 PM

**Artificial Synapses using Ferroelectric Memristors Embedded with CMOS Circuit for Image Recognition**\*\*\*& + Y. Nishitani, Y. Kaneko, and M. Ueda, Advanced Technology Research Laboratories, Panasonic Corporation, Kyoto, JAPAN

VI.B-7  
2:10 PM  
**Late News**

**Detection of the conductive filament growth direction in resistive memories**\*\*\*& - E. Yalon<sup>1</sup>, D. Kalaev<sup>2</sup>, A. Gavrilov<sup>1</sup>, S. Cohen<sup>1</sup>, I. Riess<sup>2</sup> and D. Ritter<sup>1</sup>, <sup>1</sup>Department of Electrical Engineering, Technion, Israel Institute of Technology, Haifa, ISRAEL and <sup>2</sup>Physics Department, Technion, Israel Institute of Technology, Haifa, ISRAEL

VI.B-8  
2:30 PM

**Late News**