2014 IEEE 57th International Midwest Symposium on Circuits and Systems

(MWSCAS 2014)

College Station, Texas, USA
3-6 August 2014

Pages 1-538

IEEE Catalog Number: CFP14MID-POD
ISBN: 978-1-4799-4131-5

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Monday, August 4, 2014

Session A1L-A: Nyquist-Rate Data Converters I

Chair: R. Jake Baker, *University of Nevada, Las Vegas*
Time: Monday, August 4, 2014, 10:10 - 11:50
Location: Mockingbird

A counting analog-to-digital converter (ADC) is proposed which achieves a high sampling rate by performing the conversion in several (N) steps. In terms of the effective number of bits (ENOB) of the ADC, the conversion time of the ADC is approximately N.2ENOB/N clock periods, which is much shorter than for traditional counting ADCs (2ENOB clock periods). This is achieved by using novel methods of residue amplification and correlated double sampling. Simulation results are provided to verify the effectiveness of this structure.

Session A1L-C: Low Power and High Performance Digital Integrated Circuits Design

Chair: Yong-Bin Kim, *Northeastern University*
Co-Chair: Kyung Ki Kim, *Daegu University*
Time: Monday, August 4, 2014, 10:10 - 11:50
Location: North & South 40

In this work, we implement our previously proposed charge sharing symmetric adiabatic logic (CSSAL) in an 8-bit S-box circuit using a multi-stage positive polarity Reed-Muller (PPRM) representation with a composite field technique. We evaluate the effectiveness of the CSSAL S-box circuit against side-channel attacks tawards the variations of the CMOS process technology. The results of this paper are obtained from the SPICE simulation with 0.18 μ and 90-nm standard CMOS technology at an operating frequency band of 125 KHz--70 MHz.

The clockless feature of asynchronous circuit promotes its application in Digital Signal Processing (DSP) under special applications such as ultra-low power and extreme environments. In this paper, Finite Impulse Response (FIR) filter is implemented in delay-insensitivity asynchronous circuit using the pipeline architecture of Multi-Threshold NULL Conventional Logic (MTNCL). The computing units with different pipeline stages and pattern delay shift registers are integrated as 4 designs of FIR filter using the IBM 130nm 8RF process. Simulation results demonstrate the tradeoff between system throughput and energy efficiency, as the number of pipeline stage changes in the circuit.

Energy-efficiency is among the most important goals of the current IC industry. To achieve this goal each subcomponent of a chip must be optimized for energy). Even though a tremendous amount of research has been dedicated to optimizing floating-point multipliers (FPM) for better performance, efforts are continuously being made to further enhance them, indicating their importance in the computing world. Hence a multi-mode operating energy-efficient FPM is introduced in this work. This double-precision multiplier dynamically adapts to three modes of operations based on the effective precision of the inputs: low-precision, asymmetric, and full modes, where a 24x24, 24x53, or 53x53 fraction multiplication is required, respectively. Due to the highly frequent occurrence of low-precision operands (i.e., the least significant bits of the fraction are zeros), switching between these modes saves energy by avoiding unnecessary bit-level computations. Results show up to 25% and 21% savings in dynamic energy and total energy, respectively. A two-tier 3DIC FPM design is also proposed to further enhance the performance of the multi-mode FPM.

This paper introduces a new three-dimensional doping scheme for the transistors in subthreshold circuits. It is characterized by the absence of halos at the source and drain region. Under the proposed scheme there can be four different doping profiles for subthreshold device. In this paper we concentrate on Gaussian doping distributions both along the channel and across the depth of the transistor. Results show that the optimized device with the proposed doping profile improves the ON current. The analysis is done by varying the doping profile and gate-source voltage (Vgs), and the observations are compared with the super-threshold device.

Session A1L-D: Power Converters for Energy Harvesting Applications

Chair: Hoi Lee, *University of Texas, Dallas*
Co-Chair: Ayman Fayed, *Iowa State University*
Time: Monday, August 4, 2014, 10:10 - 11:50
Location: Ballroom – 6

Session A1L-E: Reconfigurable RF-CAS for RADAR, Cognitive Radio and EARS – II

Chair: Changzhi Li, *Texas Tech University*
Co-Chair: Arjuna Madanayake, *University of Akron*
Time: Monday, August 4, 2014, 10:10 - 11:50
Location: Ballroom – 7

Two kinds of reconfigurable microwave couplers are presented. The first one is a 90-degree branch-line coupler with a wide range of tunable coupling ratios. When its coupling ratio is tuned to be 1, this coupler becomes a crossover. The second one possesses a reconfigurable performance between a rat-race coupler and a 90-degree coupler. Varactors are loaded to both couplers as the tuning elements. By applying suitable control voltages, reconfigurable performance is realized. Closed-form equations are derived to theoretically analyze the proposed devices. To further verify the design theory, both structures are simulated. Moreover, the first coupler is fabricated and characterized.

The Volterra Series, more specifically the Memory Polynomial Model, is utilized to model power and frequency dependent non-linear distortion of a high power amplifier. This modeling technique is also used to create a digital predistortion model that makes the overall transmission chain behave linearly as a function of power. Digital predistortion is especially useful for wideband signals, where it allows the amplifier to operate at highest power added efficiency in the compression region while still behaving linearly. Therefore, wideband radar waveforms can be generated at high fidelity, maximizing transmission power with the given equipment while maintaining low range sidelobes.

Due to the noncontact and low-cost properties of Doppler radar, it has been adopted to detect movement in variety applications. This paper introduces a portable Doppler radar sensor device named as iMotion radar which is a 2.4-GHz AC-coupled continuous-wave mode Doppler radar. This iMotion radar has been designed as a 5cm x 5cm printed circuit board and has already been used in different applications. The results for being used in different applications showed the reliability and flexibility of iMotion Radar. The detail in hardware design will be given in this paper and a body orientation identification application which has been done by iMotion Radar will be reviewed.

In this paper an RF channel-select filter with improved blocker rejection is presented. The proposed filter consists of three bandpass resonators and two notch resonators all implemented with N-path switched-capacitor filters. Due to the inclusion of notch resonators between the bandpass resonators, the rejection of the filter in the vicinity of the passband is higher compared with any existing filters. Out-of-band blockers are suppressed due to high filter rejection. The proposed filter has 48.3 dB rejection at 20 MHz offset and has 58.8 dB rejection at 45 MHz offset from the center frequency. The high stopband rejection of 71.2 dB has been achieved by creating notches outside the bandwidth of the filter. The filter is tunable from 0.2 GHz to 1.8 GHz. The filter is designed in 65 nm CMOS technology.

A miniaturized planar log-periodic dipole array (LPDA) antenna is presented. Antenna miniaturization is accomplished by replacing the uniform dipole elements of the conventional LPDA antenna with elements that possess variable-impedance profiles governed by a truncated Fourier series. Conventional and miniaturized LPDA antennas exhibiting 7 dB end-fire gains are designed to operate over the frequency range of 2 to 4 GHz. A 32 % reduction in dipole arm length was achieved. Full-wave simulation results show stable directional radiation patterns, excellent front-to-back ratio over the designed impedance bandwidth, and minimal degradation in the overall electrical performance.

Session A1L-F: High-Speed Interfaces and High-Sensitivity Signal Detectors

Chair: Marvin Onabajo, *Northeastern University*
Time: Monday, August 4, 2014, 10:10 - 11:50
Location: Brazos

This paper presents receive-side circuitry which merges near-end and far-end crosstalk cancellation. NEXT cancellation is realized with a novel 3-tap FIR filter which combines two traditional FIR filter taps and a continuous-time band-pass filter IIR tap, with all coefficients automatically determined via an on-die SS-LMS adaptation engine. FEXT cancellation is realized with a differentiator circuit whose gain is automatically adjusted with a power-detection-based adaptation loop. A 65nm CMOS prototype operates at 10 Gb/s over coupled 4-in FR4 transmission line channels with NEXT and FEXT aggressors and opens a previously closed eye to allow for a 0.2 UI timing margin.

This paper describes the implementation issues in designing a 1 tap current integrating half rate decision feedback equalizer. We introduce a new technique for designing an 8Gbps 1 tap half rate current integrating DFE in 40nm CMOS technology that draws 0.67mW from a 1.1V supply. The technique uses a delayed clock rather than speculation. This removes the speculation impact on power consumption and timing constraints especially in multi tap DFE.

This paper presents a low-power 28 Gb/s PLL-based clock and data recovery circuit in 65 nm CMOS technology. The artificial LC transmission line technique is proposed to be used in the full rate bang-bang phase detector to reduce the number of D-latches and save power consumption by 42.8% compared with the conventional phase detector design. By using the transmission line technique, the retiming circuit is merged into the phase detector, which further saves power of the data retiming circuit. The compact phase detector with built-in retiming circuit also alleviates the capacitive loading of and saves corresponding power consumed by the clock buffer. In addition, the artificial LC transmission line is proposed to be used in the clock buffer to drive the distributed capacitive loads presented by separate D-latch and save power consumption by 50% compared with the conventional inductive peaking clock buffer. The total power consumption of the CDR is 35 mW from a 1.1 V supply.

A high dynamic range, high detection sensitivity piecewise RSSI (received signal strength indicator) for software-defined radio (SDR) and cognitive radio (CR) receivers is proposed. With the reconfigurable limiting amplifiers, the RSSI achieves wide dynamic range and high detection sensitivity simultaneously. Two-path I/Q configuration RSSI structure is adopted to reduce the output voltage glitch. The transfer curve of the RSSI keeps stable under various PVT variations with the help of the self-adaptive bias circuit. The proposed RSSI has been implemented in 65nm CMOS and occupies 0.06 mm2 chip area. It consumes a scalable current from 1mA to 2.4mA from 1.2V power supply, dependent on the limiting amplifier setting. The simulated results show that the RSSI can detect the signal strength from -80dBm to 0dBm with 30mV/dB detection sensitivity and maximum 1.4dB linearity error over 100KHz~20MHz input carrier frequency range.

This paper presents the design and implementation of an electronic front-end intended for spatial detection of ion beams at counting rates higher than 10^6 particles per second. The readout system is made up of three main multi-channel building blocks, namely: a transimpedance preamplifier, a signal- conditioning line receiver and a charge-to-digital converter, which are properly combined with some off-the-shelf components. Sev- eral experiments have been carried out, considering α particles sources and particles beams, featuring an adaptive shaping time frame of 170-to-230 ns with a peak signal-to-noise ratio of up to 25.2dB. These performance metrics are competitive with the state of the art, showing the suitability of the proposed data acquisition system for accurate and fast particle tracking detection.

Session A2L-A: Nyquist-Rate Data Converters II

Chair: R. Jake Baker, *University of Nevada, Las Vegas*
Time: Monday, August 4, 2014, 13:10 - 14:50
Location: Mockingbird

In this paper a segmented pre-quantize and bypass architecture for SAR ADC has been proposed. The capacitive DAC is segmented and small capacitor array is used to convert the MSB codes. According to the result of pre-quantization unnecessary switching of high weight capacitors are bypassed, which improves the power efficiency and linearity of ADC and accelerates the conversion speed. A 10-bit 150MS/s ADC with the proposed architecture is implemented in a standard 65nm CMOS technology. According to the simulation, the ADC performs an ENOB of 9.77-bit and 82.8dB SFDR at transistor level simulation, achieving a FOM of 9.33 fJ/Conversion step.

Spectral activity detection in wideband radio-frequency (RF) signals for cognitive-radio applications typically necessitates expensive and energy-inefficient analog-to-digital converters (ADCs). In this paper, we present a novel compressive sensing (CS)-based analog front-end, which is able to sample sparse wideband RF signals at low cost and low power. The analog front-end consists of a pseudo-random non-uniform clock generator unit offering the possibility to configure the (average) undersampling factor at run-time, and a low-cost, wideband 1.9 GS/s 4-bit flash ADC. The spectral information acquired at sub-Nyquist rates can be recovered off-line via novel sparse signal dequantization algorithms. The developed analog front-end is implemented in 28 nm CMOS, and enables the recovery of spectrally sparse RF signals up to 3.8 GHz by means of CS, which corresponding to a Nyquist-equivalent sampling rate of 7.6 GS/s. The ADC and pseudo-random clock generator together occupy less than 0.1 mm^2, and consume an estimated 4.1 mW to 5.4 mW for undersampling factors between 4 and 11.5.

The SAR ADCs for biomedical application, have a strict limit on its power consumption. Two techniques are introduced into its design: a novel ladder-based reconfigurable time domain comparator is proposed to reduce the noise and to adjust power according to inputs automatically; and a novel clock distribution scheme is utilized to save more than 55% power consumption. The prototype chip is designed and fabricated in UMC 0.18µm technology. The simulation results show that with supply voltage of 0.9V, the ADC consumes 1.07µW at the sampling rate of 200kS/s. And the SNDR is 71.2 dB with 3.24kHz input signal

In this paper, we have proposed a 4-bit 5-GSample/s flash analog-to-digital converter (ADC) for pulse amplitude modulation (PAM) systems. In order to achieve low-power consumptions, digitalized cells for analogue amplifying are developed in the proposed ADC. Digitalized cells reduce power significantly due to using fewer devices as compared to pure analogue designs. A self-biasing circuit is used in the digitalized amplifier can enhance linear amplifying region. Besides, the digitalized amplifier can achieve high speed according to its bandwidth compensation technique. The test chip is implemented with 90nm CMOS Logic and Mixed-Mode 1P9M Low-K Process. The low-power digitalized ADC is operated under 5GSample/s. All the results of post-simulation are demonstrate in a 16-PAM system, and efficient number of bit is 3.9bit. Moreover, INL and DNL are less than 0.5LSB. The power consumption of the ADC is 33.7mW, and the FoM of energy per conversion step is only 0.45pJ. The overall chip area is 0.873mm2.

Session A2L-C: High Performance Digital VLSI Design Method

Chair: Jia Di, *University of Arkansas*
Co-Chair: Volnei Pedroni, *UTFPR, Brazil*
Time: Monday, August 4, 2014, 13:10 - 14:50
Location: North & South 40

Session A2L-D: Image Processing and Multimedia Systems I

Chair: Marvin Onabajo, *Northeastern University*
Time: Monday, August 4, 2014, 13:10 - 14:50
Location: Ballroom – 6

Session A2L-E: Multispectral and Hyperspectral Remote Sensing

Chair: William McDowell, *Lockheed Martin*
Co-Chair: Wasfy Mikhael, *University of Central Florida*
Time: Monday, August 4, 2014, 13:10 - 14:50
Location: Ballroom – 7

We propose a new spectral unmixing method using a semantic spectral representation, which is produced via non-homogeneous hidden Markov chain (NHMC) models applied to wavelet transforms of the spectra.Previous studies have shown that the representation is robust to spectral variability in the same materials because it can automatically detect the diagnostic spectral features in the training data. Therefore, our method can successfully detect materials while automatically extracting diagnostic features. Simulations show that our unmixing method can be effectively used in the case of Hapke mixtures.

Over the years infrared imaging technology has enabled many critical applications such as thermal and spectral imaging, medical diagnostics, and remote sensing. The growth in infrared imaging technology has been made possible by dramatic technical advances in infrared sensor manufacturing, as well as improvements in algorithms for image processing. However, the most powerful existing infrared imaging systems are still far behind their biological counterparts in many aspects including energy efficiency, computational capabilities, and performance. Inspired by biological imaging systems, in this paper we present an intelligent readout circuit based upon spectrally tunable infrared nanostructure sensors, which can revolutionize multispectral remote sensing systems.

The evolution of Electro-Optical (EO) technology has continuously advanced towards minimizing a sensor's size, weight and cost while simultaneously increasing key performance metrics such as resolution and range. Frequently, these dichotomous objectives make for a trade space which is difficult to resolve. Fortunately, the use of unresolved multispectral and hyperspectral imagery fused with other Measurement And Signature Intelligence (MASINT) such as target kinematic features presents an opportunity to extend a sensor's useful classification / discrimination range without requiring additional hardware innovation. In this paper, we will provide an overview of multispectral, hyperspectral and kinematic based MASINT phenomenologies which are available for extraction and exploitation. Additionally, we will review feature and information fusion from the perspective of Maximum Likelihood, Naïve Bayes and Bayesian Belief Networks in the context of MASINT Information Fusion.

Session A2L-F: Control Systems, Mechatronics and Robotics

Chair: Carlos Silva Cardenas, *Pontificia Universidad Católica del Peru*
Time: Monday, August 4, 2014, 13:10 - 14:50
Location: Brazos

The purpose of this paper is to extend the Quasi-Steady State Approximation and Matrix Block Diagonalization methods utilized in the Approximate Controller Design for Singularly Perturbed Aircraft Systems paper by Sawan and Shim 2005. In that paper, it was shown that an approximate controller solution could be developed by relocating only the slow poles for two-time scale aircraft dynamics. In addition, it showed the difference between the approximate solutions and the exact solutions were bounded within limits as $O(\varepsilon)$ and $O(\varepsilon 2)$. This technique was successfully applied to the lateral dynamics of the DeHaviland Canada DHC-2 Beaver. In this paper, the same technique is applied to the NASA F-8 Aircraft dynamics in order to show that the method is not unique to the Beaver and can be applied to other aircraft models. It also extended the method to consider the singularly perturbed stochastic system and confirmed stability was maintained.

Session A3P-G: Amplifiers and Filters I

Chair: Paul Furth, *New Mexico State University*
Co-Chair: Tina Wang, *Iowa State University*
Time: Monday, August 4, 2014, 14:50 - 15:40
Location: Poster Area

Session A3P-H: Amplifiers and Filters II

Chair: Paul Furth, *New Mexico State University*
Time: Monday, August 4, 2014, 14:50 - 15:40
Location: Poster Area

This paper presents the design and characterization of a high gain, high-speed differential transimpedance amplifier (TIA) to be used as front-end interface for optical receiver applications. The TIA is realized in a standard 0.18-µm digital CMOS technology and it dissipates 25.4mW from a single 1.8 V supply. The topology consists of a common gate input stage followed by a cascoded common source and a common drain stage surrounded by a global shunt-shunt feedback with phantom zero compensation to boost bandwidth and enhance stability. Using this approach the amplifier achieves transimpedance gain of 59.75 dbΩ, -3dB bandwidth of 2.9 GHz when connected to a 2-pF photodiode at the input and a 250 Ω load at the output, and 13.14 pA/√Hz input referred noise.

This paper presents a new realization of a first-order transadmittance-mode (TAM) all-pass filter (APF). In the proposed mixed-mode APF a simple transconductor, inverting voltage buffer, and unity-gain current follower are used as active building blocks. Considering the input intrinsic resistance of current follower as useful active filter parameter, the proposed TAM APF only employs a floating capacitor as external passive component. Hence, it is a resistorless circuit. In addition, due to high-impendence voltage input and high-impedance of output current terminal, it is fully cascadable filter realization. SPICE simulation results are included to support the theory. In the design the PTM 90 nm level-7 CMOS process BSIM3v3 parameters with low (±0.5 V) DC voltages were used.

Session A3P-J: Systems and VLSI Architectures

Chair: Zoran Stamenkovic, *IHP, Frankfurt*
Time: Monday, August 4, 2014, 14:50 - 15:40
Location: Poster Area

In this paper, we propose a new lifting-based DWT architecture for 9/7 filter, with lowest temporal memory among the existing architectures. This is achieved with a novel overlapped- scanning method and recalculation of intermediate DWT coefficients. The proposed architecture requires only 2N temporal memory to process N x N sized image. The architecture has a critical path of one multiplier delay and demonstrate 100% hardware utilization efficiency.

In this paper, a flipping-based high speed VLSI architecture for lifting-based 2-D DWT is proposed. The direct implementation of lifting equation has long critical path delay. To reduce the critical path, the flipping structure is widely used. In the proposed architecture, the multipliers in flipping structure are replaced by shift-and-add algorithm. This reduces the critical path delay to one adder (Ta), which is the minimum possible delay any DWT architecture can have. Thus, the proposed architecture is suitable for high frequency operation and has 100% hardware utilization with low control complexity.

A marine acoustic system for underwater target tracking is described. This system is part of the Integrated Satellite and Acoustic Telemetry (iSAT) project to study marine fauna. It is a microcontroller-based underwater projector and receiver. A narrow-band, passive sonar detection architecture is described from signal generation, through transduction, reception, signal processing and up to tone extraction. Its circuit and operation principles are described. Finally, a comparison between the current energy detection method versus an alternative matched filter approach is included.

Session A3P-K: VLSI Design, Simulation and Testing I

Chair: Carlos Silva Cardenas, *Pontificia Universidad Católica del Peru*
Time: Monday, August 4, 2014, 14:50 - 15:40
Location: Poster Area

3-D IC provides more logic space by introducing multiple tier structure. Effective communication across the tiers can be very challenging. TSVs are utilized for signal propagation between multiple tiers. Different TSV allocation methodologies have been investigated. We have analyzed different TSV redundancies and provided some guidelines. It has been found that router based redundancy requires less number of cells as compared to its counterparts. But router based redundancy is hardware demanding as compared to 1:4 and 2:4 redundancies and requires extra time to adopt spare path. Moreover, router based redundancy has about three times redundant TSVs per cell than its counterpart redundancies.

To improve immunity against process gradients, a common centroid constraint, in which every pair of capacitors should be placed symmetrically with respect to a common center point, is widely used. Several methods to obtain a good placement satisfying the constraints were proposed. However, the distance between cells in a common centroid group may be redundantly long, and it degrades the immunity. In this paper, we propose a novel algorithm to place cells belonging to each common centroid group. The algorithm is simple, but it is proved to be effective.

Comparative study between the proposed technique and MATLAB-built-in deconvolution-functions with regard to deconvolution errors is discussed, which have a crucial impact in reversing the effects of convolution with Random Telegraph Noise (RTN) and Random Dopant Fluctuation (RDF) on overall SRAM margin variations. The proposed algorithm successfully avoids noise amplification thanks to eliminating the need for any operations of differential, division, and maximum-likelihood gradient sequence. This advantage over the MATLAB-built-in deconvolution-functions has been demonstrated for the first time with applying it to a real analysis for the effects of the RTN/RDF on the overall SRAM margin variations. It has been shown that the proposed technique can reduce fail-bit-count estimation error based on the convolution of the deconvoluted-RTN with the RDF by 10^14-fold compared with the MATLAB-built-in deconvolution-functions.

Session A3P-L: VLSI Design, Simulation and Testing II

Chair: Carlos Silva Cardenas, *Pontificia Universidad Católica del Peru*
Time: Monday, August 4, 2014, 14:50 - 15:40
Location: Poster Area

Automatic sizing of analog integrated circuits (ICs) remains an open challenge. This work shows an hybrid approach for finding optimal sizes of analog IC's elements, by combining the gm/ID technique for determining the parameter ranges for a given biasing levels, and using those to limit the search space through performing multi-objective optimization with evolutionary algorithms. That way, the NSGA-II optimization algorithm is employed to optimize the width (W) and length (L) of MOSFETs of an operational transconductance amplifier, which (W/L) search spaces are found by applying equations and biasing conditions to the gm/ID technique. From simulation results, we conclude on the appropriateness of gm=ID to accelerate the computational time of evolutionary algorithms for optimizing analog ICs.

In this paper, a new time delay model is presented for the case real poles in RLC interconnect for a step input. The proposed delay model is based on the second order approximate transfer function of distributed RLC interconnect network. The proposed model would be an efficient analytical tool to estimate RLC interconnect behavior. The results indicate that the real pole model is much faster than the previously developed complex pole model.

Session A4L-A: Amplifiers

Chair: Paul Furth, *New Mexico State University*
Co-Chair: Tina Wang, *Iowa State University*
Time: Monday, August 4, 2014, 15:40 - 17:20
Location: Mockingbird

Sequential Interstage Correlated Double Sampling: A Switched-Capacitor Technique for High Accuracy Systems 262

Pedram Payandehnia (Oregon State University), Hamidreza Maghami (Oregon State University), Xin Meng (Oregon State University), Gabor C. Temes (Oregon State University), Hirokazu Yoshizawa (Saitama Institute of Technology)

A novel sequential inter-stage correlated double sampling technique has been proposed. This technique provides considerable enhancement in the effective accuracy of a switched-capacitor architecture. Superior accuracy and thermal noise performance is achieved compared to the conventional correlated double sampling technique. The proposed approach provides higher input signal bandwidth by reducing the number of clock phases using a predictive phase compared to the other sequential techniques to achieve the same performance. Also, the proposed approach has the capability of driving both resistive and capacitive loads

An Investigation Into the Effect of Carrier Generators on Power Supply Noise in PWM Class D Amplifiers 266

Huiqiao He (Nanyang Technological University), Tong Ge (Nanyang Technological University), Linfei Guo (Nanyang Technological University), Joseph S. Chang (Nanyang Technological University)

Class D amplifiers are ubiquitous as audio amplifiers due to their significantly higher power-efficiency compared to their linear counterparts (such as Class AB) due to the digital-like switching mode operation of the Class D output stage. However, one drawback of Class D amplifiers is the susceptibility to supply noise, qualified and quantified by Power Supply Rejection Ratio (PSRR) and Power Supply Induced Intermodulation Distortion (PS-IMD). Poor PSRR and PS-IMD may result in audible noise at the output and this is particular the case when the Class D amplifier is integrated with in an SoC (System on a Chip) where the power supply is usually noisy. In this paper, PSRR and PS-IMD of Single-ended, 2-state bridge-tied load (BTL) and 3-state BTL Class D amplifiers based on various Carrier Generators are investigated and compared. We show that the design of the carrier generator is critical and should be designed according to the structure of the Class D amplifier " we show in this paper that the same Carrier Generator may result in >70dB PSRR in the 3-state BTL Class D amplifier but a mere 1dB PSRR in the 2-state BTL Class D amplifier.

A Simple Slew Rate Enhancement Technique with Improved Linearity and Preserved Small Signal Performance 270

Bin Huang (Iowa State University and Maxim Integrated Products Inc.), Degang Chen (Iowa State University)

A simple yet very effective slew rate enhancement (SRE) method is proposed. The proposed SRE feedback is off for small signal operation to preserve an amplifier's small signal performance, and is activated to enhance slew rate (SR) and linearity only when an amplifier is slewing. The new SRE scheme applies to both single-stage and multi-stage, both single-ended and fully differential amplifiers. Compared with a conventional OTA, the OTA with the proposed SRE scheme shows SRE by a factor of 23.2, THD improvement of 6dB and preserved small signal performance with only 1.2% area and 2% power consumption overhead. Compared with the adaptive biasing method, the proposed scheme shows 300% SR improvement, 18dB THD improvement but with power and area consumption decreased by 11.1% and 25% respectively.

Session A4L-B: Advances in Device Modeling and Circuits for Special Applications

Chair: Marvin Onabajo, *Northeastern University*
Time: Monday, August 4, 2014, 15:40 - 17:20
Location: Ballroom – 5

High Voltage Charge Pump with Triple Well Diodes in a 0.13 µm Bulk CMOS Process 274

Jiwei Sun (Clemson University), Pingshan Wang (Clemson University)

This paper presents charge pump circuits with modified triple well diodes as charge transfer switches for charging on-chip pulse generation circuits in a low-voltage bulk CMOS process. Guard-rings and isolation deep n-wells are used to improve the breakdown voltages and reduce leakage currents of the diodes. Model parameters of the triple well diode are extracted based on measured diode characteristics. These parameters are then used to analyze our charge pump. The proposed charge pump circuits are implemented in a commercial 0.13 µm bulk CMOS process. The output voltage of the four-stage charge pump circuit can be up to 18.1 V, which is much higher than the n-well/p-substrate breakdown voltage (~10 V) of the given process.

Comparison of MOSFET Mismatch Models with Random Physical and Random Model Variables 278

Srijita Patra (Iowa State University), Randall Geiger (Iowa State University)

A comparison between two established MOSFET mismatch modeling approaches, one based upon the use of uncorrelated random physical variables and one based upon the use of correlated random model variables where the correlation is ignored, is presented. An analytical formulation is introduced that enables the designer to easily predict the relative errors in matching performance that will occur if the more popular random model parameters are used instead of the uncorrelated physical parameters. It is shown that neglecting the correlation inherent in the random model variables will result in under-estimate of the area required for meeting a fixed yield target but in the example process considered in this paper, the errors introduced by using the correlated model parameters are small.

Session A4L-C: FPGA and Digital Hardware Design

Chair: Nader Rafla, *Boise State University*
Time: Monday, August 4, 2014, 15:40 - 17:20
Location: North & South 40

This paper describes ongoing research pertaining to the analysis of design radiation hardness for circuits implemented in Field-Programmable Gate Array (FPGA) devices. Radiation induces single event effects in FPGAs that can cause erroneous operation by upsetting data bits or changing logic behavior. Design-level techniques can mitigate these upsets to some degree; however, there is currently no method available to quantify the benefit of these techniques. This research is developing a framework to score designs for upset hardness. Additionally, this framework will determine the most susceptible locations in design netlists that would most benefit from additional design mitigation against upset.

Hardware Trojans pose a difficult threat to hardware systems due to the difficulty in their identification. In many cases, the differences observed between Trojan and Trusted chips can be very small. This research explored the feasibility of using low-precision test equipment in order to identify malicious modifications to circuits programmed to Field Programmable Gate Arrays (FPGAs). Examination using an ELVIS II Instrumentation board was able to correctly classify ISCAS85 c6288 multipliers based on their internal structure, allowing for identification of suspect designs. These tests were conducted in the context of the 2012 Cyber-Security Awareness Week Embedded Systems Challenge.

Session A4L-D: Devices and Circuits for Health Monitoring I

Chair: Aydin Karsilayan, *Texas A&M University*
Time: Monday, August 4, 2014, 15:40 - 17:20
Location: Ballroom – 6

This paper reports on a corticospinal interface IC as a core building block for next-generation integrated neural interfaces targeted at functional recovery from spinal cord injury. Fabricated in 0.35um 2P/4M CMOS, the IC integrates a 2-channel, 10b, neural-recording front-end with digitally programmable gain and bandwidth, and a 4-channel, constant-current, stimulating back-end for delivering programmable trains of charge-balanced monophasic or asymmetric biphasic current pulses up to ~100uA. The IC functionality is demonstrated in vivo by low-noise recording of extracellular neural spikes from an anesthetized rat's cerebral cortex, and by distinct muscle pattern activation in the rat's hindlimb facilitated via intraspinal microstimulation.

A smart capsule for in-body pH and temperature continuous monitoring is presented, for non-invasive gastrointestinal examination. The whole system consists of a smart capsule for pH value and temperature sensing, and a portable data logger. Two chips, ADC and transceiver, and MCU is applied in the system. The power consumption is low and accuracy of the capsule system is high.

A low-power PPM demodulator has been developed for remotely powered batteryless implantable devices. The required power is harvested by the magnetic coupling with external powering coils placed under the living space of the animal. The remote powering is turned off only 1% of a bit duration during data transmission. The PPM demodulator consumes only 22.7 µW at 1.8 V and has 5.55 kb/s data rate. Entire system and basic blocks integrated using a 0.18 µm CMOS technology are presented. Experimental results show the effectiveness of the PPM demodulator and the communication system.

Session A4L-E: Advances in Energy and Power ICs

Chair: Hoi Lee, *University of Texas, Dallas*
Co-Chair: Ayman Fayed, *Iowa State University*
Time: Monday, August 4, 2014, 15:40 - 17:20
Location: Ballroom – 7

Session A4L-F: SPECIAL SESSION: Smart Energy and Security

Chair: Shiyan Hu, *Michigan Technological University*
Co-Chair: Jiang Hu, Texas A&M University
Time: Monday, August 4, 2014, 15:40 - 17:20
Location: Brazos

Electric Vehicles (EV) are known to have three times more energy efficient than petroleum internal combustion engine (ICE) vehicles. This is true if we do not consider electricity generation, transmission and vehicle battery charging efficiency. ICE vehicles have various vendor-specific technologies regarding fuel efficiency including engines, transmissions and their matching. EV, on the other hand, fuel efficiency is largely dependent on the vehicle weight thanks to simplified drivetrain such as direct drive without a transmission. Nevertheless, true energy efficiency of EV should be justified by the source of electricity. This paper introduces a custom, light-weight EV prototype for partial solar powered EV. We demonstrate the custom energyefficient EV prototype and possibility of partially solar-powered EV. I

Smart home becomes an emerging research topic these years. It offers various advantages such as facilitating the control of home appliances and the reduction of electricity bill. In this paper, a dynamic programming based game theoretic algorithm is proposed for multiple user smart home scheduling which can handle home appliances with multiple discrete power levels. The simulation results on test cases of 1000 to 5000 users demonstrate that our algorithm using game theory can achieve reduction of monetary cost of energy consumption by 29% on average comparing to the algorithm without game theory. In addition, our algorithm produces more balanced energy consumption.

Model-based design is being increasingly used in the development of real-time embedded control systems due to its capabilities to support early design verification and validation through formal functional models. Similarly as in the case for circuit design, to facilitate the adoption of high level functional models and truly reduce design complexity, it is important to have automated synthesis tools that can generate correct and optimal implementations from those functional models. The development of such synthesis tools has some unique challenges compared to synchronous circuit design - the functional model for real-time embedded systems has more diverse semantics, the implementation platform is more distributed and often asynchronous, and there are strict timing requirements along with a variety of other design objectives.

Tuesday, August 5, 2014

Session B1P-G: Sensors and Oscillators

Chair: Jin Liu, *University of Texas at Dallas*
Time: Tuesday, August 5, 2014, 9:20 - 10:10
Location: Poster Area

This paper describes a fast-settling all-digital PLL with a low-power TDC based on retimed reference clock and a lock detector focused on monitoring a toggling phase error. With the intention of reducing power dissipation, the proposed TDC employs the low-rate reference and retimed reference clocks to measure the fine fractional phase error between the low-rate reference and high-rate oscillator clocks. In addition, the use of the retimed reference clock to the TDC results in a new simple DCO clock period calculation algorithm which employs the maximum and minimum values for the fractional error correction. A lock detector, which is required to accomplish the switchover of the DCO frequency tuning mode, allows a fast settling to be actuated independent of loop bandwidth and frequency step. By dissipating 8mW at 1.2-V supply voltage, the proposed digital PLL achieves 230ns settling time, 1.7psrms period jitter.

Session B1P-H: Techniques, Simulation, Modeling and Testing

Chair: Jin Liu, *University of Texas at Dallas*
Time: Tuesday, August 5, 2014, 9:20 - 10:10
Location: Poster Area

Analog signal-processing in deep sub-micron technologies poses many challenges arising from both low supply voltage and intrinsic voltage-gain of short channel devices. Class- AB CMOS transconductance obtained by a pair of complementary transistors is a widely used power efficient building block because it has linear v/i characteristics. This is topologically the same as the logic inverter of CMOS digital systems. This block enables the basic signal-processing operations of addition, subtraction, scaling and integration. Replica-circuits are used to keep the large process, voltage and temperature (PVT) variations under control. Thus we can perform analog signal-processing at a level of precision required for designing high-speed data communication systems. This paper discusses this in a canonical fashion. Simulation results using device models for 65 nm CMOS process are presented to validate these ideas.

Bootstrapping techniques improve the linearity of switched-capacitor circuits, especially for low supply voltage. This paper proposes simple but effective techniques for bootstrapping floating switches. The method is applicable to such fundamental circuits as sample-and-hold (S/H) stages, switched-capacitor (SC) filters and SC amplifiers. It can make the on-resistance and channel charge of the switches independent of the signal, and hence enables linear operation even for low bias voltages.

The Read out Integrated Circuit (ROIC) consists of charge integration, charge to voltage conversion, Pixel voltage multiplexing, signal transfer and amplification stage. The IR detectors requires the integration of large charge handling capacity >10M", at the same time sensitive enough to detect signals just above the noise floor of better than 900". The design and measured results of 4x4 array ROIC chip with 10 M" charge handling capacity , 30µm pixel pitch, snapshot mode of operation, variable integration time, 3 Mpps readout rate and readout noise of 350" reported at ambient temperature and discussed in the paper.

Challenges of using standard circuit simulators to determine the presence or absence of undesired operating points are discussed. Examples are given of circuits and simulation strategies that show the presence of undesired operating points when they exist but other examples are given that show the same strategies can fail to show the presence of undesired operating points under modestly different simulation conditions. Since many of the most widely used analog and mixed-signal circuits that are known to be vulnerable to the multiple equilibrium point problem have no standard electrical inputs, it is shown that a temperature sweep may be useful in some applications for identifying the presence of undesired operating points.

On-chip data processing capabilities have increased very rapidly over the last decades creating off-chip bandwidth a strong limiting factor. Limitations of this off-chip communication originate from interconnect, vias and connectors leading to reflections over chip-to-chip interconnect and leads to intersymbol interference. These variations dynamically change based on interconnect length, number of vias and connectors, needing adaptive equalization. This scenario becomes more worse and unpredictable in a multi-drop bus environment, leading to complete eye closure. In this work, we propose a 5 Gb/s adaptive continuous time linear equalizer (CTLE) with eye-monitoring in a multi-drop bus environment. The coefficients of CTLE are adjusted to compensate the channel nonlinearities based on the feedback received from the eye-monitoring device. Adaptive CTLE is designed in 1.8V, 0.18u m CMOS technology for 5 Gb/s data transmission over a 7.5 inch FR4 PCB trace. The power consumed by adaptive CTLE is 18mW for a bit error rate of 10^(-12).

Session B1P-J: Linear and Non-Linear Circuits and Systems

Chair: Samuel Palermo, *Texas A&M University*
Time: Tuesday, August 5, 2014, 9:20 - 10:10
Location: Poster Area

Session B1P-K: Power Management Techniques I

Chair: Ayman Fayed, *Iowa State University*
Time: Tuesday, August 5, 2014, 9:20 - 10:10
Location: Poster Area

A stepwise-voltage-generation circuit was devised that is based on a capacitor bank and that dissipates no energy when a stepwise voltage is generated. The stepwise voltage is generated spontaneously, and depends neither on the initial voltages to the capacitors nor on the switching order. A new adiabatic-charging circuit based on this circuit was also devised that increases the voltage in a stepwise fashion. The total capacitance of the capacitors in the regenerator is much smaller than a load capacitance, which enables construction of a very small adiabatic regenerator. This regenerator cannot be made with a conventional circuit, which uses a tank capacitor that is much larger than a load capacitor for adiabatic charging.

Anti-islanding detection is essential for grid connected inverter to avoid substantial safety accident. Many Anti-islanding methods available now are proposed based on ideal grid and load conditions. Then most of them have weaknesses as high sensitivity to grid distortion in grid-connection state. This will certainly limit their wide application in some aspects. Active Frequency Drift (AFD) and Reactive power variation method (RPV) are two promising active anti-islanding detection methods. In this paper, the performance of these two methods under various extreme conditions are considered and compared, including different grid distortion conditions, different loading conditions.

This paper provides a classification of high efficiency switching power-gyrator structures and their use as cells for energy processing in photovoltaic solar facilities. Having into account the properties of these topologies presented in the article, their inclusion in solar facilities allows increasing the performance of the whole installation. Thus, the design, simulation and implementation of a G-type power gyrator are carried out throughout the text. In addition, in order to obtain the maximum power from the photovoltaic solar panel, a maximum power point tracking (MPPT) is mandatory in the energy processing path. Therefore, the practical implementation carried out includes a control loop of the power gyrator in order to track the aforementioned maximum power point of the photovoltaic solar panel.

Voltage instability is caused by the inability of the system to meet reactive power demand. The problem of voltage instability is even more critical for an isolated microgrid, which only has generators with limited reactive power capacities. In this paper, we investigated what happens if all generators in the system hit their reactive power limit. To simplify the analysis, a simple two-bus example was used. Analytical power flow solutions was derived, and the corresponding physical interpretation was discussed. The physical constraints of the generator determined whether the power flow solution is feasible. It was found that when the reactive power limit of the generators is hit, even though there is a power flow solution, due to the physical limitation of the generator, no feasible solution exists. This causes the system to experience voltage collapse.

Session B1P-L: Power Management Techniques II

Chair: Ayman Fayed, *Iowa State University*
Time: Tuesday, August 5, 2014, 9:20 - 10:10
Location: Poster Area

This article shows the proposal of a linear"assisted converter or linear"&"switching hybrid converter with a constant switching frequency. The control loop of the system is based on the current"mode technique. The main disadvantage of a converter with current"mode control is the inherent instability of the loop when switch duty ratios are greater than 0.5. In order to make stable the proposed linear"assisted converter, the article shows the technique based on a slope compensation.

Session B2L-A: References and Oscillators

Chair: Jin Liu, *University of Texas at Dallas*
Time: Tuesday, August 5, 2014, 10:10 - 11:50
Location: Mockingbird

Session B2L-B: Design and Analysis of Linear and Non-Linear Systems

Chair: Samuel Palermo, *Texas A&M University*
Time: Tuesday, August 5, 2014, 10:10 - 11:50
Location: Ballroom – 5

Session B2L-C: VLSI Design and Simulation

Chair: Nader Rafla, *Boise State University*
Time: Tuesday, August 5, 2014, 10:10 - 11:50
Location: North & South 40

We evaluate leakage currents of 6T and 8T FinFET SRAM cell schemes using shorted gate and low power FinFET configurations. Reverse-biasing the cross-coupled inverter FinFETs' back gates reduces leakage current by up to 97% and minimizes leakage variation due to parameter and temperature variations. The 6T Low-Power FinFET scheme uses these configurations and has lowest leakage; however, 8T SRAM schemes outperform 6T SRAM schemes since leakage can be reduced by schemes that reverse-bias the cross-coupled inverter FinFET back gates without reducing read speed or read static noise margin; the 8T Low-Power Inverters scheme has lowest leakage and energy-delay product.

The silicon-on-insulator (SOI) MOSFET is considered as an alternative to the bulk (silicon-based MOSFET in CMOS circuits for applications requiring low-voltage and low-power operation. Fully depleted SOI (FDSOI) benefits from a high current driven ability; so, this technology preserves advantageous features, such as steep sub threshold characteristics and small short channel effects. This paper presents a comprehensive assessment of different SRAM (Static Random Access Memory) cells utilizing different numbers of transistors (i.e. 8 and 9). These cells are evaluated by HSPICE for different performance metrics (such as write/read delay, stability, critical charge, power consumption and tolerance to voltage threshold variation) at the 22nm technology node

Session B2L-D: Devices and Circuits for Health Monitoring II

Chair: Marvin Onabajo, *Northeastern University*
Time: Tuesday, August 5, 2014, 10:10 - 11:50
Location: Ballroom – 6

In order to fight against severe risks of security and privacy for implantable medical devices, an on-chip security guard based on zero-power authentication is proposed and verified in this paper. The conception of ‘zero-power’ is realized by virtue of wireless power recovery instead of fetching power from primary battery. The security guard recovers both data and clock from external wireless signals based on amplitude shift keying pulse width modulation. It features a wireless data rate of 500 Kbps and no need for on-chip clock generator. The Hash encryption is adopted in authentication and features a 32-bit ALU to speed up the SHA-1 computation with an estimated peak power of about only 1 mW, which is affordable by wireless power recovery which has a capacity of several mW. FPGA and chip implementation verify the feasibility of this system.

This paper presents the design of a monolithic low power CMOS low-noise instrumentation amplifier (INA) for low-power biosensor applications. To achieve high-fidelity cardiac signal acquisition, the INA circuit and system design requirements are discussed. Design strategies for mitigating the in-band flicker noise and thermal noise using chopper-stabilization and current scaling techniques are investigated. Sub-threshold operation is also utilized to reduce power. The INA achieves a simulated noise spectral density of 39.9 nV/√Hz from dc to 300Hz in 4.6µW, with an outstanding noise efficiency factor (NEF) of 2.47.

An instrumentation amplifier with a mechanism that generates negative capacitances at its input is presented. The architecture includes two digitally programmable capacitors between the input stage and the current feedback loop to cancel the input capacitances from the electrode cables and printed circuit board. The negative capacitance generation technique can improve the input impedance from a few mega ohms to above 500MOhm without significant impact on performance parameters such as the common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), total harmonic distortion (THD), and noise. A 93.6uW instrumentation amplifier was designed and simulated using IBM 0.13um CMOS technology.

Session B2L-E: Reconfigurable RF-CAS for RADAR, Cognitive Radio and EARS – I

Chair: Arjuna Madanayake, *University of Akron*
Co-Chair: Changzhi Li, *Texas Tech University*
Time: Tuesday, August 5, 2014, 10:10 - 11:50
Location: Ballroom – 7

Session B2L-F: Continuous-Time Filters

Chair: Igor Filanovsky, *University of Alberta*
Time: Tuesday, August 5, 2014, 10:10 - 11:50
Location: Brazos

Session B3L-A: Delta-Sigma Techniques I

Chair: R. Jake Baker, *University of Nevada, Las Vegas*
Time: Tuesday, August 5, 2014, 13:10 - 14:50
Location: Mockingbird

Session B3L-B: RF Power Amplifiers

Chair: Kamran Entesari, *Texas A&M University*
Time: Tuesday, August 5, 2014, 13:10 - 14:50
Location: Ballroom – 5

Session B3L-C: Systems and Hardware/Software Co-Design

Chair: Zoran Stamenkovic, *IHP, Frankfurt*
Time: Tuesday, August 5, 2014, 13:10 - 14:50
Location: North & South 40

Session B3L-D: BioSignal Processing

Chair: Hoda S. Abdel-Aty-Zohdy, *Oakland University*
Co-Chair: Marvin Onabajo, *Northeastern University*
Time: Tuesday, August 5, 2014, 13:10 - 14:50
Location: Ballroom – 6

Session B3L-E: Circuits Tolerant to Radiation Effects

Chair: Ricardo Reis, *Universidade Federal do Rio Grande do Sul, Brazil*
Time: Tuesday, August 5, 2014, 13:10 - 14:50
Location: Ballroom – 7

Session B4P-G: Image Processing and Multimedia Systems III

Chair: Joseph Chang, *Nanyang Technological University, Singapore*
Time: Tuesday, August 5, 2014, 14:50 - 15:40
Location: Poster Area

An edge-detection scheme suitable for machine vision and digital motion detection applications is presented. The scheme is inspired by the human visual system (human retina) and modified for a compact and scalable CMOS hardware implementation. In addition, the pixel circuit and the implementation of the scheme on CMOS image sensor focal-plane are proposed and the simulation results are presented. The proposed acquisition technique and the corresponding CMOS circuit can easily be adjusted to various imaging applications and scaled towards new CMOS technology nodes and high resolution image sensors.

Session B4P-H: Digital Signal Processing II

Chair: Joseph Chang, *Nanyang Technological University, Singapore*
Time: Tuesday, August 5, 2014, 14:50 - 15:40
Location: Poster Area

Analysis of l2-sensitivity for two-dimensional (2-D) state-space digital filters is performed more precisely by taking into account 0 and ±1 elements. First, the improved version of an l2-sensitivity measure is developed for the Roessor local state-space model. Next, that of an l2-sensitivity measure is explored for the Fornasini-Marchesini second local state-space model. Finally, numerical examples are presented to evaluate the improved l2-sensitivity measures for the considered two local state-space models by means of the proposed methods.

The filtered-x least mean square (FxLMS) algorithm for active noise control (ANC) systems is based on the second order moment of the error signal. In this paper we consider ANC for impulsive noise having peaky distribution with heavy tail. Such impulsive noise can be modeled using non-Gaussian stable process for which the second order moments do not exist, and hence, the FxLMS algorithm becomes unstable. Recently, we have proposed variants of the FxLMS algorithm where an improved performance has been realized by thresholding the input data or by efficiently normalizing the step-size. In this paper, we propose a modified binormalized data-reusing (BNDR) algorithm for impulsive ANC. The proposed algorithm is derived by minimizing a modified cost function, and is based on reusing the past and present samples of data. The computer simulations are carried out to demonstrate the effectiveness of the proposed algorithm. It is shown that an improved performance has been realized with a reasonable increase in computational complexity.

In this paper, a new complex adaptive notch filters based on oscillator based algorithm has been proposed. The approach presented for secon-order real coefficient IIR filters has been applied to derive a coefficient-update agorithm for a first-order complex adaptive notch filter. Convergence characteristics of the proposed algorithm have been analyzed. Unbiased frequency estimation of a complex sinusoid has been achieved by thinning the notch bandwidth. Computer simulations show the effectiveness of the proposed algolithm.

This paper presents the applications of simple multiplierless filters to decrease the passband droop and to increase the alias rejection in the folding bands of comb filters. The comparisons with some methods proposed in the literature, are also included to show the benefit of the proposed approach. It is also shown that the method is convenient for the traditional non-recursive comb structure with the decimation factor which is the power of two. In that way the magnitude characteristic of the structure is significantly improved while keeping the power efficiency of the original structure, by placing three simple filters in last two stages.

Session B4P-J: Communication and Wireless Systems

Chair: Faramarz Bahmani, *Broadcom Co.*
Time: Tuesday, August 5, 2014, 14:50 - 15:40
Location: Poster Area

Session B4P-K: Neural Networks

Chair: Kamran Entesari, *Texas A&M University*
Time: Tuesday, August 5, 2014, 14:50 - 15:40
Location: Poster Area

Session B4P-L: VCOs and Frequency Synthesizers

Chair: Kamran Entesari, *Texas A&M University*
Time: Tuesday, August 5, 2014, 14:50 - 15:40
Location: Poster Area

Session B5L-A: Delta-Sigma Techniques II

Chair: R. Jake Baker, *University of Nevada, Las Vegas*
Time: Tuesday, August 5, 2014, 15:40 - 17:20
Location: Mockingbird

Session B5L-B: Switching and Linear Power Conversion Techniques

Chair: Ayman Fayed, *Iowa State University*
Co-Chair: Hoi Lee, *University of Texas, Dallas*
Time: Tuesday, August 5, 2014, 15:40 - 17:20
Location: Ballroom – 5

Ultra low duty-cycle clock signal is required in buck converters with large step-down voltage conversion ratio. Given the maximum achievable rise and fall time as well as the minimum ON time of the transistors, this sets a maximum limit on the operating frequency. Different buck converter architectures are proposed to achieve the same voltage conversion ratio with a larger duty cycle. Therefore, the constraints on the minimum transistor ON time and the maximum operating frequency are relaxed. The proposed converters are completely independent on mutual coupling and, as a consequence, they do not suffer from any leakage inductance and do not need any protection or clipping circuits. The analysis produces the relation between the duty-cycle and the voltage gain and shows how much the enhancements are.

An adaptive feed-forward power supply noise cancellation technique for low-dropout regulator (LDR) which requires no switches is proposed in this paper. By utilizing replica, transconductances (gm , gds) of the large pass transistor are linearly reproduced to construct a load-current-depedent ratioed feed-forward path from supply to gate of pass transistor. The power supply rejection (PSR) capability is enhanced by adaptively feeding compensation charging current to gate parasitic capacitor of the pass transistor, which is effective in a wide load range. The idea of the PSR enhancement technique is implemented in an output capacitor-less LDR in a standard 65-nm CMOS process. The total on-chip capacitance for compensation and low-pass filtering is 40pF. The output is 1.0V and delivers a maximum current of 50mA at 200mV drop-out. Simulations verify that the PSR is further enhanced in mid-frequency range (~100kHz"10MHz) compared with conventional techniques, without feed-forward ratio selection via switches, and it generates ignorable effects on stability and 200-ns full load transient response.

A new control strategy for Power Factor Correction (PFC) rectifier which has double-line frequency ripple decoupling capability is presented and experimentally implemented. Based on the commonly used Boost PFC regulator, an integrated non-cascading ripple-port on the DC-side completely filters the double-line frequency ripple. Hence, the output capacitance required is significantly reduced and high reliability film capacitors can be used to replace the bulky, low reliability electrolytic ones. The proposed control scheme for the ripple-port guarantees the ripple cancellation under various load conditions. Furthermore, comparing to conventional PFC rectifier, the proposed rectifier has improved transient response to load dynamics.

Session B5L-C: Digital Signal Processing I

Chair: Ricardo Reis, *Universidade Federal do Rio Grande do Sul, Brazil*
Co-Chair: Majid Ahmadi, *U of Windsor*
Time: Tuesday, August 5, 2014, 15:40 - 17:20
Location: North & South 40

Joint optimization of high-order error-feedback and state-space realization to minimize roundoff noise at the output of a closed-loop system with a state-estimate feedback controller subject to l_2-scaling constraints is investigated. The problem is converted into an unconstrained optimization problem by using linear-algebraic techniques. The unconstrained optimization problem at hand is then solved iteratively by employing an efficient quasi-Newton algorithm with closed-form formulas for key gradient evaluation. Analytical details are given as to how the proposed technique can be applied to the case where high-order error-feedback matrices are diagonal. A numerical example is presented to illustrate the utility of the proposed technique.

This paper proposes an adaptive bilinear filter with a diagonal-channel structure for nonlinear active noise control. Based on the diagonal-channel structure, the diagonal-channel bilinear filtered-X least mean square (DBFXLMS) and recursive least square (DBFXRLS) algorithms are derived. In order to reduce the computational load for the DBFXRLS algorithm, the DBFXRLS algorithm with a sequential channel update (DBFXRLS-SEQ) is proposed. Computational complexity for each algorithm is examined. Computer simulations demonstrate the control performance improvement using the proposed algorithms.

We propose a new efficient design algorithm to synthesize low complexity FIR filters, which has been applied to EEG signals feature extraction filter bank. A prudently defined bit-level frequency response sensitivity function is designed as a measure for the quantization decision making. Common subexpressions sharing is maximized with instant checking and updating of common subepxressions statistics. By this new algorithm, the filter coefficients are quantized into optimal patterns. The effectiveness of the proposed algorithm is demonstrated using two design examples where the solution saves about 82.6% and 48.5% of hardware complexity over the baseline implementation and other competing methods.

This paper presents a comb-based nonrecursive decimation structure with improved magnitude characteristics, where the decimation factor M is a power of two. A rotated cosine filter is introduced to increase the attenuation in the folding bands. Additionally, the passband droop is decreased by using a simple multiplierless compensation filter which works at low rate. The multiplierless rotated term is also introduced. The method is illustrated with examples and the comparisons with other methods are provided.

In this paper, a copy-move image forgery detection scheme is developed based on a block matching algorithm. Instead of considering spatial blocks, 2D-DWT is performed on the forged image and then DWT domain blocks are considered, where only approximate DWT coefficients are utilized. In order to reduce the computational burden, unlike conventional approaches, instead of performing block matching operation among all blocks, some candidate blocks are first selected from the non-overlapping blocks based on a similarity measure. In the next stage, all overlapping blocks are compared with the candidate blocks. A similarity criterion is introduced to finally detect the forged blocks. Extensive simulation is carried out on several forged images and it is found that proposed algorithm can efficiently detect copy-move forgery.

Session B5L-D: Image Processing and Multimedia Systems II

Chair: Moataz Abdelwahab, *Alexandria Academy*
Time: Tuesday, August 5, 2014, 15:40 - 17:20
Location: Ballroom – 6

In this paper a human action recognition algorithm based on two-view of optical flow in multiple layers per camera employing the transform domain and 2DPCA is presented. This method explores more distinctive features between actions. It is not sensitive to translation, alignment and noise. In addition the use of 2DPCA maintains the spatial relation between pixels and increases the recognition accuracy. Experimental results performed on the Weizmann action and the INIRIA IXMAS datasets confirm these excellent properties compared to recent reported methods.

In this work, we investigate the problem of estimating time-varying noise distribution parameter on a factor graph. A new message passing scheme is proposed by incorporating the variational Bayes (VB) into the belief propagation algorithm for estimating of time-varying noise distribution parameter in a low-density parity-check decoder. The scheme can also be used for the estimation of correlation noise model parameter in distributed video coding. A Bayesian estimator is used to estimate this parameter by obtaining its posterior distribution given the channel output. The VB algorithm is employed to approximate the complex form of the posterior distribution with a simple distribution. Finally, this distribution is used to derive a closed form expression for the messages on the augmented factor graph for online parameter estimation and decoding process at the same time.

Session B5L-E: Printed Electronics and Electronics for Space

Chair: Joseph Chang, *Nanyang Technological University, Singapore*
Co-Chair: Ge Tong, *Nanyang Technological University, Singapore*
Time: Tuesday, August 5, 2014, 15:40 - 17:20
Location: Ballroom – 7

Wednesday, August 6, 2014

Session C1P-G: Data Converters

Chair: R. Jake Baker, *University of Nevada, Las Vegas*
Time: Wednesday, August 6, 2014, 9:20 - 10:10
Location: Poster Area

Session C1P-H: Methodologies for Biomedical Signal Processing

Chair: Hoda S. Abdel-Aty-Zohdy, *Oakland University*
Time: Wednesday, August 6, 2014, 9:20 - 10:10
Location: Poster Area

This paper introduces an enhanced Genetic Algorithm GA that is faster and more efficient than the standard one. A simple 3D convex surface is optimized using different methods, Brute-Force, standard GA, and the enhanced GA. The enhanced GA is able to find the global minima within a certain range by using the least possible number of calculations which, means less processing time and is robust to parameter selections. Special software was developed using Java for this purpose; also MS-Excel was used to represent the data map as charts.

Session C1P-J: Circuits for Processing Biomedical Signals

Chair: Hoda S. Abdel-Aty-Zohdy, *Oakland University*
Time: Wednesday, August 6, 2014, 9:20 - 10:10
Location: Poster Area

In this paper, a low-noise CMOS readout front end for MEMS biopotential acquisition applications is presented. The proposed circuit, implemented using 130 nm standard CMOS process, has a thermal noise floor of 10 nV/√Hz, a corner frequency of 300 mHz, and dissipates 3.2µW of power when powered using a 1 V supply. The designed circuit occupies a die area of 0.007mm2 and thus renders itself as an excellent candidate for acquiring biopotential signals through MEMs sensors.

This paper presented a novel IntraBody Communication Receiver Front End (RFE) based on switched capacitor filter scheme and proposed sampling rate boosting technique. New technique aims to increase the oversampling ratio without rising system clock frequency to enhance the transmission performance. In this work, specifically, sampling rate is boosted 4 times with 50MHz system clock, which can reach 200MHz sampling frequency. Based on the measurement result, proposed RFE achieves a 2.5Mb/s data rate upon RZ coding, 170cm transmission distance and 4.14mW power. Measurement results demonstrate the effectiveness of proposed technique and its advantages compared to other conventional receiver front end circuits.

This paper presents a 128.7nW analog front-end amplifier and Gm-C filter for biomedical sensing applications, specifically for Electroencephalogram (EEG) use. The proposed neural amplifier has a supply voltage of 1.8V, consumes a total current of 71.59nA, for a total dissipated power of 128nW and has a gain of 40dB. Also, a 3th order Butterworth Low Pass Gm-C Filter with a 14.7nS transconductor is designed and presented. The filter has a pass band suitable for use in EEG (1-100Hz). The amplifier and filter utilize current sources without resistance which provide 56nA and (1.154nA x5) respectively. The proposed amplifier occupies and area of 0.26mm2 in 0.3µm TSMC process.

a low power, low noise implantable neural recording interface for use in a Radio-Frequency Identification (RFID) is presented in this paper. A two stage neural amplifier, selective reference thresholder and a serial peripheral interface for communication are integrated in this system. The midband gain of neural amplifier is 59.1dB with a 3dB bandwidth from 0.45 to 8 kHz. Input-referred noise and total power consumption are 8.7µVrms and 3.19 µW respectively. The thresholder detects the output signal at sampling rate of 20 kHz with four different references and the digital output is sent out through transmitter to drive light emitting diode (LED). The chip is designed and fabricated in 0.18-µm process. The simulation result demonstrates the neural recording interface's suitability for instu neutral activity recording.

Session C1P-K: Nanoscale Digital VLSI Design I

Chair: Yong-Bin Kim, *Northeastern University*
Time: Wednesday, August 6, 2014, 9:20 - 10:10
Location: Poster Area

For many image processing systems, the computing power required can not be provided by a single sequential processor, this is why many designers appeal to multiprocessor systems (parallelism). This article proposes an original flexible MP-SoC (Multi-Processors System on Chip) architecture for image processing applications. Developing processors network systems tailored to a particular application domain is critical and design-time consuming in order to achieve high-performance customized solutions. This paper introduces a 16-core MP-SoC ASIC with a software configuration. In particular, each tile of the network can configure its communication links depending on the most relevant overall parallelism scheme for a targeted application. Results are shown in term of power, area and timing performance for a 65 nm CMOS technology ASIC design. A case study (grey scale histogram analyzes) is presented to illustrate the proposed flexible MP-SoC design methodology and enables to focus on architecture exploration, instantiated scheme of parallelization and timing performance.

This paper investigates the performance of array multipliers utilizing FinFET models for the following feature sizes: 20nm, 16nm, 14nm, 10nm and 7nm. Using basic array multiplier topology and standard cell 28 transistor full adders, the static power and delay of FinFET array multiplier circuits were investigated using HSPICE and low power Predictive Technology Models (PTM). Simulation results show an increase in static power and a decrease in delay as the feature size decreases. Comparisons between array multiplier sizes show nonlinear increases in both static power and delay as size increases from 4x4 up to 16x16. The results obtained in this research will provide a starting point for the design and analysis of more complex FinFET based arithmetic circuit designs.

Session C1P-L: Nanoscale Digital VLSI Design II

Chair: Carlos Silva Cardenas, *Pontificia Universidad Católica del Peru*
Time: Wednesday, August 6, 2014, 9:20 - 10:10
Location: Poster Area

In this paper, we analyze and compare five different low-power SRAM cell topologies in terms of their data retention voltages (DRV). The circuit simulation and analysis was carried out using HSPICE with the 45 nm, 32 nm, and 22 nm low-power Predictive Technology Model (PTM) transistor models by setting the SRAM cells to an initial state and bringing the supply voltage down to several different standby voltages. Based on these results, the standard 6T SRAM cell provides the lowest DRV out of all of the SRAM cells in this study at the 45 nm and 32 nm process nodes, but the 7T, 8T, and 10T SRAM cells provide better DRV performance at the 22 nm process node. These results give a first look at the effects that SRAM cell topology can have on DRV, and provide a starting point for future research into this topic.

In this paper, multiple full adder circuits have been implemented using the FinFET device described by the BSIMCMG model. A variety of adders have been selected to compare the impact of this technology and evaluate the performance advantages that can be achieved. Full adder designs tested in this work include 28 transistor mirror adder, 10 transistor complementary and level restoring carry logic adder and ultra low power full adder (ULPFA) architectures which cover a broad spectrum of adder designs. Comprehensive simulation results demonstrate FinFET transistors' advantage in key design metrics, including reduced dynamic power, leakage current and delay. Overall, PDP gains of up to 83% is observed when compared to conventional CMOS circuits. However, FinFET pass-transistor circuits without level restorers are shown to be more vulnerable to voltage degradation compared to CMOS counterparts.

This paper presents a power consumption optimization methodology (PCOM) for low-power/ low-voltage single-cycle microprocessor circuit design via multi-threshold CMOS (MTCMOS) techniques. Based on the optimization methodology with the dual-threshold techniques, a 32-bit single-cycle MIPS microprocessor design has been optimized in terms of circuit design using dual-threshold HVT/SVT CMOS devices. According to SPICE simulation results, the power consumption of the 80,000-transistor 32-bit MIPS microprocessor, using a 90nm CMOS technology and operating at 1V with a 0.9-ns clock period, based on the optimization methodology with the dual-threshold technique, has been reduced by 27.23% during the standby period and 12.53% during the dynamic switching period as compared to the one using the conventional standard-threshold SVT CMOS devices.

Power consumption is an important aspect of almost any electrical device design. Near-Threshold Computing (NTC) is a voltage scaling technique that makes it possible to reduce the power consumption of CMOS devices with the cost of speed and reliability. We are using NTC to design low-power cache memory circuit for a low-performance sensor-based system. Caches consume noteworthy portions of power and area of this kind of systems, and therefore reducing their power consumption has a meaningful impact on the overall power consumption of the whole system. In this paper, 8T SRAM and 6T SRAM memory cells are compared in order to establish guidelines for choosing SRAM cell constructions for NTC systems. 8T SRAM is traditionally concerned as a more reliable memory cell, but we have managed to design 6T SRAM which executes read operation with an acceptaple reliability; read being the most vulnerable operation of conventional 6T SRAM cell. Also, our 6T SRAM cell has 31% smaller area and smaller power consumption.

Aggressive CMOS technology scaling trends exacerbate the aging-related degradation of propagation delay and energy efficiency in nanoscale designs. Recently, Power-gating has been utilized as an effective low-power design technique which has also been shown to alleviate some aging impacts. However, the use of MOSFETs to realize power-gated designs will also encounter aging-induced degradations in the sleep transistors themselves which necessitates the exploration of design strategies to utilize power-gating effectively to mitigate aging. In particular, Bias Temperature Instability (BTI) which occurs during activation of power-gated voltage islands is investigated with respect to the placement of the sleep transistor in the header or footer as well as the impact of ungated input transitions on interfacial trapping. Results indicate the effectiveness of power-gating on NBTI/PBTI phenomena and propose a preferred sleep transistor configuration for maximizing higher recovery.

Session C2L-A: Sensors

Chair: Jin Liu, *University of Texas at Dallas*
Time: Wednesday, August 6, 2014, 10:10 - 11:50
Location: Mockingbird

The technique of maximizing image sharpness is a powerful means of adaptively correcting phase aberrations in wavefronts. Crucial to this correction is a sensor that provides an accurate real-time estimate of image sharpness. In this paper, we introduce a novel image sharpness sensor using CMOS active pixel technology that computes image sharpness at a sample rate of 7.8 kHz. The sharpness sensor contains a 40x40 pixel array and is fabricated in a 0.5-um CMOS process through MOSIS. Power consumption is 12 mW. Each pixel is 24.5 x 24.5 um2 with a fill factor of 20%. Experimental results obtained under open-loop static conditions show that the output value changes by 87.5% when the sensor is moved 1 cm away from the 50-cm focal point. This sensor finds potential applications in closed-loop adaptive optics systems.

Conventional centroid architectures employ an image sensor sampled at high frame rates, analog-to-digital conversion, and digital signal processing to compute the image centroid. Latency and/or power dissipation may become prohibitively large. Therefore, fast single-chip centroid computation circuits are gaining importance in adaptive optics applications. To this end we present a fully-integrated centroid computation sensor with improved bandwidth using a transimpedance amplifier with a novel adaptive pole tracking technique. The circuit is designed to operate over five orders of magnitude of light intensity. The outputs are two signals representing the (x, y) centroid coordinates. A 48x48 pixel array was fabricated in a 0.5-um CMOS process. Chip measurements verify a bandwidth improvement of 6 times. The supply is 1.8 V, total power consumption is 2.16 mW, and core area is 2.18 mm2.

We present the design and analysis of an analog CMOS image sensor as an improvement to the design presented in previous work. The current sensing and amplification is implemented using a current amplifier utilizing symmetric current mirrors which improves the bandwidth and hence the readout speed of the image sensor. In addition, faster settling time reduces the 1/f noise introduced by the in-pixel source-follower transistor of active pixel sensors with the help of the CDS circuit. We demonstrate a speed improvement of five times over the standard APS design for a current amplifier gain of five.

A high-accuracy CMOS interface for differential capacitive sensors using a time-to-digital converter (TDC) is presented for high-accuracy ratiometric operation. A capacitance-to-time converter (CTC) is developed based on a switched-capacitor (SC) sample/hold (S/H) circuit and an integrator. The proposed TDC achieves high resolution without using higher frequency clock signals. The Performances of the proposed CMOS interface are simulated by HSPICE. Simulated results have demonstrated that the proposed interface can convert the difference-to-sum ratio of sensor capacitors to digital numbers. The resolutions of 11.3 bits are achieved with calibration. The maximum nonlinear errors are smaller than 0.55 LSB. A prototype circuit built using discrete components has confirmed the principles of operation.

A test signal generator to calibrate analog front-ends for biopotential measurements is presented. The integrated signal generator enables detection of the input impedance at the front-end instrumentation amplifier based on current injection and amplitude detection. It can generate picoampere currents while ensuring a high output impedance of 2.9 gigaohms up to 100 Hz. The test signal generator was designed and simulated in 0.13um CMOS technology and it consists of a temperature-compensated relaxation oscillator, a frequency divider, a limiter, and an operational transconductance amplifier.

Session C2L-B: RF LNAs and TIAs

Chair: Kamran Entesari, *Texas A&M University*
Time: Wednesday, August 6, 2014, 10:10 - 11:50
Location: Ballroom – 5

An inductorless wide band LNA is designed with low NF and high linearity. It is based on the use of both the passive and active feedback with current reuse techniques to achieve the required low NF, high BW, and suitable gain. An auxiliary transistor is added to the differential implementation to achieve a high linearity. The circuit is designed in 0.13µm TSMC technology and exhibits a gain of 18.4dB over an entire bandwidth of 6.6GHz. Across the whole band of interest, the NF does not exceed 3dB, while the IIP3 is maintained above 6dBm, and it consumes 13.4mW DC power from a 1.5V supply.

A transimpedace amplifier (TIA) for optical links with data-rate (DR) of up to 30Gbps, realized in a 28nm CMOS technology is presented. The design uses several bandwidth and gain enhancement techniques such as regulated common-gate, transimpedance boosting by current injection, transimpedance/transadmittance feedback and active inductor. The measured bandwidth is 22GHz with a power consumption of only 2mW, achieving a 0.067pJ/bit energy efficiency. The gain of the TIA is approximately 43dBΩ with only one stage. No passive planar inductors are used, therefore the area is only 0.0004mm2 and is to our knowledge the smallest TIA reported to date in the 30Gbps DR range.

The growing demand for high-speed communication necessitates high-data-rate and power- efficient integrated optical link solutions. In this paper, a power-efficient CMOS transimpedance amplifier (TIA) is proposed which uses current-reuse and inductive-peaking techniques to achieve a wide bandwidth, a low input impedance, and a high gain. As a proof-of-concept, a DC-to-27-GHz TIA is designed and laid out in a 0.13-µm CMOS process. Post-layout simulation results show that in the presence of a photo diode with a capacitance as large as 500 fF, the TIA achieves a 3-dB bandwidth of 27.3 GHz and a gain of 50 dBΩ while consuming 14.3 mW from a 1.2-V supply.

We present the design and characterization of a broadband, low-noise transimpedance amplifier (TIA) with adjustable gain-peaking, implemented in 65-nm CMOS. The TIA exhibits 40-GHz bandwidth, 20-dB gain and consumes 107 mW power. An additional continuously-tunable 12-dB gain-peaking near 40 GHz is available through a simple yet effective tuning mechanism, consuming only 14% more power. The adjustable gain-peaking functionality incorporated in the TIA can potentially reduce power consumption and complexity of an optical receiver and is highly desirable for adaptively-equalized receiver architectures. 50 Gb/s operation is demonstrated electrically as well as in an optical testbed. A low input-referred noise current of 2.5 uArms is achieved, suggesting an average optical power sensitivity of -14.6 dBm with a 0.5 A/W PD.

Session C2L-C: Low-Power Wireless Circuits

Chair: Fan Xiaohua, *Institute of Microelectronics of Chinese Academy of Sciences*
Co-Chair: Bo Xia, *Feeltel Corporation*
Time: Wednesday, August 6, 2014, 10:10 - 11:50
Location: North & South 40

In this paper, a power reduction technique for wideband common gate low noise amplifiers (LNA) is proposed for low power application. Stacked current reused complementary capacitive cross coupling (CCCC) concept is proposed to improve LNA power efficiency. As a proof of the concept, the improved broadband differential common-gate LNAs (CG-LNA) designed in 0.18μm CMOS technology. The LNA achieves a 21.2dB peak voltage gain over 3dB bandwidth from 53MHz - 3.3GHz, 2.95dB minimum noise figure (NF) and -2.2dBm IIP3. The current consumption of the LNA core from 1.8V supply is 368uA.

The ever increasing dynamic range requirement for the RX path and maximum transmission power requirement for the TX path add difficulty in the Bluetooth transceiver design. The tradeoff between noise and linearity performance is carefully examined to meet the RX dynamic range requirement. RX anti-interference performance is improved by careful system level planning. TX non-idealities are addressed in design to achieve large usable output power. A transceiver with -92dBm sensitivity and 9dBm maximum TX power is implemented following the proposed methodology.

We propose an RF channelizer architecture that uses the concept of 3-way Iterative Down-Conversion (IDC) to channelize a wideband incident spectrum while only using a fixed LO synthesizer. The proposed architecture can realize a concurrent channelizer that can analyze channels simultaneously, or a fast-switching channelizer that can analyze channels sequentially but with very short switching times between channels. We present an RF channelizer demonstrator prototype that was fabricated in a 65nm CMOS process. It implements a partially-concurrent architecture with the ability to concurrently down-convert a subset of channels while being able to switch very quickly between the non-concurrent channels. It splits an input spectrum of 0.6GHz-9GHz into 7 channels each of 1.2GHz bandwidth. Channelizer performance depends on the selected operation mode. The measured channel switching duration can be as fast as 8ns, and is always under 1μs. The chip occupies an area of 2mm x 1mm and consumes an average power of 435mW while offering a dynamic range between 58dB to 63dB based on noise and linearity performance.

The research presented focuses on implementation of RF digital predistorters using polynomial optimization techniques. By representing the system with a set of two polynomials, we have been able to apply algebraic techniques resulting in reduction in cost of implementing digital predistorters. To test this approach we have used model of a communication channel using traveling wave tube amplifier and we have compared our method with the direct and buffered evaluation of Volterra series representing this system. Our design decreases the number of multiplications by 35% and the number of adders by 12.9% in comparison with the best technique previously used. The FPGA implementation also demonstrated decrease of 29% in DSP usage and decrease of 71.5% in logic blocks. We saw an increase of 30% in speed comparing to the previous attempts due to smaller bit-width operations and lower routing complexity of our optimized solution.

Session C2L-D: Nanoelectronics and Neural Networks

Chair: Rashmi Jha, *University of Toledo*
Time: Wednesday, August 6, 2014, 10:10 - 11:50
Location: Ballroom – 6

For flash memory devices the thicknesses of the control and tunneling oxides in the floating gate transistor (FGT) are crtical parameters. We recently proposed a floating gate transstor using multilayer graphene nanoribbon (MLGNR) and carbon nanotube (CNT). In this paper, we have analyzed the impacts of scaling the thickness of the control and tunneling oxides in the proposed MLGNR/CNT based FGT. According to ITRS, semiconductor industry has already adopted 6nm thick tunneling oxide for 18-nm and 22-nm technology nodes. By 2020, technology is expected to move to 10nm node, and 5nm tunnel oxide is predicted for 8nm-14nm nodes. For less than 20nm technology nodes, ultra-thin tunnel oxide would lead to higher tunneling current density that will affect the reliability of the flash memory cell. Based on our analysis we have provided some recommendations about the scaling of oxide thickness in the proposed MLGNR/CNT floating gate transistor.

This paper presents a simulation-based study to understand the impact of coupling capacitance on the read operation of nanoscale RRAM devices in 1D1R crossbar memory architectures. Our simulation results show that the coupling capacitances can form additional sneak paths which can lead to RRAM HRS read failure. Increase in the coupling capacitance increases the transient charging current when an ultra-fast read pulse is used for the read operation. The transient charging current causes temporal reduction in LRS:HRS read current ratio which puts a limit on the read speed. This issue can be alleviated by using larger read pulses, however, this comes at the cost of higher read energy. Finally, the signature of coupling capacitance becomes more severe as the size of the crossbar increase.

This paper proposes a new macromodel that takes into account the threshold switching and the resistance recovery processes in addition to the drift behavior of a Phase Change Memory (PCM). Simulation results are provided for both DC and drift behaviors; they show that the proposed macromodel is very accurate at a small error when compared with data from experimental devices. A sensitivity analysis of the macromodel is also performed to show its operation with respect to parameter variations. The model is suitable for circuit design based on PCM devices.

Catastrophic forgetting is a well studied problem in artificial neural networks in which past representations are rapidly lost as new representations are constructed. We hypothesize that such forgetting occurs due to overlap in the hidden layers, as well as the global nature in which neurons encode information. We introduce a novel technique to mitigate forgetting which effectively minimizes activation overlapping by using online clustering to effectively select neurons in the feedforward and back-propagation phases. We demonstrate the memory retention properties of the proposed scheme using the MNIST digit recognition data set.

Session C2L-E: Surviving Challenges in Design Automation

Chair: Peng Li, *Texas A&M University*
Co-Chair: Esteban Tlelo-Cuautle, *Institute for Astrophysics, Optics and Electronics*
Time: Wednesday, August 6, 2014, 10:10 - 11:50
Location: Ballroom – 7

Session C3L-A: Filters

Chair: Ayman Fayed, *Iowa State University*
Co-Chair: Wei Fu, *Iowa State University*
Time: Wednesday, August 6, 2014, 13:10 - 14:50
Location: Mockingbird

Session C3L-B: Design Techniques for ADCs

Chair: Vishal Saxena, *Boise State University*
Time: Wednesday, August 6, 2014, 13:10 - 14:50
Location: Ballroom – 5

An approach towards a high speed current mode SAR ADC is presented. Even though SAR ADCs based on charge redistribution have been significantly improved in efficiency and operating frequency, they are still limited by the settling requirements of the switched capacitor DAC. To overcome this limitation, we propose the use of a current mode SAR ADC incorporating a current steering DAC operating at 2 GS/s and an overall Nyquist rate conversion speed of 200 MS/s. In this paper, the main focus is placed on the design of a high-resolution low-input-impedance transimpedance amplifier (TIA) used as the comparator preamplifier in the proposed current mode SAR ADC. For high-speed operation, trade-offs between input resistance, noise and voltage headroom pose challenges in the design of the high-speed TIA. Our analysis is compared against a schematic level implementation in a 1.2 /1.8 V 90 nm CMOS technology. The TIA implementation is simulated on transistor level to achieve an overall resolution of 10 bit in the proposed current based SAR ADC together with the input Gm and current steering DAC over a Nyquist band from DC to 100 MHz.

As device dimensions and supply voltage are shrinking, the design of high-speed and high-resolution analog-to-digital converters (ADCs) is getting more and more challenging. Since the shrinking device sizes enable high-speed and low-power digital circuits, there has been a trend to use digital circuits to estimate and correct for the analog circuit nonidealities (i.e. calibrate) to realize high-performance ADCs. This summary paper enumerates some of the digital techniques that have been adopted in the past two decades to realize high-speed high-resolution pipelined ADCs, which are typically used in communication and imaging applications.

Session C3L-C: On-Chip Built-In Test and Self-Calibration Techniques

Chair: Marvin Onabajo, *Northeastern University*
Co-Chair: Yong-Bin Kim, *Northeastern University*
Time: Wednesday, August 6, 2014, 13:10 - 14:50
Location: North & South 40

Due to the proliferation of nanometer CMOS mixed-signal/RF circuits and a push towards high operating speeds (5-100 Ghz+), there has been renewed interest in the design of high-speed circuits and systems that can self-calibrate and self-heal post-manufacture and in the field. In the past, designers have invented self-healing mechanisms that are tailored towards specific (critical) mixed-signal/RF performance metrics of specific circuit architectures (transmitter, receiver, etc). What is desired, however, is the ability to monitor multiple performance metrics concurrently and trade them off against one another in an optimal manner, through performance tuning mechanisms, to satisfy system-level Quality of Service (QoS) guarantees. Further, the methods employed must be scalable across different device types/circuit architectures and supported by CAD tools that enable automation of self-healing design procedures. In this paper, recent research advances are presented that allow low cost and rapid self-healing of complex mixed-signal/RF systems and enable the development of design automation tools to support such activity across diverse performance metrics and circuit types.

In this paper we describe a novel Built-in-Self-Test (BIST) method using a voltage comparator to detect gate-oxide and drain leakage current for LDMOS by applying a pulse test stimulus. A temperature calibration circuit was also designed for LDMOS-based motor drivers.

Advance in technology nodes of IC fabrication has introduced increased variation. This presents new challenges for delay testing. To address this challenge, speed-binning based on on-chip delay sensor measurements has been proposed as alternative to current speed-binning methods. This practice requires advanced data analysis techniques for the binning result to be accurate. In this paper, based on experiments with silicon data collected from on-chip delay sensors in a commercial design using sub-65 nm process, we demonstrate that optimizing sensor selection can benefit speed-binning accuracy. An optimization algorithm is presented, and result showed it is capable of improving accuracy beyond 93\%.

Session C3L-D: Speech Processing

Chair: Genevieve sapijaszko, *UCF/Devry*
Co-Chair: Waleed Alrasheed, *King Fahd U Saudi Arabia*
Time: Wednesday, August 6, 2014, 13:10 - 14:50
Location: Ballroom – 6

This paper proposes a feature extraction scheme for speaker"independent Speech Emotion Recognition. The feature is derived from the Teager energy operated wavelet coefficients of speech . The wavelet coefficients thus enhanced is used to compute entropy. The feature vector is fed to unsupervised K-means clustering in a nonhierarchical process and is then used in a supervised KNN classifier. It is seen that KNN classifier is more capable of distinguishing emotions when a hierarchical approach is followed. Detail simulations using EMO-DB German speech emotion database show that the proposed feature with supervised hierarchical classification approach provides the higher accuracy.

Session C3L-E: Energy Efficient System Solutions

Chair: Neeraj Magotra, *Energy Efficient System Solutions*
Time: Wednesday, August 6, 2014, 13:10 - 14:50
Location: Ballroom – 7

This paper is a concise overview of current low power hearing aid DSP architectures

A novel design of a proportional"integral"differential equivalent controller using state observer based Extended Kalman Filter (EKF) for a Permanent Magnet Synchronous Motor (PMSM) is proposed. The EKF is constructed to achieve a precise estimation of the speed and current from the noisy measurement. Linear Quadratic Regulator (LQR) technique is used to construct a proportional integral derivative (PID) controller to achieve the speed command tracking performance. The proposed method greatly enhances the speed control performance. The simulation results for the speed response and variation of the states when the PMSM is subjected to the load disturbance are presented. The results verify the effectiveness of the proposed method.

This paper focuses on design issues related to the development of an energy efficient Digital Signal Processing (DSP) hearing aid system that can result in various DSP hearing aid products. The approach is predicated on utilizing commercially available DSP chips while meeting system requirements and end-user expectations. It describes how energy efficiency can be achieved at various levels, designing and tailoring the necessary algorithms to consume less power, selecting appropriate components with a focus on functionality " satisfying end-user expectations. The approach has led to the development of binaural DSP hearing aids in various form factors.

Advance Driver Assistance Systems (ADAS), once limited to high end luxury automobiles are fast becoming popular with Mid and entry level segments driven in part by legislation coming in to effect in the latter part of this decade. These systems require support for a wide variety of applications, from surround-view visual systems to safety critical vision applications (eg Pedestrian Detect, automatic braking etc). In this white paper we describe some of the existing and emerging trends and applications in each of these segments along with the requirements and motivations for each of these features. We also highlight TI's automotive class TDA2x device, a state of the art automotive grade device capable of handling complex ADAS applications within a low power and cost budget.