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# TABLE OF CONTENTS

Monday, August 4, 2014

## Session A1L-A: Nyquist-Rate Data Converters I

**Chair:** R. Jake Baker, *University of Nevada, Las Vegas*

**Time:** Monday, August 4, 2014, 10:10 - 11:50

**Location:** Mockingbird

### **Calibration Technique Tracking Temperature for Current-Steering Digital-to-Analog Converters** ..... 1

*Haiyang Zhu (Analog Devices, Inc.), Wenhua Yang (Analog Devices, Inc.), Nathan Egan (Analog Devices, Inc.), Yong-Bin Kim (Northeastern University)*

In this paper, a novel foreground calibration technique is presented for current-steering DACs. Each current source is in parallel with a CAL DAC injecting a small correction current that corrects the mismatch and tracks the temperature variations. High matching accuracy is not only achieved at the calibration temperature, but also maintained across a wide operating temperature range from -40° to 120° Celsius. A 14-bit DAC is designed in a standard 65nm CMOS process to verify the concept. The transistor level simulation results show that the new calibration technique reduces the worst case INL and DNL of the DAC across the whole temperature range by a factor of 15.7 and 12.8 compared with the intrinsic matching and by a factor of 2.9 and 2.8 compared with the conventional calibration method. The DAC achieves real 14-bit level INL and DNL across a wide temperature range with only 10-bit level raw matching.

### **A Novel Self-Calibration Scheme for 12-Bit 50MS/s SAR ADC** ..... 5

*In-Seok Jung (Northeastern University), Yong-Bin Kim (Northeastern University)*

This paper presents a low-power 12-bit 50MS/s successive approximation register (SAR) analog-to-digital converter (ADC) using single input condition for Built-In Self Test (BIST) that uses a novel self-calibration scheme to reduce both offset voltage of a comparator and capacitor mismatch of the DAC. The proposed self-calibration scheme changes the offset voltage of the comparator continuously for every step to decide one-bit code. The changed offset voltage of the comparator is able to cancel not only inherent offset voltage of the comparator but also the mismatch of DAC. Consequently, the total mismatch error of both the comparator and capacitor of DAC can be reduced.

### **A 10 Bit Cryogenic CMOS D/A Converter** ..... 9

*Md Tanvir Rahman (University of New South Wales), Torsten Lehmann (University of New South Wales)*

A 10 bit cryogenic current steering D/A converter (DAC), operating from room temperature to as low as 4.2K temperature, is presented here. The converter is primarily designed for a Silicon (Si) quantum computer controller circuit for initializing quantum bits (qubits). A new analog calibration method with an on chip reference current generator is applied to all the bits of the converter to overcome the nonlinearity and mismatch errors of the current sources in low temperature. The converter drives a 50 ohm load to 0.5V while its average power consumption is about 32mW from a 3V power supply. The cryogenic DAC's differential nonlinearity (DNL) is plus minus 0.27 LSB and integral nonlinearity (INL) remains within -0.49 and 0.41 LSB. The complete system is designed, simulated and laid out using a commercial standard 0.5 micro meter Silicon-on-Sapphire (SOS) CMOS process.

### **A 15B, Sub-10ps Resolution, Low Dead Time, Wide Range Two-Stage TDC** ..... 13

*Noble Narku-Tetteh (Texas A&M University), Alex Titriku (Texas A&M University), Samuel Palermo (Texas A&M University)*

A coarse-fine hierarchical time-to-digital converter (TDC) utilizes two looped structures to achieve a wide dynamic range with high resolution and minimal dead time. The coarse stage consists of a looped TDC, a counter, and a novel counter clock control scheme which allows for indefinite range extension, while the fine stage employs a Vernier delay loop with a new edge-sensitive pulse-generator-based delay element that reduces loop non-linearity associated with mismatched rise/fall times. Fabricated in 1.8V 0.18µm CMOS, the TDC achieves an input range of 204.8ns, 8.125ps resolution, and 7.5ns dead-time, while consuming 35mW at 100MS/s and occupying 0.23mm<sup>2</sup> core area.

**Multi-Step Counting ADC** ..... 17

*Pedram Payandehnia (Oregon State University), Xin Meng (Oregon State University),  
Gabor C. Temes (Oregon State University)*

A counting analog-to-digital converter (ADC) is proposed which achieves a high sampling rate by performing the conversion in several (N) steps. In terms of the effective number of bits (ENOB) of the ADC, the conversion time of the ADC is approximately  $N \cdot 2 \cdot \text{ENOB} / N$  clock periods, which is much shorter than for traditional counting ADCs ( $2 \cdot \text{ENOB}$  clock periods). This is achieved by using novel methods of residue amplification and correlated double sampling. Simulation results are provided to verify the effectiveness of this structure.

**Session A1L-C: Low Power and High Performance Digital Integrated Circuits Design**

**Chair:** Yong-Bin Kim, *Northeastern University*

**Co-Chair:** Kyung Ki Kim, *Daegu University*

**Time:** Monday, August 4, 2014, 10:10 - 11:50

**Location:** North & South 40

**Process Variation Verification of Low-Power Secure CSSAL AES S-Box Circuit** ..... 21

*Câncio Monteiro (Gifu University), Yasuhiro Takahashi (Gifu University), Toshikazu Sekine (Gifu University)*

In this work, we implement our previously proposed charge sharing symmetric adiabatic logic (CSSAL) in an 8-bit S-box circuit using a multi-stage positive polarity Reed-Muller (PPRM) representation with a composite field technique. We evaluate the effectiveness of the CSSAL S-box circuit against side-channel attacks towards the variations of the CMOS process technology. The results of this paper are obtained from the SPICE simulation with 0.18  $\mu\text{s}$  and 90-nm standard CMOS technology at an operating frequency band of 125 KHz--70 MHz.

**An Asynchronous Finite Impulse Response Filter Design for Digital Signal Processing Circuit** ..... 25

*Liang Men (University of Arkansas), Jia Di (University of Arkansas)*

The clockless feature of asynchronous circuit promotes its application in Digital Signal Processing (DSP) under special applications such as ultra-low power and extreme environments. In this paper, Finite Impulse Response (FIR) filter is implemented in delay-insensitivity asynchronous circuit using the pipeline architecture of Multi-Threshold NULL Conventional Logic (MTNCL). The computing units with different pipeline stages and pattern delay shift registers are integrated as 4 designs of FIR filter using the IBM 130nm 8RF process. Simulation results demonstrate the tradeoff between system throughput and energy efficiency, as the number of pipeline stage changes in the circuit.

**A Multi-Mode Energy-Efficient Double-Precision Floating-Point Multiplier** ..... 29

*Gopi Neela (University of Southern California), Jeffrey Draper (University of Southern California)*

Energy-efficiency is among the most important goals of the current IC industry. To achieve this goal each subcomponent of a chip must be optimized for energy. Even though a tremendous amount of research has been dedicated to optimizing floating-point multipliers (FPM) for better performance, efforts are continuously being made to further enhance them, indicating their importance in the computing world. Hence a multi-mode operating energy-efficient FPM is introduced in this work. This double-precision multiplier dynamically adapts to three modes of operations based on the effective precision of the inputs: low-precision, asymmetric, and full modes, where a  $24 \times 24$ ,  $24 \times 53$ , or  $53 \times 53$  fraction multiplication is required, respectively. Due to the highly frequent occurrence of low-precision operands (i.e., the least significant bits of the fraction are zeros), switching between these modes saves energy by avoiding unnecessary bit-level computations. Results show up to 25% and 21% savings in dynamic energy and total energy, respectively. A two-tier 3DIC FPM design is also proposed to further enhance the performance of the multi-mode FPM.

**Transistor Doping Profile Optimization for Low Power Subthreshold Circuits** ..... 33

*Munem M. Hossain (University of Missouri-Kansas City), Masud H. Chowdhury (University of Missouri-Kansas City)*

This paper introduces a new three-dimensional doping scheme for the transistors in subthreshold circuits. It is characterized by the absence of halos at the source and drain region. Under the proposed scheme there can be four different doping profiles for subthreshold device. In this paper we concentrate on Gaussian doping distributions both along the channel and across the depth of the transistor. Results show that the optimized device with the proposed doping profile improves the ON current. The analysis is done by varying the doping profile and gate-source voltage (Vgs), and the observations are compared with the super-threshold device.

## Session A1L-D: Power Converters for Energy Harvesting Applications

**Chair:** Hoi Lee, *University of Texas, Dallas*

**Co-Chair:** Ayman Fayed, *Iowa State University*

**Time:** Monday, August 4, 2014, 10:10 - 11:50

**Location:** Ballroom – 6

### **A Bipolar Output Voltage Pulse Transformer Boost Converter with Charge Pump Assisted**

**Shunt Regulator for Thermoelectric Energy Harvesting** ..... 37

*Ying-Khai Teh (Hong Kong University of Science and Technology), Philip K.T. Mok (Hong Kong University of Science and Technology)*

This work first generates  $\pm 1V$  output via the self-startup pulse transformer boost converter. Another on-chip single-stage voltage tripler then generates 3V output from the extra output power of boost converter, which is shunted otherwise. Higher voltage headroom is instrumental for sensor, analog and RF circuits. Charge pump clock frequency is adaptively tracking the input voltage, which is sensed using power-saving time-domain digital technique. Based on a standard CMOS 0.13- $\mu m$  technology, chip measurement verified the standalone boost converter and simulation confirmed the overall system operations. The system requires minimum startup input voltage of 36 mV and input power of 5.8  $\mu W$ .

### **A 20-300mV Transformer-Based Self-Startup Flyback Converter with MPPT and ZCS**

**Control for Thermoelectric Energy Harvesting** ..... 41

*Haozhou Zhang (Zhejiang University), Menglian Zhao (Zhejiang University), Sheng Liu (Zhejiang University), Yuhua Fang (Zhejiang University), Xiaobo Wu (Zhejiang University)*

This paper presents a novel transformer-based flyback dc-dc converter with MPPT and ZCS control for ultra low input voltage of 20-300mV. By dividing startup process into two modes, the startup time is 0.1s at  $V_{IN}=300mV$  and 3s at  $V_{IN}=50mV$ . And the MPPT accuracy is 98%, maximizing the input energy. The switching current of Mp1 is less than 5% of the inductor peak current. By turning off blocks when MPPT and ZCS have been done, the current consumption of controller is only 0.6 $\mu A$ . The peak efficiency is 91% when  $V_{IN}$  is larger than 100mV. And the efficiency is 75% at  $V_{IN}=20mV$ .

**A Switched-Capacitor Voltage Regulator for Ultra-Low Power Energy Harvesting Systems** ..... 45

*Jarno Salomaa (Aalto University), Mika Pulkkinen (Aalto University), Kari Halonen (Aalto University)*

In this paper, an SC voltage doubler-based voltage regulator for ultra-low power energy harvesting applications is presented. It produces a stable 1.2-V power supply, using inputs from 0.63V to 1.8V. External compensation and on-chip output capacitor ensure good performance even with zero load current and any load capacitance. The regulator tolerates arbitrary input ramp-ups, and is immune to blackout and brownout. The regulator ASIC is implemented in a 0.18 $\mu m$  CMOS process. The measured regulator peak power and current efficiency are 63% (ideal: 80%) and 49% (50%), respectively. The performance has been characterized with load currents from zero to 100 $\mu A$ .

**A Burst-Mode based Boost Converter Harvesting Photovoltaic Energy for Low Power Applications** ..... 49

*Sheng Liu (Zhejiang University), Yi Zhao (Zhejiang University), Menglian Zhao (Zhejiang University),*

*Haozhou Zhang (Zhejiang University), Xiaobo Wu (Zhejiang University)*

This paper treats the case of harvesting photovoltaic energy. Dealing with low power applications, the power transfer stage, which is a boost converter, is designed to work at burst-mode to achieve low power consumption. And a simple Maximum Power Point Tracking (MPPT) method, based on open voltage detection, is also utilized in the system to increase the system's power efficiency. The chip, with the power MOSFETS in it, was implemented in Global Foundry 0.18  $\mu m$ , 1.8/3.3 V, RFCMOS process, and the power efficiency reached 80% at 80 mV input voltage and 100  $\mu A$  load current.

**Model and Prototype of a Green Electrostatic Harvester of Vibration Energy** ..... 53

*Yin Li (University of Guelph), Manjusri Misra (University of Guelph), Stefano Gregori (University of Guelph)*

This paper presents the model and the prototype of a regenerative electrostatic energy harvester based on a mechanically-variable capacitor with no startup battery. The functionality of the device is verified through simulations and measurements. The measurement results are compared with those of an electrostatic energy harvester based on a startup battery in similar conditions. The proposed device is smaller and harvests more energy per cycle than the conventional one. The compact and battery-less design makes it a promising solution to power small, green electronic systems.

## Session A1L-E: Reconfigurable RF-CAS for RADAR, Cognitive Radio and EARS – II

**Chair:** Changzhi Li, *Texas Tech University*

**Co-Chair:** Arjuna Madanayake, *University of Akron*

**Time:** Monday, August 4, 2014, 10:10 - 11:50

**Location:** Ballroom – 7

### **Reconfigurable Microwave Couplers with Dynamic Performance Control** ..... 57

*Mi Zhou (University of North Texas), Han Ren (University of North Texas), Jin Shao (University of North Texas), Bayaner Arigong (University of North Texas), Jun Ding (University of North Texas), Hualiang Zhang (University of North Texas)*

Two kinds of reconfigurable microwave couplers are presented. The first one is a 90-degree branch-line coupler with a wide range of tunable coupling ratios. When its coupling ratio is tuned to be 1, this coupler becomes a crossover. The second one possesses a reconfigurable performance between a rat-race coupler and a 90-degree coupler. Varactors are loaded to both couplers as the tuning elements. By applying suitable control voltages, reconfigurable performance is realized. Closed-form equations are derived to theoretically analyze the proposed devices. To further verify the design theory, both structures are simulated. Moreover, the first coupler is fabricated and characterized.

### **Frequency-Dependent Power Amplifier Modeling and Correction for Distortion in Wideband Radar Transmissions** ..... 61

*Z. Dunn (University of Oklahoma), M. Yearly (University of Oklahoma), C. Fulton (University of Oklahoma)*

The Volterra Series, more specifically the Memory Polynomial Model, is utilized to model power and frequency dependent non-linear distortion of a high power amplifier. This modeling technique is also used to create a digital predistortion model that makes the overall transmission chain behave linearly as a function of power. Digital predistortion is especially useful for wideband signals, where it allows the amplifier to operate at highest power added efficiency in the compression region while still behaving linearly. Therefore, wideband radar waveforms can be generated at high fidelity, maximizing transmission power with the given equipment while maintaining low range sidelobes.

### **Wireless Radar Devices for Smart Human-Computer Interaction** ..... 65

*Yiran Li (Texas Tech University), Changzhan Gu (Marvell Semiconductor Inc.), Tooraj Nikoubin (Texas Tech University), Changzhi Li (Texas Tech University)*

Due to the noncontact and low-cost properties of Doppler radar, it has been adopted to detect movement in variety applications. This paper introduces a portable Doppler radar sensor device named as iMotion radar which is a 2.4-GHz AC-coupled continuous-wave mode Doppler radar. This iMotion radar has been designed as a 5cm x 5cm printed circuit board and has already been used in different applications. The results for being used in different applications showed the reliability and flexibility of iMotion Radar. The detail in hardware design will be given in this paper and a body orientation identification application which has been done by iMotion Radar will be reviewed.

### **Reconfigurable N-Path RF Front-End Filter with Improved Blocker Rejection** ..... 69

*Md. Naimul Hasan (University of California, Davis), Sudhir Aggarwal (Nokia Research Center), Qun Jane Gu (University of California, Davis), Xiaoguang Liu (University of California, Davis)*

In this paper an RF channel-select filter with improved blocker rejection is presented. The proposed filter consists of three bandpass resonators and two notch resonators all implemented with N-path switched-capacitor filters. Due to the inclusion of notch resonators between the bandpass resonators, the rejection of the filter in the vicinity of the passband is higher compared with any existing filters. Out-of-band blockers are suppressed due to high filter rejection. The proposed filter has 48.3 dB rejection at 20 MHz offset and has 58.8 dB rejection at 45 MHz offset from the center frequency. The high stopband rejection of 71.2 dB has been achieved by creating notches outside the bandwidth of the filter. The filter is tunable from 0.2 GHz to 1.8 GHz. The filter is designed in 65 nm CMOS technology.

### **A Transmission Line Circuit-Oriented Approach for Miniaturization of a Log-Periodic Dipole Array (LPDA) Antenna** ..... 73

*Mohammad J. Almalkawi (Directed Energy, Inc.), Lee W. Cross (Directed Energy, Inc.), Khair A. Alshamaileh (University of Toledo)*

A miniaturized planar log-periodic dipole array (LPDA) antenna is presented. Antenna miniaturization is accomplished by replacing the uniform dipole elements of the conventional LPDA antenna with elements that possess variable-impedance profiles governed by a truncated Fourier series. Conventional and miniaturized LPDA antennas exhibiting 7 dB end-fire gains are designed to operate over the frequency range of 2 to 4 GHz. A 32 % reduction in dipole arm length was achieved. Full-wave simulation results show stable directional radiation patterns, excellent front-to-back ratio over the designed impedance bandwidth, and minimal degradation in the overall electrical performance.



## Session A1L-F: High-Speed Interfaces and High-Sensitivity Signal Detectors

**Chair:** Marvin Onabajo, *Northeastern University*

**Time:** Monday, August 4, 2014, 10:10 - 11:50

**Location:** Brazos

### **10 Gb/s Adaptive Receive-Side Near-End and Far-End Crosstalk Cancellation Circuitry** ..... 77

*Byungho Min (Texas A&M University), Noah Hae-Woong Yang (Texas A&M University), Samuel Palermo (Texas A&M University)*

This paper presents receive-side circuitry which merges near-end and far-end crosstalk cancellation. NEXT cancellation is realized with a novel 3-tap FIR filter which combines two traditional FIR filter taps and a continuous-time band-pass filter IIR tap, with all coefficients automatically determined via an on-die SS-LMS adaptation engine. FEXT cancellation is realized with a differentiator circuit whose gain is automatically adjusted with a power-detection-based adaptation loop. A 65nm CMOS prototype operates at 10 Gb/s over coupled 4-in FR4 transmission line channels with NEXT and FEXT aggressors and opens a previously closed eye to allow for a 0.2 UI timing margin.

### **A 8 Gbps 0.67mW 1 Tap Current Integrating DFE in 40nm CMOS** ..... 81

*Ahmed Ismail (Mixel, Inc. / Ain Shams University), Sameh Ibrahim (Ain Shams University), Mohamed Dessouky (Ain Shams University)*

This paper describes the implementation issues in designing a 1 tap current integrating half rate decision feedback equalizer. We introduce a new technique for designing an 8Gbps 1 tap half rate current integrating DFE in 40nm CMOS technology that draws 0.67mW from a 1.1V supply. The technique uses a delayed clock rather than speculation. This removes the speculation impact on power consumption and timing constraints especially in multi tap DFE.

### **A Low-Power 28 Gb/s CDR using Artificial LC Transmission Line Technique in 65 nm CMOS** ..... 85

*Shita Guo (Southern Methodist University), Tianzuo Xi (Southern Methodist University), Guoying Wu (Southern Methodist University), Tianwei Liu (Southern Methodist University), Tao Zhang (Southern Methodist University), Ping Gui (Southern Methodist University), Yanli Fan (Texas Instruments Inc.), Mark Morgan (Texas Instruments Inc.)*

This paper presents a low-power 28 Gb/s PLL-based clock and data recovery circuit in 65 nm CMOS technology. The artificial LC transmission line technique is proposed to be used in the full rate bang-bang phase detector to reduce the number of D-latches and save power consumption by 42.8% compared with the conventional phase detector design. By using the transmission line technique, the retiming circuit is merged into the phase detector, which further saves power of the data retiming circuit. The compact phase detector with built-in retiming circuit also alleviates the capacitive loading of and saves corresponding power consumed by the clock buffer. In addition, the artificial LC transmission line is proposed to be used in the clock buffer to drive the distributed capacitive loads presented by separate D-latch and save power consumption by 50% compared with the conventional inductive peaking clock buffer. The total power consumption of the CDR is 35 mW from a 1.1 V supply.

### **-80dBm~0dBm Dynamic Range, 30mV/dB Detection Sensitivity Piecewise RSSI for SDR/CR Receivers** ..... 89

*Xinwang Zhang (Tsinghua University), Baoyong Chi (Tsinghua University), Bingqiao Liu (Tsinghua University), Zhihua Wang (Tsinghua University)*

A high dynamic range, high detection sensitivity piecewise RSSI (received signal strength indicator) for software-defined radio (SDR) and cognitive radio (CR) receivers is proposed. With the reconfigurable limiting amplifiers, the RSSI achieves wide dynamic range and high detection sensitivity simultaneously. Two-path I/Q configuration RSSI structure is adopted to reduce the output voltage glitch. The transfer curve of the RSSI keeps stable under various PVT variations with the help of the self-adaptive bias circuit. The proposed RSSI has been implemented in 65nm CMOS and occupies 0.06 mm<sup>2</sup> chip area. It consumes a scalable current from 1mA to 2.4mA from 1.2V power supply, dependent on the limiting amplifier setting. The simulated results show that the RSSI can detect the signal strength from -80dBm to 0dBm with 30mV/dB detection sensitivity and maximum 1.4dB linearity error over 100KHz~20MHz input carrier frequency range.

### **Readout Electronic System for Particle Tracking in Secondary Electron Detectors** ..... 93

*A. Garzón-Camacho (Institute for the Structure of Matter (CSIC)), B. Fernández (Universidad de Sevilla), M.A.G. Alvarez (Universidade de São Paulo), J. Ceballos (Instituto de Microelectrónica de Sevilla / CSIC-Universidad de Sevilla), J.M. de la Rosa (Instituto de Microelectrónica de Sevilla / CSIC-Universidad de Sevilla)*

This paper presents the design and implementation of an electronic front-end intended for spatial detection of ion beams at counting rates higher than 10<sup>6</sup> particles per second. The readout system is made up of three main multi-channel building blocks, namely: a transimpedance preamplifier, a signal-conditioning line receiver and a charge-to-digital converter, which are properly combined with some off-the-shelf components. Several experiments have been carried out, considering  $\alpha$  particles sources and particles beams, featuring an adaptive shaping time frame of 170-to-230 ns with a peak signal-to-noise ratio of up to 25.2dB. These performance metrics are competitive with the state of the art, showing the suitability of the proposed data acquisition system for accurate and fast particle tracking detection.

## Session A2L-A: Nyquist-Rate Data Converters II

**Chair:** R. Jake Baker, *University of Nevada, Las Vegas*

**Time:** Monday, August 4, 2014, 13:10 - 14:50

**Location:** Mockingbird

### **A Energy-Efficient High Speed Segmented Pre-Quantize and Bypass DAC for SAR ADCs** ..... 97

*Xiaoyang Wang (University of Electronic Science and Technology of China), Xiong Zhou (University of Electronic Science and Technology of China), Qiang Li (University of Electronic Science and Technology of China)*

In this paper a segmented pre-quantize and bypass architecture for SAR ADC has been proposed. The capacitive DAC is segmented and small capacitor array is used to convert the MSB codes. According to the result of pre-quantization unnecessary switching of high weight capacitors are bypassed, which improves the power efficiency and linearity of ADC and accelerates the conversion speed. A 10-bit 150MS/s ADC with the proposed architecture is implemented in a standard 65nm CMOS technology. According to the simulation, the ADC performs an ENOB of 9.77-bit and 82.8dB SFDR at transistor level simulation, achieving a FOM of 9.33 fJ/Conversion step.

### **A 1.9 GS/s 4-Bit Sub-Nyquist Flash ADC for 3.8 GHz Compressive Spectrum Sensing in 28 nm CMOS** ..... 101

*David Bellasi (ETH Zürich), Luca Bettini (ETH Zürich), Thomas Burger (ETH Zürich), Qiuting Huang (ETH Zürich), Christian Benkeser (RUAG Space), Christoph Studer (Cornell University)*

Spectral activity detection in wideband radio-frequency (RF) signals for cognitive-radio applications typically necessitates expensive and energy-inefficient analog-to-digital converters (ADCs). In this paper, we present a novel compressive sensing (CS)-based analog front-end, which is able to sample sparse wideband RF signals at low cost and low power. The analog front-end consists of a pseudo-random non-uniform clock generator unit offering the possibility to configure the (average) undersampling factor at run-time, and a low-cost, wideband 1.9 GS/s 4-bit flash ADC. The spectral information acquired at sub-Nyquist rates can be recovered off-line via novel sparse signal dequantization algorithms. The developed analog front-end is implemented in 28 nm CMOS, and enables the recovery of spectrally sparse RF signals up to 3.8 GHz by means of CS, which corresponding to a Nyquist-equivalent sampling rate of 7.6 GS/s. The ADC and pseudo-random clock generator together occupy less than 0.1 mm<sup>2</sup>, and consume an estimated 4.1 mW to 5.4 mW for undersampling factors between 4 and 11.5.

### **A 0.9V 12-Bit 200-kS/s 1.07μW SAR ADC with Ladder-Based Reconfigurable Time-Domain Comparator** ..... 105

*Xiaolin Yang (Zhejiang University), Yin Zhou (Zhejiang University), Menglian Zhao (Zhejiang University), Zhongyi Huang (Zhejiang University), Lin Deng (Zhejiang University), Xiaobo Wu (Zhejiang University)*

The SAR ADCs for biomedical application, have a strict limit on its power consumption. Two techniques are introduced into its design: a novel ladder-based reconfigurable time domain comparator is proposed to reduce the noise and to adjust power according to inputs automatically; and a novel clock distribution scheme is utilized to save more than 55% power consumption. The prototype chip is designed and fabricated in UMC 0.18μm technology. The simulation results show that with supply voltage of 0.9V, the ADC consumes 1.07μW at the sampling rate of 200kS/s. And the SNDR is 71.2 dB with 3.24kHz input signal

### **A Low-Power Analog-to-Digital Converter with Digitalized Amplifier for PAM Systems** ..... 109

*Yingchieh Ho (National Dong-Hwa University), Chou-Ming Kuo (National Chiao-Tung University), ChauChin Su (National Chiao-Tung University)*

In this paper, we have proposed a 4-bit 5-GSample/s flash analog-to-digital converter (ADC) for pulse amplitude modulation (PAM) systems. In order to achieve low-power consumptions, digitalized cells for analogue amplifying are developed in the proposed ADC. Digitalized cells reduce power significantly due to using fewer devices as compared to pure analogue designs. A self-biasing circuit is used in the digitalized amplifier can enhance linear amplifying region. Besides, the digitalized amplifier can achieve high speed according to its bandwidth compensation technique. The test chip is implemented with 90nm CMOS Logic and Mixed-Mode 1P9M Low-K Process. The low-power digitalized ADC is operated under 5GSample/s. All the results of post-simulation are demonstrate in a 16-PAM system, and efficient number of bit is 3.9bit. Moreover, INL and DNL are less than 0.5LSB. The power consumption of the ADC is 33.7mW, and the FoM of energy per conversion step is only 0.45pJ. The overall chip area is 0.873mm<sup>2</sup>.

## Session A2L-C: High Performance Digital VLSI Design Method

**Chair:** Jia Di, *University of Arkansas*

**Co-Chair:** Volnei Pedroni, *UTFPR, Brazil*

**Time:** Monday, August 4, 2014, 13:10 - 14:50

**Location:** North & South 40

### **Framework of a Scalable Delay-Insensitive Asynchronous Platform Enabling Heterogeneous Concurrency** ..... 113

*Liang Men (University of Arkansas), Jia Di (University of Arkansas)*

Parallel architecture of asynchronous circuits has great potential in improving throughput while reducing energy consumption. This paper presents a parallel platform designed using delay-insensitive asynchronous logic. Heterogeneous data processing units as well as datapath control logic are integrated in the platform. All these units share the common data I/O and external handshaking control channels. Asynchronous arbiters are incorporated to make the cores' data requests mutually exclusive. The highly-modular interface and delay-insensitivity allow the platform to be easily cascaded to construct large systems. Simulation results indicate the functional correctness of the heterogeneous platform as well as its cascaded structure.

### **Delay Variation Analysis in the Presence of Power Supply Noise in Nano-Scale Digital VLSI Circuits** ..... 117

*Bardia Bozorgzadeh (Case Western Reserve University), Shahab Shahdoost (Case Western Reserve University),*

*Ali Afzali-Kusha (University of Tehran)*

In this paper, a novel analytical model is proposed to predict the delay variation due to the power supply noise in nanotechnologies. First, an analytical model is derived for the special case of an inverter gate; next, it is shown that the derived model can also be applied to the other gates. The proposed analytical model helps us to better understand the main contributors to the delay variation and provides an accurate prediction of the delay variation due to the power supply noise in nano-scale VLSI circuits. The accuracy of the proposed model is verified with SPICE simulation in 90nm and 45nm predictive technology models. The maximum error of the proposed model is 7.5% and 8.3% in 90nm and 45nm technologies respectively.

### **Modeling the Effect of NMOS Gate Capacitance in an On-Chip Decoupling Capacitor PAA Countermeasure** .. 121

*Matthew Mayhew (University of Guelph), Radu Muresan (University of Guelph)*

In this paper we develop a general model based on the width of a decoupling NMOS gate capacitor for use in the design of decoupling based PAA countermeasures. A polynomial equation was determined based on experimental data to link the width of the decoupling element with the data security provided by the countermeasure architecture. The proposed model is meant to act as a tool for a designer when considering the incurred design overheads when allocating area during the initial planning phase. Experimental data was collected from the simulation of a partial decoupling test bench implemented in 65 nm TSMC technology.

### **Detailed Analysis of Implementation Options for Timed Finite State Machines in Hardware** ..... 125

*Volnei A. Pedroni (Universidade Tecnológica Federal do Paraná)*

Very few topics affect a larger audience of digital circuit designers than the subject of correctly designing and implementing finite state machines (FSMs) in hardware. For that purpose, it was shown recently that any FSM can be classified into one of just three categories, called regular, timed, and recursive FSMs. The main problem, highly subject to gross errors in practice and not properly covered by any EDA tool, is the implementation of the timed machines, because the timer must be simple and, more importantly, it is the FSM itself who must control the timer, deciding when (and how) it should run, stop, or be zeroed. This paper addresses this issue by presenting a detailed analysis of two timer-control strategies, along with corresponding circuits, design variations, pros and cons, and experimental results with hardware and power consumption measurements from implementations in three FPGA devices.

### **An Improvement Technique for the Test Compression Ratio and Application Time of Multiple Expansion Scan Chain based SoC using New Cost Function** ..... 129

*Do Han Lee (Samsung Electronics, Co. Ltd. and Sungkyunkwan University),*

*Tae Hee Han (Sungkyunkwan University)*

The importance of an efficient methodology for testing defects generated during IC manufacturing process is more than ever significant as the complexity of system on a chip (SoC) increases. Scan test is the most prevalent method for detecting stuck-at faults of digital integrated circuits. There are great demands for more efficient and lossless improvement techniques to reduce test cost growth caused by increase in chip density. In this paper, we propose a new multiple expansion scan chain (MESCC) based technique by exploiting novel cost function considering additional variables for the total chain length of concatenated chains and sophisticated dependency analysis between each pair of chains. This proposed method is applied to two digital IP blocks of state-of-the-art mobile SoC fabricated in 14nm CMOS process. Experimental results show that the test data volume (TDV) is reduced by 10.4% and the longest chain length (LCL) decreases by 47.1% in maximum respectively when compared to existing works.



## Session A2L-D: Image Processing and Multimedia Systems I

**Chair:** Marvin Onabajo, *Northeastern University*

**Time:** Monday, August 4, 2014, 13:10 - 14:50

**Location:** Ballroom – 6

### **An Efficient Implementation of Deep Convolutional Neural Networks on a Mobile Coprocessor** ..... 133

*Jonghoon Jin (Purdue University), Vinayak Gokhale (Purdue University), Aysegul Dundar (Purdue University), Bharadwaj Krishnamurthy (Purdue University), Berin Martini (Purdue University), Eugenio Culurciello (Purdue University)*

In this paper we present a hardware accelerated real-time implementation of deep convolutional neural networks (DCNNs). DCNNs are becoming popular because of advances in the processing capabilities of general purpose processors. DCNNs produce hundreds of intermediate results whose constant memory accesses result in inefficient use of general purpose processor hardware. By using an efficient routing strategy, we are able to maximize utilization of available hardware resources but also obtain high performance in real world applications. Our system, consisting of an ARM processor and a coprocessor, is capable of a peak performance of 40G-ops/s while consuming less than 4W of power.

### **Supervised Facial Recognition based on Multi-Resolution Analysis and Feature Alignment** ..... 137

*Ahmed Aldhahab (University of Central Florida), George Atia (University of Central Florida), Wasfy B. Mikhael (University of Central Florida)*

A new supervised algorithm for face recognition based on the integration of Two Dimensional Discrete Multiwavelet, Radon, and Discrete Wavelet Transform is proposed. In the feature extraction step, Multiwavelet filter banks are used to extract useful information from the databases. The extracted information is then aligned using the Radon Transform, and localized by 2D DWT. This information is fed into a Neural Network based classifier. The proposed method is tested on three databases, namely, ORL, YALE and FERET. It is shown that this approach can significantly improve the classification performance and the storage requirements of the overall recognition system.

### **Contourlet Domain Image Denoising using the Alpha-Stable Distribution** ..... 141

*H. Sadreazami (Concordia University), M. Omair Ahmad (Concordia University), M.N.S. Swamy (Concordia University)*

In this paper, a new contourlet-based method for denoising of images corrupted by additive white Gaussian noise is proposed. The alpha-stable distribution is used to model the contourlet coefficients of noise-free images. This model is then exploited to develop a Bayesian minimum mean absolute error estimator. A modified empirical characteristic function-based method is employed for estimating the parameters of the assumed alpha-stable prior. The performance of the proposed denoising method is evaluated by using standard noise-free images corrupted with simulated noise and compared with that of the other state-of-the-art methods. The results show that the proposed method provides values of the peak signal-to-noise ratio higher than that provided by some of the existing techniques along with superior visual quality images.

### **A Hardware Implementation of Hough Transform based on Parabolic Duality** ..... 145

*Naren Ramesh (University of Cincinnati), George Purdy (University of Cincinnati), Carla Purdy (University of Cincinnati), Justin Smith (Northern Kentucky University)*

Hough Transform is a pattern recognition tool commonly used in many image processing algorithms. The one problem that still remains fundamental to the parabolic form of the Hough Transform with respect to straight line detection is its inability to detect vertical lines. This has caused Hough Transform algorithms to use the Radon Transform rather than the parabolic form for straight lines in most cases. This paper presents a method to overcome this drawback by incorporating two different forms of the slope intercept equation of a line. We also reduce memory requirements, thus enabling higher precision for computations. We model the proposed algorithm using an FPGA simulation tool to determine its basic functionality with respect to computational overhead and accuracy. The new algorithm overcomes the difficulties of hardware implementation of the Radon Transform of Hough Transform by avoiding the use of CORDIC algorithms and trigonometric lookup tables which only add extra overhead and reduce precision.

## Session A2L-E: Multispectral and Hyperspectral Remote Sensing

**Chair:** William McDowell, *Lockheed Martin*

**Co-Chair:** Wasfy Mikhael, *University of Central Florida*

**Time:** Monday, August 4, 2014, 13:10 - 14:50

**Location:** Ballroom – 7

### **Hyperspectral Unmixing via Semantic Spectral Representations** ..... 149

*Yuki Itoh (University of Massachusetts, Amherst), Siwei Feng (University of Massachusetts, Amherst), Marco F. Duarte (University of Massachusetts, Amherst), Mario Parente (University of Massachusetts, Amherst)*

We propose a new spectral unmixing method using a semantic spectral representation, which is produced via non-homogeneous hidden Markov chain (NHMC) models applied to wavelet transforms of the spectra. Previous studies have shown that the representation is robust to spectral variability in the same materials because it can automatically detect the diagnostic spectral features in the training data. Therefore, our method can successfully detect materials while automatically extracting diagnostic features. Simulations show that our unmixing method can be effectively used in the case of Hapke mixtures.

### **An Intelligent Readout Circuit for Infrared Multispectral Remote Sensing** ..... 153

*Payman Zarkesh-Ha (University of New Mexico)*

Over the years infrared imaging technology has enabled many critical applications such as thermal and spectral imaging, medical diagnostics, and remote sensing. The growth in infrared imaging technology has been made possible by dramatic technical advances in infrared sensor manufacturing, as well as improvements in algorithms for image processing. However, the most powerful existing infrared imaging systems are still far behind their biological counterparts in many aspects including energy efficiency, computational capabilities, and performance. Inspired by biological imaging systems, in this paper we present an intelligent readout circuit based upon spectrally tunable infrared nanostructure sensors, which can revolutionize multispectral remote sensing systems.

### **MASINT Fusion of Multispectral, Hyperspectral and Kinematic Phenomenology** ..... 157

*William McDowell (University of Central Florida and Lockheed Martin Missiles & Fire Control), Wasfy B. Mikhael (University of Central Florida)*

The evolution of Electro-Optical (EO) technology has continuously advanced towards minimizing a sensor's size, weight and cost while simultaneously increasing key performance metrics such as resolution and range. Frequently, these dichotomous objectives make for a trade space which is difficult to resolve. Fortunately, the use of unresolved multispectral and hyperspectral imagery fused with other Measurement And Signature Intelligence (MASINT) such as target kinematic features presents an opportunity to extend a sensor's useful classification / discrimination range without requiring additional hardware innovation. In this paper, we will provide an overview of multispectral, hyperspectral and kinematic based MASINT phenomenologies which are available for extraction and exploitation. Additionally, we will review feature and information fusion from the perspective of Maximum Likelihood, Naïve Bayes and Bayesian Belief Networks in the context of MASINT Information Fusion.

## Session A2L-F: Control Systems, Mechatronics and Robotics

**Chair:** Carlos Silva Cardenas, *Pontificia Universidad Católica del Peru*

**Time:** Monday, August 4, 2014, 13:10 - 14:50

**Location:** Brazos

### **Approximate Controller Design for Singularly Perturbed Aircraft Systems** ..... 161

*Joseph E. Graziosi (Wichita State University), M.E. Sawan (Wichita State University), J.W. Watkins (Wichita State University)*

The purpose of this paper is to extend the Quasi-Steady State Approximation and Matrix Block Diagonalization methods utilized in the Approximate Controller Design for Singularly Perturbed Aircraft Systems paper by Sawan and Shim 2005. In that paper, it was shown that an approximate controller solution could be developed by relocating only the slow poles for two-time scale aircraft dynamics. In addition, it showed the difference between the approximate solutions and the exact solutions were bounded within limits as  $O(\epsilon)$  and  $O(\epsilon^2)$ . This technique was successfully applied to the lateral dynamics of the DeHaviland Canada DHC-2 Beaver. In this paper, the same technique is applied to the NASA F-8 Aircraft dynamics in order to show that the method is not unique to the Beaver and can be applied to other aircraft models. It also extended the method to consider the singularly perturbed stochastic system and confirmed stability was maintained.

**Deadzone Compensation in Motion Control Systems using Model Reference Direct Inverse Control** ..... 165

*Carlos S. Betancor-Martín (Universidad de Las Palmas de Gran Canaria), Juan A. Montiel-Nelson (Universidad de Las Palmas de Gran Canaria), Aurelio Vega-Martínez (Universidad de Las Palmas de Gran Canaria)*

This work introduces the application of the model reference direct inverse control technique for compensating the deadzone of DC servo systems. In order to improve the control performance related to modeling errors and disturbances, we design a proportional integral fuzzy controller in the feedback loop. Though the implementation of the proposed control is simple, results demonstrate a better behavior than more complex control techniques proposed in the literature. We study the robustness of the proposed system varying different parameters of the system.

**Low Pull-In Voltage Electrostatic MEMS Switch using Liquid Dielectric** ..... 169

*Mohammed Affan Zidan (King Abdullah University of Science and Technology), Jurgen Kosel (King Abdullah University of Science and Technology), Khaled N. Salama (King Abdullah University of Science and Technology)*

In this paper, we present for electrostatic MEMS switch with liquids as dielectric to reduce the actuation voltage. The concept is verified by simulating a lateral dual gate switch, where the required pull-in voltage is reduced by more than 8 times after using water as a dielectric, to become as low as 5.36V. The proposed switch is simulated using COMSOL multiphysics using various liquid volumes to study their effect on the switching performance. Finally, we propose the usage of the lateral switch as a single switch XOR logic gate.

**Session A3P-G: Amplifiers and Filters I**

**Chair:** Paul Furth, *New Mexico State University*

**Co-Chair:** Tina Wang, *Iowa State University*

**Time:** Monday, August 4, 2014, 14:50 - 15:40

**Location:** Poster Area

**A Digital to Transconductance Converter for Nauta Structure op-Amps in 65nm CMOS** ..... 173

*Andrew Nicholson (University of New South Wales), Julian Jenkins (Perceptia Devices, Inc.), André van Schaik (University of Western Sydney), Tara Julia Hamilton (University of New South Wales), Torsten Lehmann (University of New South Wales)*

We propose a digital-to-transconductance converter based on a weighted sum of parallel CMOS inverters designed with a specific width ratio such that they exhibit only negative differential non-linearity of output transconductance over the range of digital control bits. The converter forms the crucial role inside digitally programmable Nauta structure op-amps we have under active research. Nauta structure differential operational amplifiers are being investigated for their potential to overcome the problems of reduced supply, voltage headroom and limited output voltage swing associated with traditional analog techniques in deep sub-micron CMOS. The design of Nauta op-amps requires transistor matching strategies within the symmetrical inverter-based architecture to enable high gain conditions.

**Time Difference Amplifiers to Improve the Dynamic Range of MASH Time Encoded ADCs** ..... 177

*Laura Conesa-Peraleja (Universidad Carlos III de Madrid), Susana Paton (Universidad Carlos III de Madrid)*

This paper presents a time difference amplifier to improve the resolution of cascaded Time Encoded (TE) Analog-to-Digital Converters (ADCs). Time difference amplifiers are employed to increase the resolution of Time-to-Digital Converters, and most of them are based on imposing a certain time offset at the input of an SR latch. They are limited in their gain and input range, and exhibit a large delay. This paper proposes a novel analog time difference amplifier that can achieve a more accurate and higher gain with limited delay. These features make this circuit more suitable for multi-stage noise shaping (MASH) TE ADCs. The dynamic range extension is proven by time-domain simulations of a 1-1 TE ADC. The residue of the first stage is a pulsed signal, which pulse-width is extended by the time difference amplifier and applied into the second stage. This allows a dynamic range improvement of around 17dB for a gain of 7.

## Session A3P-H: Amplifiers and Filters II

**Chair:** Paul Furth, *New Mexico State University*

**Time:** Monday, August 4, 2014, 14:50 - 15:40

**Location:** Poster Area

### **A 60dB $\Omega$ 2.9 GHz 0.18 $\mu$ m CMOS Transimpedance Amplifier for a Fiber Optic Receiver Application** ..... 181

*Claudio Talarico (Gonzaga University), Gaurav Agrawal (Google Inc.), Janet Wang Roveda (University of Arizona)*

This paper presents the design and characterization of a high gain, high-speed differential transimpedance amplifier (TIA) to be used as front-end interface for optical receiver applications. The TIA is realized in a standard 0.18- $\mu$ m digital CMOS technology and it dissipates 25.4mW from a single 1.8 V supply. The topology consists of a common gate input stage followed by a cascoded common source and a common drain stage surrounded by a global shunt-shunt feedback with phantom zero compensation to boost bandwidth and enhance stability. Using this approach the amplifier achieves transimpedance gain of 59.75 dB $\Omega$ , -3dB bandwidth of 2.9 GHz when connected to a 2-pF photodiode at the input and a 250  $\Omega$  load at the output, and 13.14 pA/ $\sqrt{\text{Hz}}$  input referred noise.

### **Low-Voltage Fully Cascadable Resistorless Transadmittance-Mode All-Pass Filter** ..... 185

*Norbert Herencsar (Brno University of Technology), Jaroslav Koton (Brno University of Technology), Kamil Vrba (Brno University of Technology), Oguzhan Cicekoglu (Bogazici University)*

This paper presents a new realization of a first-order transadmittance-mode (TAM) all-pass filter (APF). In the proposed mixed-mode APF a simple transconductor, inverting voltage buffer, and unity-gain current follower are used as active building blocks. Considering the input intrinsic resistance of current follower as useful active filter parameter, the proposed TAM APF only employs a floating capacitor as external passive component. Hence, it is a resistorless circuit. In addition, due to high-impedance voltage input and high-impedance of output current terminal, it is fully cascadable filter realization. SPICE simulation results are included to support the theory. In the design the PTM 90 nm level-7 CMOS process BSIM3v3 parameters with low ( $\pm 0.5$  V) DC voltages were used.

## Session A3P-J: Systems and VLSI Architectures

**Chair:** Zoran Stamenkovic, *IHP, Frankfurt*

**Time:** Monday, August 4, 2014, 14:50 - 15:40

**Location:** Poster Area

### **Memory Efficient VLSI Architecture for Lifting-Based DWT** ..... 189

*A.D. Darji (Indian Institute of Technology Bombay), Ankur Limaye (Sardar Vallabhbhai National Institute of Technology, Surat)*

In this paper, we propose a new lifting-based DWT architecture for 9/7 filter, with lowest temporal memory among the existing architectures. This is achieved with a novel overlapped- scanning method and recalculation of intermediate DWT coefficients. The proposed architecture requires only 2N temporal memory to process N x N sized image. The architecture has a critical path of one multiplier delay and demonstrate 100% hardware utilization efficiency.

### **Flipping-Based High Speed VLSI Architecture for 2-D Lifting DWT** ..... 193

*A.D. Darji (Indian Institute of Technology Bombay), Konale Shashikanth (Sardar Vallabhbhai National Institute of Technology, Surat), Ankur Limaye (Sardar Vallabhbhai National Institute of Technology, Surat), S.N. Merchant (Indian Institute of Technology Bombay), A.N. Chandorkar (Indian Institute of Technology Bombay)*

In this paper, a flipping-based high speed VLSI architecture for lifting-based 2-D DWT is proposed. The direct implementation of lifting equation has long critical path delay. To reduce the critical path, the flipping structure is widely used. In the proposed architecture, the multipliers in flipping structure are replaced by shift-and-add algorithm. This reduces the critical path delay to one adder (Ta), which is the minimum possible delay any DWT architecture can have. Thus, the proposed architecture is suitable for high frequency operation and has 100% hardware utilization with low control complexity.

### **An Acoustic System for Autonomous Navigation and Tracking of Marine Fauna** ..... 197

*Pedro R. De La Torre (King Abdullah University of Science and Technology), Khaled N. Salama (King Abdullah University of Science and Technology), Michael L. Berumen (King Abdullah University of Science and Technology)*

A marine acoustic system for underwater target tracking is described. This system is part of the Integrated Satellite and Acoustic Telemetry (iSAT) project to study marine fauna. It is a microcontroller-based underwater projector and receiver. A narrow-band, passive sonar detection architecture is described from signal generation, through transduction, reception, signal processing and up to tone extraction. Its circuit and operation principles are described. Finally, a comparison between the current energy detection method versus an alternative matched filter approach is included.

**Formal Methods for Safety Critical System Specification** ..... 201

*Jonathan Lockhart (University of Cincinnati), Carla Purdy (University of Cincinnati),  
Philip Wilsey (University of Cincinnati)*

For safety critical systems, hardware is often preferred over software because it is easier to achieve safety critical goals in hardware alone and because hardware is considered more reliable than software. As systems become more complex software solutions will be important. Here we show that formal methods are a useful tool for developing software specifications for safety critical systems, since they reduce ambiguity in the design and can be proven consistent. Using formal methods for specification will enable the development of dependable, high-performance, reliable hardware/software safety critical systems.

**An Approach for Multi-Task and Multi-Application Mapping onto NoC-Based MPSoC** ..... 205

*Max Farias (Universidade Federal de Pernambuco), Edna Barros (Universidade Federal de Pernambuco),  
André Araújo (Universidade Federal de Pernambuco)*

The application mapping on a multiprocessor platform can influence in the system performance and in the energy consumption of an embedded systems. In this context, the paper presents a meta-heuristic based approach for energy aware application mapping for NoC-based MPSoC platform. Our approach was able to find a processor mapping that reduces the energy consumption of about 60%, in average, for the multi-task and multi-application, in comparison with the worst case mapping.

**Implementation of a NARX Neural Network in a FPGA for Modeling the Inverse Characteristics of Power Amplifiers** ..... 209

*J.A. Renteria-Cedano (Centro de Investigación y de Estudios Avanzados del Instituto Politécnico Nacional),  
L.M. Aguilar-Lobo (Centro de Investigación y de Estudios Avanzados del Instituto Politécnico Nacional),  
J.R. Loo-Yau (Centro de Investigación y de Estudios Avanzados del Instituto Politécnico Nacional),  
S. Ortega-Cisneros (Centro de Investigación y de Estudios Avanzados del Instituto Politécnico Nacional)*

In this paper the hardware implementation of a NARX neural network algorithm using a Fiel Programmable Gate Array (FPGA) is presented. A NARX network is a Recurrent Neural Network (RNN) suitable for modeling nonlinear systems with promising results for the modeling of the inverse characteristics (AM/AM and AM/PM) of Power Amplifier (PAs). The implementation is realized in Xilinx ISE tool with the Virtex-6 FPGA ML 605 Evaluation Kit using Verilog language. Experimental results have shown a high correlation with the inverse model computed with SystemVue in co-simulation with MATLAB for a GaN class F PA working with a LTE signal center at 2 GHz.

**Session A3P-K: VLSI Design, Simulation and Testing I**

**Chair:** Carlos Silva Cardenas, *Pontificia Universidad Católica del Peru*

**Time:** Monday, August 4, 2014, 14:50 - 15:40

**Location:** Poster Area

**Don't Cares based Dynamic Test Vector Compaction in SAT-ATPG** ..... 213

*Kareem Habib (Mentor Graphics Corporation), Mona Safar (Ain Shams University),  
Mohamed Dessouky (Mentor Graphics Corporation), Ashraf Salem (Mentor Graphics Corporation)*

SAT solvers have been used as ATPG solution due to the advantage of transforming the circuit to a mathematical problem that can quickly be solved rather than using traditional circuit based approach. In this paper, we present a novel technique for dynamically compacting the test vector set in SAT-based ATPG as it searches for individual vectors, hence giving out fewer patterns that cover more faults. Three-valued encoding was used to allow the use of don't cares, a value that is not part of the traditional SAT solver approach. Experimental results compare the traditional approach with the one proposed.

**Fixing Power Bugs at RTL Stage using PSL Assertions** ..... 218

*Carla Purdy (University of Cincinnati), Chandan Singh (University of Cincinnati),  
Rashna Seli (STMicroelectronics)*

Power dissipation has now become the most critical design constraint. In the design flow of an SoC, power estimation and analysis usually come into the picture only after the completion of RTL synthesis. However, design optimization for low power is most suitable before synthesis. Each decrease in process geometry makes dynamic power targets harder to achieve. Also, changes made later in the design for power optimization lead to costly re-spin. It is better to pin-point power related problems in the design as early as possible when they can still be fixed. This also reduces risk by ensuring that the design meets power goals before embarking on its implementation. Our novel approach presented in this paper introduces power analysis at the RTL stage itself, using PSL assertions. This enables the SoC designer to optimize the design from a low power perspective at a very early stage (RTL) in the design flow, where the scope of modification is maximized and the cost minimized.



**Yield Aware Inter-Logic-Layer Communication in 3-D ICs: Early Design Stage Recommendations** ..... 222

*W. Gul (National University of Sciences and Technology), S.R. Hasan (Tennessee Technological University), O. Hasan (National University of Sciences and Technology)*

3-D IC provides more logic space by introducing multiple tier structure. Effective communication across the tiers can be very challenging. TSVs are utilized for signal propagation between multiple tiers. Different TSV allocation methodologies have been investigated. We have analyzed different TSV redundancies and provided some guidelines. It has been found that router based redundancy requires less number of cells as compared to its counterparts. But router based redundancy is hardware demanding as compared to 1:4 and 2:4 redundancies and requires extra time to adopt spare path. Moreover, router based redundancy has about three times redundant TSVs per cell than its counterpart redundancies.

**Average Placement Method with Common Centroid Constraints for Analog IC Layout Design** ..... 226

*Kunihiro Fujiyoshi (Tokyo University of Agriculture and Technology), Keitaro Ue (Tokyo University of Agriculture and Technology)*

To improve immunity against process gradients, a common centroid constraint, in which every pair of capacitors should be placed symmetrically with respect to a common center point, is widely used. Several methods to obtain a good placement satisfying the constraints were proposed. However, the distance between cells in a common centroid group may be redundantly long, and it degrades the immunity. In this paper, we propose a novel algorithm to place cells belonging to each common centroid group. The algorithm is simple, but it is proved to be effective.

**Comparative Study on Deconvolution Function Dependencies of RTN/RDF Effect Estimation Errors in Analyzing Sub-nm-Scaled SRAM Margins** ..... 230

*Hiroyuki Yamauchi (Fukuoka Institute of Technology), Worawit Somha (Fukuoka Institute of Technology)*

Comparative study between the proposed technique and MATLAB-built-in deconvolution-functions with regard to deconvolution errors is discussed, which have a crucial impact in reversing the effects of convolution with Random Telegraph Noise (RTN) and Random Dopant Fluctuation (RDF) on overall SRAM margin variations. The proposed algorithm successfully avoids noise amplification thanks to eliminating the need for any operations of differential, division, and maximum-likelihood gradient sequence. This advantage over the MATLAB-built-in deconvolution-functions has been demonstrated for the first time with applying it to a real analysis for the effects of the RTN/RDF on the overall SRAM margin variations. It has been shown that the proposed technique can reduce fail-bit-count estimation error based on the convolution of the deconvoluted-RTN with the RDF by  $10^{14}$ -fold compared with the MATLAB-built-in deconvolution-functions.

## **Session A3P-L: VLSI Design, Simulation and Testing II**

**Chair:** Carlos Silva Cardenas, *Pontificia Universidad Católica del Peru*

**Time:** Monday, August 4, 2014, 14:50 - 15:40

**Location:** Poster Area

**Sizing Analog Integrated Circuits by Combining gm=ID Technique and Evolutionary Algorithms** ..... 234

*Adriana Carolina Sanabria-Borbón (Instituto Nacional de Astrofísica, Óptica y Electrónica), Esteban Tlelo-Cuautle (Instituto Nacional de Astrofísica, Óptica y Electrónica)*

Automatic sizing of analog integrated circuits (ICs) remains an open challenge. This work shows a hybrid approach for finding optimal sizes of analog IC's elements, by combining the gm/ID technique for determining the parameter ranges for a given biasing levels, and using those to limit the search space through performing multi-objective optimization with evolutionary algorithms. That way, the NSGA-II optimization algorithm is employed to optimize the width (W) and length (L) of MOSFETs of an operational transconductance amplifier, which (W/L) search spaces are found by applying equations and biasing conditions to the gm/ID technique. From simulation results, we conclude on the appropriateness of gm=ID to accelerate the computational time of evolutionary algorithms for optimizing analog ICs.

**A New Real Pole Delay Model for RLC Interconnect using Second Order Approximation** ..... 238

*Muhammad Sanaullah (University of Missouri-Kansas City), Masud H. Chowdhury (University of Missouri-Kansas City)*

In this paper, a new time delay model is presented for the case real poles in RLC interconnect for a step input. The proposed delay model is based on the second order approximate transfer function of distributed RLC interconnect network. The proposed model would be an efficient analytical tool to estimate RLC interconnect behavior. The results indicate that the real pole model is much faster than the previously developed complex pole model.

**Low-Power Loop Pipelining Mapping onto CGRA Utilizing Variable Dual VDD** ..... 242

*Bing Xu (Tsinghua University), Shouyi Yin (Tsinghua University), Leibo Liu (Tsinghua University), Shaojun Wei (Tsinghua University)*

Coarse Grained Reconfigurable Architectures (CGRAs) are promising platform based on its high-performance and low cost. Researchers have developed efficient compilers for mapping compute-intensive applications on CGRA using modulo scheduling. In order to generate loop kernel, every stage of kernel are forced to have the same execution time which is determined by the critical PE. Hence non-critical PEs can decrease the supply voltage according to its slack time. The variable Dual-VDD CGRA incorporates this feature to reduce power consumption. Previous work mainly focuses on calculating a global optimal VDDL using overall optimization method that does not fully exploit the flexibility of architecture. In this paper, we adopt variable optimal VDDL in each stage of kernel concerning their pattern respectively instead of the fixed simulated global optimal VDDL. Experiment shows our proposed heuristic approach could reduce the power by 19.5% on average for the loops of GPS, MPEG2, H.264 and audio video coding standard (AVS) without decreasing performance. The additional compilation time is negligible. The area penalty of this method is less than 3%

**Three Dimensional Robot Path Planning using a Field Programmable Analog Array** ..... 246

*Scott Koziol (Baylor University), Richard Wunderlich (Qualcomm Inc.), Jennifer Hasler (Georgia Institute of Technology)*

A reconfigurable analog integrated circuit is used to solve for a robot's path from a start point to a goal point among obstacles in a three dimensional environment. A bipartite grid algorithm is used to deterministically find a mapping from an arbitrary gridspace environment representation map with freespace and obstacles into transistors which implement the map on the reconfigurable analog circuit. 100% correct solutions were found using our hardware for sixteen Monte Carlo experimental cases.

**Power-Rail ESD Clamp Circuit with Embedded-Trigger SCR Device in a 65-nm CMOS Process** ..... 250

*Federico A. Altolaguirre (National Chiao-Tung University), Ming-Dou Ker (National Chiao-Tung University)*

SCR is the preferred ESD protection device in nanoscale CMOS technologies due to the better area efficiency compared the BIGFET, virtually no leakage current and smaller capacitance. The main drawback of the SCR is the slow turn-on speed, which is solved by adding dummy gates to block the STI formations inside the SCR structure. This work demonstrates that the dummy gate inside the SCR can be effectively used as an embedded trigger transistor, eliminating the need of an external trigger transistor in the ESD protection circuit and so further reducing silicon area and standby leakage current.

**Session A4L-A: Amplifiers**

**Chair:** Paul Furth, *New Mexico State University*

**Co-Chair:** Tina Wang, *Iowa State University*

**Time:** Monday, August 4, 2014, 15:40 - 17:20

**Location:** Mockingbird

**Analysis and Design of PWM-in-PWM-Out Class D Amplifiers** ..... 254

*Linfei Guo (Nanyang Technological University), Tong Ge (Nanyang Technological University), Yang Kang (Nanyang Technological University), Huiqiao He (Nanyang Technological University), Joseph Chang (Nanyang Technological University)*

A PWM-in PWM-out (Pulse-Width-Modulation) Class-D Amplifier (CDA) can directly receive digital PWM signals, hence not requiring DAC(s) as the 'interface' to digital signal-processing circuits. We have analytically investigated the distortion and Power-Supply-Rejection-Ratio (PSRR) of a PWM-in PWM-out CDA. We find that, contrary to conventional CDAs, the PWM-in PWM-out CDA features zero intrinsic distortions, and its PSRR is dependent on switching frequency but not the loop-gain. The derived analytical expressions are verified on the basis of HSPICE simulations. Furthermore, we show that the PWM-in PWM-out CDA is superior over a conventional CDA both in terms of Total-Harmonic-Distortion and PSRR.

**An Effective Conductance Cancellation Method with Minimal Design Effort** ..... 258

*Bin Huang (Iowa State University and Maxim Integrated Products Inc.), Degang Chen (Iowa State University)*

An easy-to-implement conductance cancellation method is proposed. To be specific, the only design work involved in the proposed method is to size a transistor in the negative conductance of the NMOS side. In addition, under all process corners, the method is able to maintain a DC gain enhancement of over 28.9dB under temperatures between -40 and 80°C, of over 27.6dB under supply voltage between 1.4V and 2V, and of over 29dB under differential output swing between -1.1V and 1.1V. Furthermore, the power and area overhead of the method are respectively only 7% and 3% of those of conventional op amps.

**Sequential Interstage Correlated Double Sampling: A Switched-Capacitor Technique for High Accuracy Systems** ..... 262

*Pedram Payandehnia (Oregon State University), Hamidreza Maghami (Oregon State University), Xin Meng (Oregon State University), Gabor C. Temes (Oregon State University), Hirokazu Yoshizawa (Saitama Institute of Technology)*

A novel sequential inter-stage correlated double sampling technique has been proposed. This technique provides considerable enhancement in the effective accuracy of a switched-capacitor architecture. Superior accuracy and thermal noise performance is achieved compared to the conventional correlated double sampling technique. The proposed approach provides higher input signal bandwidth by reducing the number of clock phases using a predictive phase compared to the other sequential techniques to achieve the same performance. Also, the proposed approach has the capability of driving both resistive and capacitive loads

**An Investigation Into the Effect of Carrier Generators on Power Supply Noise in PWM Class D Amplifiers** ..... 266

*Huiqiao He (Nanyang Technological University), Tong Ge (Nanyang Technological University), Linfei Guo (Nanyang Technological University), Joseph S. Chang (Nanyang Technological University)*

Class D amplifiers are ubiquitous as audio amplifiers due to their significantly higher power-efficiency compared to their linear counterparts (such as Class AB) due to the digital-like switching mode operation of the Class D output stage. However, one drawback of Class D amplifiers is the susceptibility to supply noise, qualified and quantified by Power Supply Rejection Ratio (PSRR) and Power Supply Induced Intermodulation Distortion (PS-IMD). Poor PSRR and PS-IMD may result in audible noise at the output and this is particular the case when the Class D amplifier is integrated with in an SoC (System on a Chip) where the power supply is usually noisy. In this paper, PSRR and PS-IMD of Single-ended, 2-state bridge-tied load (BTL) and 3-state BTL Class D amplifiers based on various Carrier Generators are investigated and compared. We show that the design of the carrier generator is critical and should be designed according to the structure of the Class D amplifier " we show in this paper that the same Carrier Generator may result in >70dB PSRR in the 3-state BTL Class D amplifier but a mere 1dB PSRR in the 2-state BTL Class D amplifier.

**A Simple Slew Rate Enhancement Technique with Improved Linearity and Preserved Small Signal Performance** ..... 270

*Bin Huang (Iowa State University and Maxim Integrated Products Inc.), Degang Chen (Iowa State University)*

A simple yet very effective slew rate enhancement (SRE) method is proposed. The proposed SRE feedback is off for small signal operation to preserve an amplifier's small signal performance, and is activated to enhance slew rate (SR) and linearity only when an amplifier is slewing. The new SRE scheme applies to both single-stage and multi-stage, both single-ended and fully differential amplifiers. Compared with a conventional OTA, the OTA with the proposed SRE scheme shows SRE by a factor of 23.2, THD improvement of 6dB and preserved small signal performance with only 1.2% area and 2% power consumption overhead. Compared with the adaptive biasing method, the proposed scheme shows 300% SR improvement, 18dB THD improvement but with power and area consumption decreased by 11.1% and 25% respectively.

**Session A4L-B: Advances in Device Modeling and Circuits for Special Applications**

**Chair:** Marvin Onabajo, *Northeastern University*

**Time:** Monday, August 4, 2014, 15:40 - 17:20

**Location:** Ballroom – 5

**High Voltage Charge Pump with Triple Well Diodes in a 0.13  $\mu\text{m}$  Bulk CMOS Process** ..... 274

*Jiwei Sun (Clemson University), Pingshan Wang (Clemson University)*

This paper presents charge pump circuits with modified triple well diodes as charge transfer switches for charging on-chip pulse generation circuits in a low-voltage bulk CMOS process. Guard-rings and isolation deep n-wells are used to improve the breakdown voltages and reduce leakage currents of the diodes. Model parameters of the triple well diode are extracted based on measured diode characteristics. These parameters are then used to analyze our charge pump. The proposed charge pump circuits are implemented in a commercial 0.13  $\mu\text{m}$  bulk CMOS process. The output voltage of the four-stage charge pump circuit can be up to 18.1 V, which is much higher than the n-well/p-substrate breakdown voltage ( $\sim 10$  V) of the given process.

**Comparison of MOSFET Mismatch Models with Random Physical and Random Model Variables** ..... 278

*Srijita Patra (Iowa State University), Randall Geiger (Iowa State University)*

A comparison between two established MOSFET mismatch modeling approaches, one based upon the use of uncorrelated random physical variables and one based upon the use of correlated random model variables where the correlation is ignored, is presented. An analytical formulation is introduced that enables the designer to easily predict the relative errors in matching performance that will occur if the more popular random model parameters are used instead of the uncorrelated physical parameters. It is shown that neglecting the correlation inherent in the random model variables will result in under-estimate of the area required for meeting a fixed yield target but in the example process considered in this paper, the errors introduced by using the correlated model parameters are small.

**Reduction in the Area of a High Voltage Multiplexer** ..... 282

*Shankar Thirunakkarasu (Broadcom Corporation), Robert E. Seymour (Texas Instruments Inc.)*

A high-voltage 16-channel, 16-bit settling, multiplexer is proposed with reduced area and better Total Harmonic Distortion (THD) and Crosstalk. Every conducting switch in this multiplexer is capable of handling +/-12V input with a constant low resistance across the entire input voltage range using a boosted-gate technique with +/-15V power supply to have better THD. The proposed multiplexer is simulated using 0.6um highvoltage thick-gate CMOS technology and verified through extensive spectre simulations. Layout was drawn and backannotated simulations were done to verify its working.

**A 1.8  $\mu$ W Area-Efficient Bio-Potential Amplifier with 90 dB DC Offset Suppression** ..... 286

*Jinyong Zhang (University of Hong Kong), Shing-Chow Chan (University of Hong Kong),  
Lei Wang (Shenzhen Institutes of Advanced Technology)*

An area-efficient and low-power low-noise amplifier with adjustable parameters for bio-potential recording applications is presented. This amplifier replaces traditional analog filters using large AC coupling capacitor with a novel DC offset suppression block based on Differential Difference Amplifier (DDA) structure, which allows the system to obtain good high pass characterization without using any area-consuming capacitors or resistors. It features configurable gain and bandwidth, which is suitable for various bio-potential applications and massive integration in medical devices. More than 90 dB DC offset suppression ratio is achieved in rejecting large DC offset and baseline drift that exist at the skin-electrode interface. The proposed bio-amplifier, designed in a 0.18  $\mu$ m CMOS process and occupies only 0.027 mm<sup>2</sup> area on chip, provides adjustable mid-band gain of 35.5/41.5/47.6/53.6 dB, tunable bandwidth from 0.01 Hz to 10 kHz. The back-annotated simulation results demonstrated the input-referred noise of 5.4  $\mu$ Vrms over 0.01 Hz-10 kHz and the total power dissipation consumed as low as 1.8  $\mu$ W at 1.2 V power supply.

**A SPICE Model for Perimeter-Gated Single Photon Avalanche Diode** ..... 290

*Mohammad Ullah Habib (University of Tennessee), Khandaker A. Al Mamun (University of Tennessee),  
Nicole McFarlane (University of Tennessee)*

In this work a comprehensive SPICE model is demonstrated for perimeter-gated single photon avalanche diodes (PGSPAD) fabricated in commercial 0.5  $\mu$ m CMOS process. This model simulates the trigger of an avalanche event of PGSPAD due to photon absorption, along with the quenching behavior. It also simulates the I-V characteristic where the breakdown voltage can be modulated with applied gate voltage. The modeling parameters are experimentally extracted from fabricated PGSPADs. This model simulates both the static and dynamic behaviors of the device. Simulated results are validated with experimental data to demonstrate the accuracy of the model.

## **Session A4L-C: FPGA and Digital Hardware Design**

**Chair:** Nader Rafla, *Boise State University*

**Time:** Monday, August 4, 2014, 15:40 - 17:20

**Location:** North & South 40

**Full Custom Implementation of a S-Box Circuit Architecture using Power Gated PLA Structure** ..... 294

*Ho Joon Lee (Northeastern University), Yong-Bin Kim (Northeastern University), Kyung Ki Kim (Daegu University)*

Advanced Encryption Standard (AES) is one of the most common symmetric encryption algorithms. The hardware complexity in AES is dominated by AES substitution box (S-Box), which is considered as one of the most complicated and costly part of the system because it is the only non-linear structure. This paper presents a low power design of Rijndael S-Box for the SubByte transformation using power-gating and PLA design techniques to reduce area and leakage power during standby mode. The proposed design has been implemented using 0.11um CMOS process with 1.2V power supply. The proposed design reduces the total leakage power and the total transistor count to 10% and 50% of the conventional design, respectively while improving the speed performance by ten times.

**Adaptive Real-Time DSP Acceleration for SoC Applications** ..... 298

*Pascal Nsame (Polytechnique Montréal), Guy Bois (Polytechnique Montréal),  
Yvon Savaria (Polytechnique Montréal)*

This paper investigates VLSI architectures for digital processing (DSP) functions amenable to low energy operation with scalable performance for H.265 high efficiency video coding (HEVC) applications. First, we describe and experimentally evaluate a novel adaptive computing fabric. Second, we propose an energy-efficient method to scale the performance of the fabric for large images or for meeting stringent real-time computation requirements. A series of tradeoffs for exploiting efficiently the application space for general purpose DSP acceleration are proposed. We experimentally show how the proposed computing fabric is re-usable for Filters, FFT and DCT acceleration with a scalable throughput. We report on the design and implementation of the fabric on a Xilinx FPGA device and show how regulated- parallelism augmented with in-memory processing techniques impact performance and power efficiency. The FPGA prototype demonstrates a sustained throughput exceeding 10Gbps irrespective of the kernel and image size for H.265 HEVC applications.



**A Framework to Quantify FPGA Design Hardness Against Radiation-Induced Single Event Effects** ..... 302

*David S. Lee (University of Southern California), Jeffrey Draper (University of Southern California)*

This paper describes ongoing research pertaining to the analysis of design radiation hardness for circuits implemented in Field-Programmable Gate Array (FPGA) devices. Radiation induces single event effects in FPGAs that can cause erroneous operation by upsetting data bits or changing logic behavior. Design-level techniques can mitigate these upsets to some degree; however, there is currently no method available to quantify the benefit of these techniques. This research is developing a framework to score designs for upset hardness. Additionally, this framework will determine the most susceptible locations in design netlists that would most benefit from additional design mitigation against upset.

**Identification of Trojans in an FPGA using Low-Precision Equipment** ..... 306

*Trey Reece (Vanderbilt University), Bradley T. Kiddie (Vanderbilt University),  
William H. Robinson (Vanderbilt University)*

Hardware Trojans pose a difficult threat to hardware systems due to the difficulty in their identification. In many cases, the differences observed between Trojan and Trusted chips can be very small. This research explored the feasibility of using low-precision test equipment in order to identify malicious modifications to circuits programmed to Field Programmable Gate Arrays (FPGAs). Examination using an ELVIS II Instrumentation board was able to correctly classify ISCAS85 c6288 multipliers based on their internal structure, allowing for identification of suspect designs. These tests were conducted in the context of the 2012 Cyber-Security Awareness Week Embedded Systems Challenge.

## **Session A4L-D: Devices and Circuits for Health Monitoring I**

**Chair:** Aydin Karsilayan, *Texas A&M University*

**Time:** Monday, August 4, 2014, 15:40 - 17:20

**Location:** Ballroom – 6

**A Multichannel Corticospinal Interface IC for Intracortical Spike Recording and Distinct Muscle Pattern Activation via Intraspinal Microstimulation** ..... 310

*Shahab Shahdoost (Case Western Reserve University), Pedram Mohseni (Case Western Reserve University),  
Shawn Frost (University of Kansas Medical Center), Randolph Nudo (University of Kansas Medical Center)*

This paper reports on a corticospinal interface IC as a core building block for next-generation integrated neural interfaces targeted at functional recovery from spinal cord injury. Fabricated in 0.35um 2P/4M CMOS, the IC integrates a 2-channel, 10b, neural-recording front-end with digitally programmable gain and bandwidth, and a 4-channel, constant-current, stimulating back-end for delivering programmable trains of charge-balanced monophasic or asymmetric biphasic current pulses up to ~100uA. The IC functionality is demonstrated in vivo by low-noise recording of extracellular neural spikes from an anesthetized rat's cerebral cortex, and by distinct muscle pattern activation in the rat's hindlimb facilitated via intraspinal microstimulation.

**A Smart Capsule for In-Body pH and Temperature Continuous Monitoring** ..... 314

*Zhexiang Chi (Tsinghua University), Hanjun Jiang (Tsinghua University), Jinpei Xia (Tsinghua University),  
Heng Liu (Tsinghua University), Zhaoyang Weng (Tsinghua University), Jingjing Dong (Tsinghua University),  
Kai Yang (Tsinghua University), Zhihua Wang (Tsinghua University)*

A smart capsule for in-body pH and temperature continuous monitoring is presented, for non-invasive gastrointestinal examination. The whole system consists of a smart capsule for pH value and temperature sensing, and a portable data logger. Two chips, ADC and transceiver, and MCU is applied in the system. The power consumption is low and accuracy of the capsule system is high.

**A Low-Power PPM Demodulator for Remotely Powered Batteryless Implantable Devices** ..... 318

*Enver G. Kilinc (École Polytechnique Fédérale de Lausanne), Catherine Dehollain (École Polytechnique  
Fédérale de Lausanne), Franco Maloberti (Università degli Studi di Pavia)*

A low-power PPM demodulator has been developed for remotely powered batteryless implantable devices. The required power is harvested by the magnetic coupling with external powering coils placed under the living space of the animal. The remote powering is turned off only 1% of a bit duration during data transmission. The PPM demodulator consumes only 22.7 μW at 1.8 V and has 5.55 kb/s data rate. Entire system and basic blocks integrated using a 0.18 μm CMOS technology are presented. Experimental results show the effectiveness of the PPM demodulator and the communication system.



**Design of an NFC Enabled Bio-Patch Solution** ..... 322

*Ricardo Zepeda (Texas Instruments Inc.), Rafael Mena (Texas Instruments Inc.)*

This paper addresses the design and implementation of an NFC enabled bio-patch solution. The design serves as a prototype for a flexible solution that would adhere to the skin. The bio-patch design incorporates a combination of sensor solutions which enable on-skin temperature measurements and galvanic skin response (GSR) monitoring. The bio-patch design consists of a single chip solution based on the RF430FRL152H device from Texas Instruments. The device handles the sensor signal conditioning, processes the sensor data, enables data-logging of the sensor data via on-board ferroelectric random access memory (FRAM) and provides the RF communication link through near field communication (NFC) to an available gateway, in this case an Android NFC enabled handset. The bio-patch can operate with or without a battery power source. Without a battery, the bio-patch is functional when in proximity of the gateway, scavenging the RF energy of the radiating element through inductive coupling. As part of the system solution, an Android app was developed to collect the information and thus provide a link to the Internet of Things.

**A Fast Fabricating Electro-Wetting Platform to Implement Large Droplet Manipulation** ..... 326

*Yiyang Li (University of Nevada-Las Vegas), Roger Chen (Genia Corporation),*

*R. Jacob Baker (University of Nevada-Las Vegas)*

Droplet actuation, merging, and splitting using controlled electro-wetting are implemented on the top of a standard printed circuit board (PCB) resulting in a fast prototyping microfluidic platform for biological experiments. Results show that lower actuation voltages and frequencies are achieved, than previously reported, to move larger droplets (30 microliter). Single-plate and dual-plate techniques are compared showing that a single-plate system can utilize lower voltages while at the same time being simpler to construct. The platform is designed for tissue immunohistochemistry staining experiments.

**Session A4L-E: Advances in Energy and Power ICs**

**Chair:** Hoi Lee, *University of Texas, Dallas*

**Co-Chair:** Ayman Fayed, *Iowa State University*

**Time:** Monday, August 4, 2014, 15:40 - 17:20

**Location:** Ballroom – 7

**A Switched Mode Li-Ion Battery Charger with Multiple Energy Harvesting Systems Simultaneously used as Input Sources** ..... 330

*Judy Amanor-Boadu (Texas A&M University), Mohamed Abouzied (Texas A&M University), Salvador Carreon-Bautista (Texas A&M University), Roland Ribeiro (Texas A&M University), Xiaosen Liu (Texas A&M University), Edgar Sanchez-Sinencio (Texas A&M University)*

Energy harvesting is a green source of energy which can help reduce the maintenance cost in the frequent replacement of batteries, reduce pollution, and enable the long term powering of devices in places that are not easily accessible. In recent past, systems have been proposed to use energy harvesting systems to charge energy storage devices. This paper presents a simple but effective solution to combine multiple energy harvesting systems simultaneously for battery charging. This ensures the effective use of environmental energy for the powering of microsystems at all times. The proposed system has a monitoring interface, which monitors the energy harvesting systems' outputs, combined with a battery charger to charge a Li-ion battery, thereby providing an approach which ensures that the battery can always be charged using green energy. The simulation of the system's behavior takes into account the variable nature of the different energy harvesting sources to ensure that the presented system is a viable option when dealing with multiple energy harvesting systems and Li-ion battery charging.

**Harvesting the Highest Power from Tiny Electrostatic Transducers with CMOS Circuits** ..... 334

*Joshua J. Cowan (Georgia Institute of Technology), Gabriel A. Rincón-Mora (Georgia Institute of Technology)*

Although energy in vibrations is often vast, the electrostatic force with which tiny variable capacitors draw power from motion is miniscule, so output power is low. Thankfully, extracting energy at higher voltages generates more power because the electrical damping force that impedes motion to draw power is stronger. Clamping the transducer to a battery is convenient in this respect, but limiting because battery voltages are low. Using a capacitor to clamp the transducer to a higher voltage is better, but only to the extent that capacitance keeps that voltage from reaching the breakdown level of the switches. In fact, when neglecting parasitic power losses in the switches and the controller, a grounded clamping capacitor can yield up to 100% of the theoretical maximum power, and up to 87% with 2.5 nF, 15-V switches, and a 3.3-V battery from a 30"250-pF transducer at 27.6 Hz. Under similar conditions, this paper also shows that battery-clamped and asynchronous and stacked capacitor-clamped systems generate 4%, 17%, and 53%.

**A Self-Regulated 588 MHz Buck Regulator with On-Chip Passives and Circuit Stuffing in 65nm** ..... 338  
*Wei Fu (Iowa State University and Texas Instruments Inc.), Ayman Fayed (Iowa State University)*

A fully-integrated 588MHz buck regulator with 20nH and 300pF on-chip inductor and capacitor in 65nm is presented. It operates from 1.8V input and produces between 0.8V to 1.2V output with maximum load of 30mA. The regulator's footprint is cut by 50% by employing circuit stuffing where the entire regulator's circuitry is implemented underneath the inductor. The regulator employs a self-regulation loop that improves its efficiency and ensures the reliability of its low-voltage power transistors. It occupies 0.12mm<sup>2</sup> with a peak efficiency of 60%, and achieves up to 13.7% better efficiency than an LDO as well as very fast dynamic response.

**Design Techniques for External Capacitor-Less LDOs with High PSR Over Wide Frequency Range** ..... 342  
*Chang-Joon Park (Texas A&M University), José Silva-Martinez (Texas A&M University), Marvin Onabajo (Northeastern University)*

the paths for power supply noise leakage in low drop-out (ldo) voltage regulators are analyzed, and techniques are discussed to minimize their effects on the output voltage. an internally compensated high power supply rejection (psr) ldo voltage regulator with adaptive supply noise compensation scheme is presented. its regulated output voltage is 1.6 v to provide 0-50 ma of current with a power supply of 1.8 v. the measured psr is better than -50 db up to 4 mhz. the fabricated ldo occupies 0.25 mm<sup>2</sup> in a 0.18 μm cmos technology. it consumes 80 μa of ground current. the load regulation for a 50 ma step with 100 ns rise/fall times is 200 mv.

**Building High-Frequency High-Voltage Switching Converters for Renewable Energy Systems** ..... 346  
*Zhidong Liu (University of Texas at Dallas), Jing Xue (University of Texas at Dallas), Lin Cong (University of Texas at Dallas), Hoi Lee (University of Texas at Dallas)*

This paper presents various circuit techniques and design considerations for high-voltage integrated switching converters to enable their high-frequency operation, thereby minimizing the converter cost, weight and volume. First, the design considerations of realizing a low-power and high-speed synchronous gate driver for power FETs are explained in order to allow the power converter operating in the MHz range with negligible power efficiency degradation. The high-speed high-accuracy high-voltage sense-FET based current sensor to monitor the peak inductor current is also discussed. To demonstrate above circuit techniques, a 40-V 9.6-W buck converter is implemented in a high-voltage 0.35-um CMOS process with dual on-chip power nFETs. The proposed converter can operate at 2 MHz. The peak power efficiency of the proposed converter is 93%, while the converter can still provide >90% efficiency under the full-load of 9.6 W at 2 MHz.

**Session A4L-F: SPECIAL SESSION: Smart Energy and Security**

**Chair:** Shiyuan Hu, *Michigan Technological University*

**Co-Chair:** Jiang Hu, *Texas A&M University*

**Time:** Monday, August 4, 2014, 15:40 - 17:20

**Location:** Brazos

**Can the SHIELD Protect our Integrated Circuits?** ..... 350  
*Farinaz Koushanfar (Rice University), Ramesh Karri (New York University Polytechnic School of Engineering)*

Mass production of Integrated Circuits (ICs) from a single blueprint (mask) renders inherent identification of the individual parts a challenge. Indelible marking of the ICs can enable fingerprinting, identification, authentication, metering, and tracing of components along the unascertained semiconductor supply chain. To enable these important objectives, a recent call by DARPA is soliciting innovative research proposals for a SHIELD that enables advanced supply chain hardware authentication capability. This paper discusses the SHIELD desiderata, threat model and its potential for addressing a number of standing challenges in this area. We emphasize on the dire need for open evaluations and thorough security analysis of the SHIELD.

**Optimal PMU Placement for Identification of Multiple Power Line Outages in Smart Grids** ..... 354  
*Jie Wu (Missouri University of Science and Technology), Jinjun Xiong (IBM T.J. Watson Research Center), Prasenjit Shil (Ameren Corporation), Yiyu Shi (Missouri University of Science and Technology)*

Placing the appropriate numbers of PMUs is critical to collect phase angle data for identifying multiple line outages in wide-area transmission system based on high installation costs and limited PMU resources. This work focuses on exploring the global optimum PMU locations for maximizing the average identification capability of multiple line outages. Inspired by Kullback-Leibler (KL) distance, this paper proposes the closed form mathematical model to describe the average identification capability of multiple simultaneous line outages. Using IEEE 14-bus system, the optimal trade-off between the average identification capability and the number of PMUs is characterized. The proposed model of average identification capability successfully portrays the statistical identification performance of multiple line outages. The numerical result shows that the global optimal PMU placement algorithm has the higher average dissimilarity distance when compared to the random PMU placement algorithm.

**Partially Solar Powered Full Electric Vehicles** ..... 358

*Jaemin Kim (Seoul National University), Donkyu Baek (Korea Institute of Science and Technology), Jeongmin Hong (Korea Institute of Science and Technology), Naehyuck Chang (Korea Institute of Science and Technology)*

Electric Vehicles (EV) are known to have three times more energy efficient than petroleum internal combustion engine (ICE) vehicles. This is true if we do not consider electricity generation, transmission and vehicle battery charging efficiency. ICE vehicles have various vendor-specific technologies regarding fuel efficiency including engines, transmissions and their matching. EV, on the other hand, fuel efficiency is largely dependent on the vehicle weight thanks to simplified drivetrain such as direct drive without a transmission. Nevertheless, true energy efficiency of EV should be justified by the source of electricity. This paper introduces a custom, light-weight EV prototype for partial solar powered EV. We demonstrate the custom energyefficient EV prototype and possibility of partially solar-powered EV. I

**Dynamic Programming based Game Theoretic Algorithm for Economical Multi-User Smart Home Scheduling** ..... 362

*Lin Liu (Michigan Technological University), Yuchen Zhou (Michigan Technological University), Yang Liu (Michigan Technological University), Shiyan Hu (Michigan Technological University)*

Smart home becomes an emerging research topic these years. It offers various advantages such as facilitating the control of home appliances and the reduction of electricity bill. In this paper, a dynamic programming based game theoretic algorithm is proposed for multiple user smart home scheduling which can handle home appliances with multiple discrete power levels. The simulation results on test cases of 1000 to 5000 users demonstrate that our algorithm using game theory can achieve reduction of monetary cost of energy consumption by 29% on average comparing to the algorithm without game theory. In addition, our algorithm produces more balanced energy consumption.

**Model-Based Synthesis for Real-Time Embedded Systems** ..... 366

*Qi Zhu (University of California, Riverside)*

Model-based design is being increasingly used in the development of real-time embedded control systems due to its capabilities to support early design verification and validation through formal functional models. Similarly as in the case for circuit design, to facilitate the adoption of high level functional models and truly reduce design complexity, it is important to have automated synthesis tools that can generate correct and optimal implementations from those functional models. The development of such synthesis tools has some unique challenges compared to synchronous circuit design - the functional model for real-time embedded systems has more diverse semantics, the implementation platform is more distributed and often asynchronous, and there are strict timing requirements along with a variety of other design objectives.

**Tuesday, August 5, 2014**

**Session B1P-G: Sensors and Oscillators**

**Chair:** Jin Liu, *University of Texas at Dallas*

**Time:** Tuesday, August 5, 2014, 9:20 - 10:10

**Location:** Poster Area

**A 230ns Settling Time Type-I PLL with 0.96mW TDC Power and Simple TV Calculation Algorithm** ..... 370

*Ja-Yol Lee (Electronics and Telecommunications Research Institute), Mi-Jeong Park (Electronics and Telecommunications Research Institute), Hyun-Kyu Yu (Electronics and Telecommunications Research Institute), Cheon-Soo Kim (Electronics and Telecommunications Research Institute)*

This paper describes a fast-settling all-digital PLL with a low-power TDC based on retimed reference clock and a lock detector focused on monitoring a toggling phase error. With the intention of reducing power dissipation, the proposed TDC employs the low-rate reference and retimed reference clocks to measure the fine fractional phase error between the low-rate reference and high-rate oscillator clocks. In addition, the use of the retimed reference clock to the TDC results in a new simple DCO clock period calculation algorithm which employs the maximum and minimum values for the fractional error correction. A lock detector, which is required to accomplish the switchover of the DCO frequency tuning mode, allows a fast settling to be actuated independent of loop bandwidth and frequency step. By dissipating 8mW at 1.2-V supply voltage, the proposed digital PLL achieves 230ns settling time, 1.7psrms period jitter.

**A Low-Noise and Low-Power Voltage-Controlled Oscillator** ..... 374

*Choong-Eui Lee (Sungkyunkwan University), Bai-Sun Kong (Sungkyunkwan University)*

This paper presents a low-noise low-power voltage-controlled oscillator (VCO). The power consumption of the VCO is reduced by eliminating the redundant current flowing through the cross-coupled latch. The phase noise is also reduced by minimizing signal transition period in which noise current has critical impact on the phase noise. The proposed VCO is implemented in a 65-nm CMOS technology, whose evaluation results indicate that the proposed VCO operates from 982MHz to 1.64GHz with up to 34% less power consumption and up to 1.93 dBc/Hz less phase noise as compared to the conventional low-noise VCO.

**A Very Low Power 7.9 Bit MEMS Pressure Sensor Suitable for Batteryless RFID Applications** ..... 378

*A. Beriain (Universidad de Navarra), H. Solar (Universidad de Navarra), R. Berenguer (Universidad de Navarra), J.A. Montiel-Nelson (Universidad de Las Palmas de Gran Canaria), J. Sosa (Universidad de Las Palmas de Gran Canaria), R. Pulido (Universidad de Las Palmas de Gran Canaria), S. García-Alonso (Universidad de Las Palmas de Gran Canaria)*

There is a strong motivation for the development of new low power sensors for wireless passive applications such as RFID. In this work, a combination of a MEMS capacitive pressure transducer and a capacitive to digital converter compatible with a sensor enabled RFID tag are presented. The MEMS transducer has been designed and fabricated using a MetalMUMPs process. Its characterization showed an output variation between 9.3 pF and 13.4 pF corresponding to a pressure variation between 0 kPa and 30 kPa, with a INL of 0,2%. On the other hand, the capacitance to digital converter has been implemented in a low cost 2P4M 0.35 $\mu$ m CMOS standard process. The interface measurements showed a resolution of 7.8 bit and an average power consumption of 16.56  $\mu$ W. Combining both devices together with a sensor enabled RFID tag, a long range passive RFID sensor for pressure measurements up to 30 kPa could be implemented.

**A CMOS based  $\mu$ -Power Smart Temperature Sensor for On-Chip Thermal Monitoring** ..... 382

*Shailesh Singh Chouhan (Aalto University), Kari Halonen (Aalto University)*

A low-power smart temperature-sensor has been developed using 0.18 $\mu$ m standard CMOS process. The sensor utilizes the dependency of rising time of the output pulse of an inverter, on drain current when triggered by a fixed frequency square wave. The working temperature of the proposed architecture is -40 degC to +85 degC with the maximum power dissipation of 4.276mW. The measured accuracy of the proposed architecture after single point calibration is between +/-1.25 degC.

**A Novel Readout Circuit for On-Sensor Multispectral Classification** ..... 386

*Javad Ghasemi (University of New Mexico), Payman Zarkesh-Ha (University of New Mexico), Sanjay Krishna (University of New Mexico), Sebastian E. Godoy (University of New Mexico), Majeed M. Hayat (University of New Mexico)*

A new readout integrated circuit (ROIC) for multispectral classification is presented. The ROIC is designed to utilize the spectral response tunability of dot-in-a-well (DWELL) infrared photodetector to exploit the possibility of real-time on-chip multispectral imaging for classification in analog domain. The unit cells are designed to include all necessary elements needed for spectral classification, including high-voltage time-varying positive and negative biases, bipolar integration, and selective sample-and-hold circuits. A test chip was designed and fabricated using TSMC's 0.35  $\mu$ m high-voltage technology. The test chip has successfully completed its initial functional tests and is ready for hybridization to a DWELL focal-plane array.

**A Time-Encoding CMOS Capacitive Sensor Readout Circuit with Flicker Noise Reduction** ..... 390

*Fernando Cardes (Universidad Carlos III de Madrid), Luis Hernandez (Universidad Carlos III de Madrid), Javier Escobar (Universidad Carlos III de Madrid), Andreas Wiesbauer (Infineon Technologies), Dietmar Straeussnigg (Infineon Technologies), Richard Gaggl (Infineon Technologies)*

This paper shows a novel capacity to digital measurement circuit that is suited for differential MEMS capacitive sensors such as pressure sensors or condenser microphones. The basic operating principle relies on two differential reactance-controlled multivibrator circuits whose frequency differences are sensed by a Time to Digital Converter. The multivibrator oscillators may be biased in the relaxation oscillation mode, where demodulated flicker noise is greatly attenuated by large scale excitation of CMOS transistors. The paper shows a system level description of the readout circuit, a full transistor design in 0.13 $\mu$ m CMOS and an oscillator characterization from measurements on a discrete demonstration circuit.



## Session B1P-H: Techniques, Simulation, Modeling and Testing

**Chair:** Jin Liu, *University of Texas at Dallas*

**Time:** Tuesday, August 5, 2014, 9:20 - 10:10

**Location:** Poster Area

### **Analog Signal Processing in Deep Submicron CMOS Technologies using Inverters** ..... 394

*K.R. Raghunandan (University of Texas at Austin), Nan Sun (University of Texas at Austin),*

*T.R. Viswanathan (University of Texas at Austin)*

Analog signal-processing in deep sub-micron technologies poses many challenges arising from both low supply voltage and intrinsic voltage-gain of short channel devices. Class- AB CMOS transconductance obtained by a pair of complementary transistors is a widely used power efficient building block because it has linear  $v/i$  characteristics. This is topologically the same as the logic inverter of CMOS digital systems. This block enables the basic signal-processing operations of addition, subtraction, scaling and integration. Replica-circuits are used to keep the large process, voltage and temperature (PVT) variations under control. Thus we can perform analog signal-processing at a level of precision required for designing high-speed data communication systems. This paper discusses this in a canonical fashion. Simulation results using device models for 65 nm CMOS process are presented to validate these ideas.

### **Bootstrapping Techniques for Floating Switches in Switched-Capacitor Circuits** ..... 398

*Xin Meng (Oregon State University), Gabor C. Temes (Oregon State University)*

Bootstrapping techniques improve the linearity of switched-capacitor circuits, especially for low supply voltage. This paper proposes simple but effective techniques for bootstrapping floating switches. The method is applicable to such fundamental circuits as sample-and-hold (S/H) stages, switched-capacitor (SC) filters and SC amplifiers. It can make the on-resistance and channel charge of the switches independent of the signal, and hence enables linear operation even for low bias voltages.

### **Implementation of High Performance Readout Integrated Circuit** ..... 402

*Hari Shanker Gupta (Indian Institute of Technology Bombay), Subhananda Chakrabarti (Indian Institute of Technology Bombay), Maryam Shojaei Baghini (Indian Institute of Technology Bombay), D.K. Sharma (Indian Institute of Technology Bombay), A S Kiran Kumar (Space Applications Centre), Sanjeev Mehta (Space Applications Centre), Sandip Paul (Space Applications Centre), Ravi Shankar Chaurasia (Space Applications Centre), Arup Roy Chowdhury (Space Applications Centre)*

The Read out Integrated Circuit (ROIC) consists of charge integration, charge to voltage conversion, Pixel voltage multiplexing, signal transfer and amplification stage. The IR detectors requires the integration of large charge handling capacity  $>10M^+$ , at the same time sensitive enough to detect signals just above the noise floor of better than 900". The design and measured results of 4x4 array ROIC chip with 10 M" charge handling capacity , 30 $\mu$ m pixel pitch, snapshot mode of operation, variable integration time, 3 Mpps readout rate and readout noise of 350" reported at ambient temperature and discussed in the paper.

### **Challenges and Opportunities for Determining Presence of Multiple Equilibrium Points with Circuit Simulators** ..... 406

*Qianqian Wang (Iowa State University), Randall L. Geiger (Iowa State University),*

*Degang J. Chen (Iowa State University)*

Challenges of using standard circuit simulators to determine the presence or absence of undesired operating points are discussed. Examples are given of circuits and simulation strategies that show the presence of undesired operating points when they exist but other examples are given that show the same strategies can fail to show the presence of undesired operating points under modestly different simulation conditions. Since many of the most widely used analog and mixed-signal circuits that are known to be vulnerable to the multiple equilibrium point problem have no standard electrical inputs, it is shown that a temperature sweep may be useful in some applications for identifying the presence of undesired operating points.

### **A 5-Gb/s Adaptive CTLE with Eye-Monitoring for Multi-Drop Bus Applications** ..... 410

*Somanshu Agarwal (International Institute of Information Technology, Hyderabad),*

*Vijaya Sankara Rao Pasupureddi (International Institute of Information Technology, Hyderabad)*

On-chip data processing capabilities have increased very rapidly over the last decades creating off-chip bandwidth a strong limiting factor. Limitations of this off-chip communication originate from interconnect, vias and connectors leading to reflections over chip-to-chip interconnect and leads to intersymbol interference. These variations dynamically change based on interconnect length, number of vias and connectors, needing adaptive equalization. This scenario becomes more worse and unpredictable in a multi-drop bus environment, leading to complete eye closure. In this work, we propose a 5 Gb/s adaptive continuous time linear equalizer (CTLE) with eye-monitoring in a multi-drop bus environment. The coefficients of CTLE are adjusted to compensate the channel nonlinearities based on the feedback received from the eye-monitoring device. Adaptive CTLE is designed in 1.8V, 0.18 $\mu$ m CMOS technology for 5 Gb/s data transmission over a 7.5 inch FR4 PCB trace. The power consumed by adaptive CTLE is 18mW for a bit error rate of  $10^{-12}$ .



<b>A CMOS Short Pulse Generator with a High-Voltage Stacked MOSFET Switch</b> .....	414
<i>Jiwei Sun (Clemson University), Pingshan Wang (Clemson University)</i>	

This paper presents a CMOS short pulse generator with a high-voltage stacked MOSFET switch, which is developed to overcome the low breakdown voltage limitations of CMOS processes. The six stacked MOSFET switch is fabricated in a 0.13  $\mu\text{m}$  CMOS process. The measurement results agree with simulation results reasonably well. A CMOS short pulse generator circuit with 5 mm pulse-forming-line (PFL) is also implemented with the switch. Pulses of  $\sim 2.44$  V amplitude and  $\sim 122$  ps duration on a 50  $\Omega$  load are obtained. The discrepancies between measurements and anticipated results (i.e. 4.8 V output with 77 ps pulse duration) include measurement connection system and parasitic effects.

## **Session B1P-J: Linear and Non-Linear Circuits and Systems**

**Chair:** Samuel Palermo, *Texas A&M University*

**Time:** Tuesday, August 5, 2014, 9:20 - 10:10

**Location:** Poster Area

<b>Memcapacitor based CMOS Neural Amplifier</b> .....	418
<i>A.H. Madian (German University in Cairo), S.H. Moustafa (German University in Cairo), H.E. El-Kolaly (German University in Cairo)</i>	

In this paper, a CMOS neural amplifier based on memcapacitor has been realized. A memcapacitor is a new element based on memristor theory. A performance comparison between memcapacitor based realization and conventional integrated one has been introduced. The circuits were simulated using 90nm CMOS technology for a total input referred noise of 1.97  $\mu\text{Vrms}$  when using memcapacitors for a range of frequency from 0.013Hz to 10 kHz. The simulation shows a good performance with a smaller size compared to the conventional integrated capacitors.

<b>Calculation of Closing Impedance in Feedback Systems based on Cut-Insertion Theorem</b> .....	422
<i>I.M. Filanovsky (University of Alberta), B. Pellegrini (Università di Pisa)</i>	

The cut-insertion theorem allows one obtain the parameters of one-loop feedback system (i.e. the system of order one) resulting from insertion into a cut the two-port providing preservation of the currents and voltages in the rest of network. Yet practical application of this theorem is limited by calculation of the impedance closing one side of the cut (it should be obtained, in general, from an algebraic equation with polynomial coefficients which are very difficult to calculate). The paper shows how to circumvent this difficulty: using the cut-inserted two-port which includes an independent current (voltage) source on one side of the cut and an independent voltage (current) source on the other side one obtains the signal graph of the feedback system of order two. The closing impedance is then directly calculated using the Mason's formula and the branch transmissions of this graph. Then other parameters of the equivalent one-loop system such as loop gain, transfer function, etc., can be easily found.

<b>Mixed Numerical and Analytical Analysis of Nonlinear Circuits with Nonsmooth Inputs: A Hyperbolic Algebra Approach</b> .....	426
<i>Wieslaw Marszalek (DeVry University), Zdzislaw Trzaska (Warsaw University of Ecology &amp; Management)</i>	

A mixed numerical and analytical analysis of oscillatory non-harmonic solutions of nonlinear circuits with nonsmooth inputs is presented. The focus of the paper is on using hyperbolic algebra in the analysis of nonlinear circuits with periodic nonsmooth inputs of the square or triangular wave types. The numerical aspect of our approach relies on verifying periodic solutions in those cases when analytical analysis is not possible or cumbersome. Several illustrative examples are presented.

<b>Digital Post-Distortion Linearization of Wideband Wireless Receiver Nonlinearity</b> .....	431
<i>Ifiok Umoh (Santa Clara University), Tokunbo Ogunfunmi (Santa Clara University)</i>	

In this paper, we develop a new digital postdistortion technique for linearizing wideband wireless receiver nonlinearity primarily from the low noise amplifier (LNA) in Software Defined wireless (SDR) systems. This goal is achieved by combining an adaptive digital post-distorter in the transceiver in such a way as to compensate for interference resulting from the LNA's. The proposed technique simultaneously maintains the good performance characteristics of inductively degenerated common source (CS) LNAs' base SDR transceiver while improving linearity. We show an improvement in IIP3 by a factor greater than 7:8dB in the worst case and as high as 16:8dB. Since this technique is applied to the digital base-band, the number of components and therefore the size and cost of analog parts of the LNA is reduced.

<b>A Hybrid Chaos-Based Pseudo-Random Bit Generator in VHDL-AMS</b> .....	435
<i>Michal Melosik (Poznan University of Technology), Wieslaw Marszalek (DeVry University)</i>	

A new pseudo-random bit generator with an increased level of security and possible resistance to hacker attacks is presented. The generator is based on hybrid (analog and digital) chaotic systems. We also use the VHDL-AMS language in modeling of both the chaotic systems and generator. The 0/1 test for chaos is applied to evaluate the generator's performance. Examples of the chaotic signal responses obtained from VHDL-AMS are included.

## Session B1P-K: Power Management Techniques I

**Chair:** Ayman Fayed, *Iowa State University*

**Time:** Tuesday, August 5, 2014, 9:20 - 10:10

**Location:** Poster Area

### **A New Stepwise Adiabatic Charging Circuit with a Smaller Capacitance in a Regenerator than a Load Capacitance** ..... 439

*Shunji Nakata (Kinki University), Hiroshi Makino (Osaka Institute of Technology), Yoshio Matsuda (Kanazawa University)*

A stepwise-voltage-generation circuit was devised that is based on a capacitor bank and that dissipates no energy when a stepwise voltage is generated. The stepwise voltage is generated spontaneously, and depends neither on the initial voltages to the capacitors nor on the switching order. A new adiabatic-charging circuit based on this circuit was also devised that increases the voltage in a stepwise fashion. The total capacitance of the capacitors in the regenerator is much smaller than a load capacitance, which enables construction of a very small adiabatic regenerator. This regenerator cannot be made with a conventional circuit, which uses a tank capacitor that is much larger than a load capacitor for adiabatic charging.

### **Analysis and Comparison of Two Active Anti-Islanding Detection Methods** ..... 443

*Xiao Li (Texas A&M University), Robert S. Balog (Texas A&M University)*

Anti-islanding detection is essential for grid connected inverter to avoid substantial safety accident. Many Anti-islanding methods available now are proposed based on ideal grid and load conditions. Then most of them have weaknesses as high sensitivity to grid distortion in grid-connection state. This will certainly limit their wide application in some aspects. Active Frequency Drift (AFD) and Reactive power variation method (RPV) are two promising active anti-islanding detection methods. In this paper, the performance of these two methods under various extreme conditions are considered and compared, including different grid distortion conditions, different loading conditions.

### **Power Gyration Structures: Versatile Cells for Energy Processing in Photovoltaic Solar Facilities** ..... 447

*Herminio Martínez-García (Universitat Politècnica de Catalunya)*

This paper provides a classification of high efficiency switching power-gyration structures and their use as cells for energy processing in photovoltaic solar facilities. Having into account the properties of these topologies presented in the article, their inclusion in solar facilities allows increasing the performance of the whole installation. Thus, the design, simulation and implementation of a G-type power gyration are carried out throughout the text. In addition, in order to obtain the maximum power from the photovoltaic solar panel, a maximum power point tracking (MPPT) is mandatory in the energy processing path. Therefore, the practical implementation carried out includes a control loop of the power gyration in order to track the aforementioned maximum power point of the photovoltaic solar panel.

### **Investigation of Reactive Power Limit Induced Voltage Collapse** ..... 451

*Hung-Ming Chou (Texas A&M University), Garng M. Huang (Texas A&M University), Karen L. Butler-Purry (Texas A&M University)*

Voltage instability is caused by the inability of the system to meet reactive power demand. The problem of voltage instability is even more critical for an isolated microgrid, which only has generators with limited reactive power capacities. In this paper, we investigated what happens if all generators in the system hit their reactive power limit. To simplify the analysis, a simple two-bus example was used. Analytical power flow solutions was derived, and the corresponding physical interpretation was discussed. The physical constraints of the generator determined whether the power flow solution is feasible. It was found that when the reactive power limit of the generators is hit, even though there is a power flow solution, due to the physical limitation of the generator, no feasible solution exists. This causes the system to experience voltage collapse.

## Session B1P-L: Power Management Techniques II

**Chair:** Ayman Fayed, *Iowa State University*

**Time:** Tuesday, August 5, 2014, 9:20 - 10:10

**Location:** Poster Area

### **Design of a Linear-Assisted DC-DC Switching Regulator with Constant Switching Frequency** ..... 455

*Herminio Martínez-García (Universitat Politècnica de Catalunya)*

This article shows the proposal of a linear-assisted converter or linear-switching hybrid converter with a constant switching frequency. The control loop of the system is based on the current-mode technique. The main disadvantage of a converter with current-mode control is the inherent instability of the loop when switch duty ratios are greater than 0.5. In order to make stable the proposed linear-assisted converter, the article shows the technique based on a slope compensation.

**A Dual-Input Forward Converter for Downhole Drilling Applications** ..... 459

*Ruichen Zhao (Baker Hughes Incorporated), Steven A. Morris (Baker Hughes Incorporated), Alexis Kwasinski (University of Texas at Austin)*

Due to the harsh environment and increasing power consumption downhole, few existing power generation technologies could independently meet the power generation needs and reliability requirements. With multiport converters, multiple power sources can be efficiently integrated and may also achieve higher reliability, higher efficiency, and component saving. In the proposed topology, an auxiliary input is integrated and independently controlled by merely adding a diode and a MOSFET to a dual-switch forward converter. Additionally, the auxiliary input leg virtually works as a conventional forward converter and shares the resetting diodes with the original leg.

**Power Losses and Efficiency Analysis of the Quadratic Buck Converter in CCM** ..... 463

*Agasthya Ayachit (Wright State University), Marian K. Kazimierczuk (Wright State University)*

This paper presents the derivation of the efficiency and the steady-state dc voltage transfer function of the lossy quadratic buck converter operating in the continuous conduction mode (CCM). The effect of variation in the duty cycle and load resistance on the efficiency and dc voltage transfer function will be discussed. Conduction loss for every component in the circuit will be derived and the total converter losses will be expressed as functions of the duty ratio and the output power. A design of the quadratic buck converter with an output voltage of 10 V at an output power of 10 W operating at a switching frequency of 100 kHz is considered to illustrate the analysis. The results will be compared with that of the conventional buck dc-dc converter. It will be shown that, both the topologies have comparable efficiencies over the entire load range.

**SmartShelter: A Sustainable Power System Design using Energy Harvesting Techniques** ..... 467

*Leticia Ibarra (Texas A&M University), Benjamin Hilton (Texas A&M University), Mehna Nawal (Texas A&M University), Salvador Carreon-Bautista (Texas A&M University), Mohamed Abouzied (Texas A&M University), Xiaosen Liu (Texas A&M University), Roland Ribeiro (Texas A&M University), Judy Amanor-Badu (Texas A&M University), Ethan Miller (Texas A&M University), Jorge Vanegas (Texas A&M University), Edgar Sanchez-Sinencio (Texas A&M University)*

In the event of a large-scale natural disaster, families and nations are often unprepared for post-disaster living conditions. Disaster relief shelters are inadequate replacements for destroyed homes; the crowded living space stimulates the spread of illnesses and the lack of electricity exacerbates psychological stress. A modernized shelter equipped with electricity and structural integrity would address several issues imposed by current disaster relief shelter. Using micro-energy harvesting techniques, a SmartShelter has the ability to locally generate minimal amounts of electricity and provide adequate protection for natural disaster victims. Through its novel design, the SmartShelter utilizes solar, thermal, piezoelectric, and radiofrequency energy harvesting modules to sustain electricity generation and strategically support structural integrity. As a proof-of-concept design, a prototype SmartShelter is proposed using commercially available energy harvesting modules. With this prototype, it will be proven that micro-energy harvesting techniques may be utilized to generate sufficient amounts of power to sustain a low-power generating system.

**Session B2L-A: References and Oscillators**

**Chair:** Jin Liu, *University of Texas at Dallas*

**Time:** Tuesday, August 5, 2014, 10:10 - 11:50

**Location:** Mockingbird

**Effects of Non-Ideal Characteristics of Substrate BJT on Bandgap Reference Circuits** ..... 471

*Rui Bai (Iowa State University), Randall L. Geiger (Iowa State University)*

This paper explores the non-ideal characteristics of bipolar junction transistor (BJT) on band gap reference circuit. First, the base spreading resistors (BSR) in a BJT have a significant impact on voltage reference. Given the temperature dependence of the resistors, the impacts on the voltage reference becomes more considerable. Secondly, the forward current gain ( $\beta$ ) is temperature dependent which causes a variation in voltage reference. Finally, the different layout techniques of a BJT will affect the accuracy of the voltage reference, which includes the contacts positions, finger numbers and the geometry of the emitter. With a BSR BJT model, the voltage reference increases by 20%. Considering the temperature dependence of  $\beta$ , the inflection point increases by around 30 °C and the sensitivity changes by 25 ppm/°C. Furthermore, different layout techniques will change the effective BSR, which causes a shift of the voltage reference.

**A CMOS Supply-Insensitive with 13ppm/°C Temperature Coefficient Current Reference** ..... 475

*Yen-Ting Wang (Iowa State University), Degang Chen (Iowa State University), Randall L. Geiger (Iowa State University)*

A simple all CMOS low temperature coefficient current reference is designed. Two opposite temperature coefficient supply-insensitive self-bias reference generators that have a function of threshold voltage, mobility and resistor are utilizing to compensate the first-order and second-order temperature curvature. The proposed circuit is designed in AMI 0.5 $\mu$ m process with 5V supply voltage over the temperature range of -45°C to 125 °C. The proposed circuit achieves a 16 $\mu$ A current with temperature coefficient of 13ppm/°C, the supply variation of the designed current is  $\pm 1.2\%$  over  $\pm 10\%$  Vdd change and the accuracy over process variation is  $\pm 4.1\%$ .

**0.7 V Supply, 8 nW, 8 ppm/°C Resistorless Sub-Bandgap Voltage Reference** ..... 479

*Oscar E. Mattia (Universidade Federal do Rio Grande do Sul), Hamilton Klimach (Universidade Federal do Rio Grande do Sul), Sergio Bampi (Universidade Federal do Rio Grande do Sul)*

In this work a new resistorless sub-bandgap voltage reference topology is presented. It is a self-biased and small area circuit that works in the nano-ampere consumption range, and under 1 V of power supply. The behavior of the circuit is analytically described, a design methodology is proposed and simulation results are presented for a standard 0.18  $\mu\text{m}$  CMOS process. A reference voltage of 463 mV is demonstrated, with a temperature coefficient of 8 ppm/C for the 0 to 125 C range, while the power consumption of the whole circuit is 8.25 nW under a 0.75 V supply at 27 C. The estimated silicon area is 0.0043 mm<sup>2</sup>.

**Quadrature Error of Two-Integrator Oscillators** ..... 483

*João Casaleiro (Universidade Nova de Lisboa), Luis B. Oliveira (Universidade Nova de Lisboa), Igor M. Filanovsky (University of Alberta)*

The demand for small-size multi-standard receivers leads to the design of modern receiver architectures with wide tuning range. The performance of these receivers is related to the image rejection ratio, which makes the improvement of the quadrature accuracy mandatory. Hence, minimizing the quadrature error of the receiver's quadrature oscillator is an important goal. In this work, we analyse the sources of quadrature error in the two-integrator oscillator, working in quasi-sinusoidal regime, and propose compensation techniques to minimize the error. Simulation results confirm the amplitude and phase error equations, and show that the quadrature error can be reduced with no impact on the phase noise. We show that the quadrature error increases with the amplitude and circuit component mismatches, and decreases with the amplifier's gains. Based on the theoretical analysis, a novel quadrature error compensation technique to minimize the quadrature error is proposed.

**A Low Power and Low Distortion VCO based ADC using a Pulse Frequency Modulator** ..... 487

*Eric Gutierrez (Universidad Carlos III de Madrid), Luis Hernandez (Universidad Carlos III de Madrid), Ulrich Gaier (Lantiq A GmbH), Sergio Walter (Lantiq A GmbH), Liang Zou (Lantiq A GmbH)*

This paper shows a novel VCO based ADC which uses an inverter delay line as a monostable to implement a pulse frequency modulator. The inverter delay line doubles as a Time to Digital converter, providing a multibit digital output similar to a ring oscillator. The pulse frequency modulator is based on a gm-C integrator, operating as a closed loop transconductor for the low bandwidth input signal path and as a charge pump for the monostable feedback. This way a high linearity is achieved while the total power consumption is kept on the order of a calibrated VCO-ADC. The paper shows first the basic system level operation and behavioral simulations, and also a transistor level design example in 0.25 $\mu\text{m}$  CMOS technology.

## **Session B2L-B: Design and Analysis of Linear and Non-Linear Systems**

**Chair:** Samuel Palermo, *Texas A&M University*

**Time:** Tuesday, August 5, 2014, 10:10 - 11:50

**Location:** Ballroom – 5

**Simulations of 3rd Order Voltage Switched CP-PLL using a Fast Event Switching Macromodeling** ..... 491

*Ehsan Ali (Aix-Marseille University), Wenceslas Rahajandraibe (Aix-Marseille University), Fayrouz Haddad (Aix-Marseille University), Christian Hangmann (Universität Paderborn), Christian Hedayat (Fraunhofer-Institut für Elektronische Nanosysteme)*

In this paper, the transient behavior of the 3rd order VSCP-PLL is investigated using an event-driven (ED) macro-modeling technique. Since the ED-technique has a very short simulation time and is computer resource efficient. Due to its inherent competency, the off-locking behavior of the system can easily be characterized. Related to the VSCP-PLL architecture, some features are highlighted and further extended to compare its performance with an equivalent PLL operating with a current switched charge-pump (CSCP). The simulations are performed using a piece-wise linear and non-linear VCO transfer characteristic.

**A Comparison of Continuous Time Sigma Delta Modulator Simulation Methods** ..... 495

*Kyung Kang (University of Nevada-Las Vegas), Peter Stubberud (University of Nevada-Las Vegas)*

Several common approaches for simulating continuous time sigma delta modulators (CT  $\Sigma\Delta\text{Ms}$ ) include SPICE modeling, solving differential equations, implementing difference equations based on impulse invariance and using Simulink. In this paper, the delta transform is used to determine difference equations which are used to simulate CT  $\Sigma\Delta\text{Ms}$ . This method's speed and accuracy are compared to the other afore mentioned methods with respect to the elapsed time of simulation and the signal to quantization noise ratio (SQNR), respectively.



**Corrected and Accurate Verilog-A for Linear Dopant Drift Model of Memristors** ..... 499

*Ahmed A. Emara (Cairo University), Mohamed M. Aboudina (Cairo University),  
Hossam A.H. Fahmy (Cairo University)*

There is an urgent need to develop accurate memristor circuit models for use in future large designs. Several Verilog-A and SPICE models have been presented which vary in their accuracy and simulation speed. This paper corrects a previous Verilog-A model and enhances the accuracy of another one. The results show that our proposal is stable over long simulation time, correctly predicts the behavior of circuits, provides a better accuracy, and is as fast as previous models. These results make our model the best choice for large memory or logic circuits designs using memristors.

**Verification of a Chaos-Based Random Number Generator through the Bootstrap** ..... 503

*Salih Ergün (TÜBİTAK National Research Institute of Electronics and Cryptology)*

A random number generation method based on a cross coupled chaotic oscillator is introduced. Numerical model for the proposed design has been developed where bootstrap method is utilized which allows us to estimate the statistical characteristics of underlying chaotic signal. Numerical results verifying the feasibility and correct operation of the random number generator are given such that numerically generated binary sequences fulfill FIPS-140-2 statistical test suites for randomness without post-processing. Presented random number generator features much higher and constant throughput rates and allows for offset compensation.

**Novel Dissipative Lagrange-Hamilton Formalism for LC/Van der Pol Oscillator with New Implication on Phase Noise Dependency on Quality Factor** ..... 507

*Bosco Leung (University of Waterloo)*

A novel method of doing co-ordinate transformation for LC/van der pol(vdp) oscillator is proposed. It allows vdp to be solved as a conservative system by applying Hamiltonian formulation using calculus of variation. The procedure is developed to calculate the constant of integration, a generalized concept of energy. Such constant of integration, which is different from energy, has implication on the dependency of phase noise on quality factor Q. This is examined, which shows that the traditional dependency on Q is not totally correct.

**Session B2L-C: VLSI Design and Simulation**

**Chair:** Nader Rafla, *Boise State University*

**Time:** Tuesday, August 5, 2014, 10:10 - 11:50

**Location:** North & South 40

**Post-Silicon Tuning Aware Wafer Matching Algorithm for 3D Integration of ICs** ..... 511

*Sangdo Park (Samsung Electronics), Taewhan Kim (Seoul National University)*

This work addresses the problem of wafer-to-wafer matching algorithm for 3D integration of ICs. One critical limitation of the traditional wafer matching methods is that they have attempted to maximize the number of resulting 3D ICs with no faulty (bad) die, but never took into account the time variation between the individual dies in a 3D integrated chip. We show that without considering time variation between dies as well as within wafers during wafer-to-wafer matching, a more aggressive post-silicon tuning is required with increased design cost or a reduced parametric yield of chips is resulted. To overcome this limitation, we propose a post-silicon tuning aware comprehensive wafer matching algorithm to improve the parametric yield of 3D chips. Through experiments with benchmark designs, it is shown that the proposed wafer matching algorithm is able to enhance the parametric yield by up to 8%.

**Modeling, Analyzing, and Abstracting Single Event Transient Propagation at Gate Level** ..... 515

*Ghath Bany Hamad (Polytechnique Montréal), Syed Rafay Hasan (Tennessee Technological University),  
Otmame Ait Mohamed (Concordia University), Yvon Savaria (Polytechnique Montréal)*

Soft errors have become one of the most challenging issues that impact the reliability of modern microelectronic systems at terrestrial altitudes. A new methodology to abstract, model, and analyze Single Event Transient (SET) propagation at different abstraction levels (transistor and gate level) is proposed. Transistor level characterization libraries are developed to abstract the impact of input patterns, pulse polarity, and propagation paths characteristics on the SET duration. Thereafter, these libraries are utilized to analyze SET pulse propagation at gate level using MDG model checker. We have implemented the proposed method on different ISCAS85 benchmark combinational circuits. The proposed methodology is orders of magnitude faster than circuit level simulations. Moreover, we have developed gate level characterization libraries to abstract SET pulse propagation behavior at the gate level.

**Efficient and Accurate RIE Modeling Methodology for BEOL 2.5D Parasitic Extraction** ..... 519

*Nur Kurt Karsilayan (Mentor Graphics Corporation), Jim Falbo (Mentor Graphics Corporation),  
Dusan Petranovic (Mentor Graphics Corporation)*

An efficient and accurate sensitivity based methodology is introduced for modeling reactive ion etch (RIE) in BEOL 2.5D parasitic extraction. Proposed methodology involves calibration of analytical equations based on layout parameters that are fitted to capacitance and sensitivity data from 2D field solver. Formulas are derived along with new capacitance and sensitivity equations in a 2.5D parasitic extraction framework. Calibration runtime is reduced due to sensitivity modeling while the overall BEOL accuracy is comparable to the case with no RIE effect. Proposed method has been validated over a wide range of technologies from 65nm to 20nm.



**An Evaluation of 6T and 8T FinFET SRAM Cell Leakage Currents** ..... 523

*Michael A. Turi (Pacific Lutheran University), José G. Delgado-Frias (Washington State University)*

We evaluate leakage currents of 6T and 8T FinFET SRAM cell schemes using shorted gate and low power FinFET configurations. Reverse-biasing the cross-coupled inverter FinFETs' back gates reduces leakage current by up to 97% and minimizes leakage variation due to parameter and temperature variations. The 6T Low-Power FinFET scheme uses these configurations and has lowest leakage; however, 8T SRAM schemes outperform 6T SRAM schemes since leakage can be reduced by schemes that reverse-bias the cross-coupled inverter FinFET back gates without reducing read speed or read static noise margin; the 8T Low-Power Inverters scheme has lowest leakage and energy-delay product.

**FDSOI SRAM Cells for Low Power Design at 22nm Technology Node** ..... 527

*Linbin Chen (Northeastern University), Fabrizio Lombardi (Northeastern University),*

*Jie Han (University of Alberta)*

The silicon-on-insulator (SOI) MOSFET is considered as an alternative to the bulk (silicon-based MOSFET in CMOS circuits for applications requiring low-voltage and low-power operation. Fully depleted SOI (FDSOI) benefits from a high current driven ability; so, this technology preserves advantageous features, such as steep sub threshold characteristics and small short channel effects. This paper presents a comprehensive assessment of different SRAM (Static Random Access Memory) cells utilizing different numbers of transistors (i.e. 8 and 9). These cells are evaluated by HSPICE for different performance metrics (such as write/read delay, stability, critical charge, power consumption and tolerance to voltage threshold variation) at the 22nm technology node

## **Session B2L-D: Devices and Circuits for Health Monitoring II**

**Chair:** Marvin Onabajo, *Northeastern University*

**Time:** Tuesday, August 5, 2014, 10:10 - 11:50

**Location:** Ballroom – 6

**An On-Chip Security Guard based on Zero-Power Authentication for Implantable Medical Devices** ..... 531

*Qing Yang (Tsinghua University), Songping Mai (Tsinghua University), Yixin Zhao (Tsinghua University),*

*Zhijun Wang (Tsinghua University), Chun Zhang (Tsinghua University), Zhihua Wang (Tsinghua University)*

In order to fight against severe risks of security and privacy for implantable medical devices, an on-chip security guard based on zero-power authentication is proposed and verified in this paper. The conception of 'zero-power' is realized by virtue of wireless power recovery instead of fetching power from primary battery. The security guard recovers both data and clock from external wireless signals based on amplitude shift keying pulse width modulation. It features a wireless data rate of 500 Kbps and no need for on-chip clock generator. The Hash encryption is adopted in authentication and features a 32-bit ALU to speed up the SHA-1 computation with an estimated peak power of about only 1 mW, which is affordable by wireless power recovery which has a capacity of several mW. FPGA and chip implementation verify the feasibility of this system.

**A Fully Integrated Low Noise CMOS Instrumentation Amplifier Design for Low-Power Biosensors** ..... 535

*Vighnesh Rudra Das (Texas Tech University and Texas Instruments), Donald Y.C. Lie (Texas Tech University),*

*Tam Nguyen (Texas Tech University)*

This paper presents the design of a monolithic low power CMOS low-noise instrumentation amplifier (INA) for low-power biosensor applications. To achieve high-fidelity cardiac signal acquisition, the INA circuit and system design requirements are discussed. Design strategies for mitigating the in-band flicker noise and thermal noise using chopper-stabilization and current scaling techniques are investigated. Sub-threshold operation is also utilized to reduce power. The INA achieves a simulated noise spectral density of 39.9 nV/ $\sqrt{\text{Hz}}$  from dc to 300Hz in 4.6 $\mu\text{W}$ , with an outstanding noise efficiency factor (NEF) of 2.47.

**Instrumentation Amplifier Input Capacitance Cancellation for Biopotential and Bioimpedance Measurements** ... 539

*Chun-Hsiang Chang (Northeastern University), Marvin Onabajo (Northeastern University)*

An instrumentation amplifier with a mechanism that generates negative capacitances at its input is presented. The architecture includes two digitally programmable capacitors between the input stage and the current feedback loop to cancel the input capacitances from the electrode cables and printed circuit board. The negative capacitance generation technique can improve the input impedance from a few mega ohms to above 500M $\Omega$  without significant impact on performance parameters such as the common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), total harmonic distortion (THD), and noise. A 93.6 $\mu\text{W}$  instrumentation amplifier was designed and simulated using IBM 0.13 $\mu\text{m}$  CMOS technology.

## Session B2L-E: Reconfigurable RF-CAS for RADAR, Cognitive Radio and EARS – I

**Chair:** Arjuna Madanayake, *University of Akron*

**Co-Chair:** Changzhi Li, *Texas Tech University*

**Time:** Tuesday, August 5, 2014, 10:10 - 11:50

**Location:** Ballroom – 7

### **Combined Time-Delay FIR and 2-D IIR Filters for Ears, Radar, and Imaging Applications** ..... 543

*Arjuna Madanayake (University of Akron), Sewwandi Wijayarathna (University of Akron), Chamith Wijenayake (University of Akron)*

A linear antenna array beamforming method which significantly improves the spatial selectivity of conventional phased/timed arrays is presented. A two-dimensional (2-D) infinite impulse response (IIR) digital beam filter is employed as a pre-processing stage to existing phased/timed arrays, thereby mathematically modifying the array transfer function. Introduction of a pre-filter is possible due to multi-input multi-output signal flow structure of the 2-D IIR beam filters, and the improvement in spatial selectivity is presented using closed-form frequency response and array pattern simulations. An example wireless communication scenario shows that the proposed beamformer leads to additional gain of more than 10 dB in terms of the BER vs. SIR performance.

### **Wideband LNA and Multi-Standard Frequency Synthesizer for Reconfigurable Radio** ..... 547

*Jinghong Chen (University of Arizona), Deping Huang (University of Arizona), Tienyu Chang (University of Florida), Jenshan Lin (University of Florida)*

This paper presents low-cost small-area DC-to-8GHz packaged and ESD-protected wideband LNAs and a wideband fractional-N frequency synthesizers implemented in CMOS technologies for reconfigurable radio applications.

### **Software-Configured Smart Radar Sensor for Civil and Biomedical Applications** ..... 551

*Guochao Wang (Texas Tech University), José-María Muñoz-Ferreras (Universidad de Alcalá), Roberto Gómez-García (Universidad de Alcalá), Changzhi Li (Texas Tech University)*

software has shown a much higher flexibility compared to hardware so as to be widely used in digital signal processing. In fact, the hardware and/or analog system can also gain merits from the flexibility of software. In this paper a hybrid radar system is described. Its transmitted signal as well as operating mode is digitally configured by software instead of conventional hardware one which is mainly decided by hardware. This method helps radar to break through some bottle necks radars have been long suffering. These chronic limitations used to be considered as hardware problems since they are directly related to some physical parameters of radars. In this paper, the presented software-configured radar system were tested in civil and bio-medical applications, demonstrates that this method can lead the radar as a mean of wireless sensor to the areas dominated by contact or invasive technology, or can further boost the performance in existing applications.

### **Switchless Matching Networks for Dual-Band Class-E Power Amplifiers** ..... 555

*Yifei Li (Iowa State University), Zhen Zhang (Iowa State University), Nathan M. Neihart (Iowa State University)*

This paper presents two different switchless (concurrent) dual-band load networks for class E power amplifier at 800 MHz and 1.9 GHz for 4G LTE standards. The two presented load structures, the all-lumped element and the transformer-based structure not only provide optimal impedance at both fundamental frequencies but also present high impedance up to their 3rd harmonics. Simulated PAEs for the all-lumped element and the transformer-based load network are above 62% and 57% with output powers of 26.5 dBm at 800 MHz and 1.9 GHz, respectively.

### **Dual-Band Microwave Power Amplifier Design using GaN Transistors** ..... 559

*Jin Shao (University of North Texas), David Poe (University of North Texas), Han Ren (University of North Texas), Bayaner Arigong (University of North Texas), Mi Zhou (University of North Texas), Jun Ding (University of North Texas), Rongguo Zhou (University of North Texas), Hyoungsoo Kim (University of North Texas), Hualiang Zhang (University of North Texas)*

This paper presents the design and the applications of dual-band microwave power amplifiers using GaN transistors. First, a dual-band power amplifier using dual-band transmission line (TL) impedance matching networks, which can simultaneously match two different complex impedances to 50  $\Omega$  at two uncorrelated frequencies, is introduced. Secondly, design of a dual-band GaN based Doherty power amplifier (DPA) is presented in this paper.

## Session B2L-F: Continuous-Time Filters

**Chair:** Igor Filanovsky, *University of Alberta*

**Time:** Tuesday, August 5, 2014, 10:10 - 11:50

**Location:** Brazos

### **On Design of Low-Voltage CMOS Current Amplifiers** ..... 563

*I.M. Filanovsky (University of Alberta), J.K. Järvenhaara (Tampere University of Technology),*

*N.T. Tchamov (Tampere University of Technology)*

The paper presents a new approach to design of current amplifiers. The amplifying cell core represents the connection of three transistors: a bias transistor and a differential pair. The bias transistor sets the distribution of currents in the differential pair. When an external current signal is applied to the core input the outputs of the differential pair provide two complementary current signals. The loading of the differential pair by a current mirror provides current conversion, and, depending on the current mirror orientation, one obtains a positive or negative current amplifying stage. These stages can be directly cascaded to obtain multistage high current gain amplifier. The gain of multistage amplifier may be stabilized using an external resistive current divider or external differential pair used as current distributor. The paper considers static and dynamic characteristics of the amplifying stages, and the frequency response of the two-stage amplifier. The amplifier was designed for 45 nm CMOS technology, the simulation was done using Cadence. The results of calculations and simulations are in a reasonable agreement.

### **Negative Impedance Inverter and All-Pass Filter Realizations using Adder and Subtractor Blocks** ..... 567

*Shahram Minaei (Dogus University), Merih Yildiz (Dogus University), Izzet Cem Gökknar (Dogus University),*

*Erkan Yuce (Pamukkale University)*

In this paper, using newly introduced analog adder and subtractor circuits, a new negative impedance converter, a lossy inductor simulator and an all-pass filter structure are presented. The proposed configurations have very simple structures containing only one or two adder/subtractor blocks together also with one or two passive elements. All capacitors used are grounded which is beneficial from the integrated circuit point of view and absorption of parasitic capacitors of the active blocks. The non-ideal analyses for all of the proposed circuits are given. Design examples for realizing 10 mH inductances are presented and tested with SPICE. The simulations are based on level 49 TSMC 0.25  $\mu\text{m}$  process parameters. The designed inductances show good performance between a few ten kHz to a few MHz. In addition inverting and non-inverting all-pass filter examples providing 90 degree phase shift at 790 kHz are given. The presented all-pass filters have high-input and low-output impedances resulting in easy cascadability. Frequency responses of the proposed all-pass filters are simulated to verify the theoretical analysis.

### **New Low-Voltage Low-Power VM All-Pass Filter using Current Follower with Non-Unity Gain** ..... 571

*Norbert Herencsar (Brno University of Technology), Jaroslav Koton (Brno University of Technology), Kamil Vrba*

*(Brno University of Technology), Shahram Minaei (Dogus University), Izzet Cem Gökknar (Dogus University)*

In this paper, a new realization of a first-order voltage-mode (VM) All-Pass Filter (APF) using a grounded capacitor, three resistors, and a single Current Follower (CF) with non-unity gain (i.e. four) is presented. The number of external resistors in the proposed VM APF can be reduced to two by considering the input intrinsic resistance of the CF as a useful active parameter. In comparison to the second-generation current conveyor-based current follower implementations employing large number of metal-oxide-semiconductor field-effect transistors (MOSFETs), here the used CF is composed of only four MOSFETs. Hence, it is favorable for low-voltage low-power circuit design. The APF was designed at pole frequency of 9.8 MHz with 112  $\mu\text{W}$  power consumption using PTM 90 nm level-7 CMOS process BSIM3v3 parameters and with  $\pm 0.5$  V DC voltages. SPICE simulation results are included to support the theory.

### **Design of RF Amplifier with Enhanced Performance** ..... 575

*M. Tanseer Ali (University of Greenwich), Ruiheng Wu (University of Greenwich)*

In this paper, a RF CMOS amplifier is designed on the basis of a novel negative impedance linearization technique with negative differential resistance (NDR) element. The simulation results show that the designed amplifier can achieve high gain accuracy, good linearity with improved efficiency, revealing that the proposed technique could find wider application in RF/Microwave circuits and systems.

### **A Novel Fully Differential Current Mode Universal Filter** ..... 579

*Alok Kumar Singh (Delhi Technological University), Pragati Kumar (Delhi Technological University)*

In this communication, one of the recently proposed active building block namely Current Differencing Current Conveyor (CDCC) has been used to design a current mode universal filters in fully differential form. The proposed universal filter has the property of independently tuneable gain, bandwidth and pole frequency. The number of passive elements used in this circuit is minimum when compared to other fully differential universal filter circuits with similar tuneability properties.

## Session B3L-A: Delta-Sigma Techniques I

**Chair:** R. Jake Baker, *University of Nevada, Las Vegas*

**Time:** Tuesday, August 5, 2014, 13:10 - 14:50

**Location:** Mockingbird

### **Comb Structures for Sigma-Delta ADCs with High Even Decimation Factors** ..... 583

*Gerardo Molina Salgado (Instituto Nacional de Astrofísica, Óptica y Electrónica), Gordana Jovanovic Dolecek (Instituto Nacional de Astrofísica, Óptica y Electrónica), José M. de la Rosa (Instituto de Microelectrónica de Sevilla / CSIC-Universidad de Sevilla)*

This paper analyses comb-based decimation structures for Sigma-Delta Analog-Digital Converters (ADCs), with high even decimation factors. The topology under study has two stages: the first stage is a non-recursive-comb and the second one is a CIC (Cascaded-Integrator-Comb) structure. As a result, efficient structures are identified in terms of the power consumption and silicon area. Additionally, alternative topologies are proposed to improve alias rejections of the analyzed decimator structures.

### **A Noise-Coupled Low-Distortion Delta-Sigma ADC with Shifted Loop Delays** ..... 587

*Xin Meng (Oregon State University), Yi Zhang (Oregon State University), Tao He (Oregon State University), Gabor C. Temes (Oregon State University)*

A low-power low-distortion delta-sigma modulator topology with shifted loop delay is proposed. Compared to the conventional low-distortion modulator, this topology can relax the critical timing for quantization and DEM by shifting the loop delay from the last integrator to the feedback path. Also, by adding one more feedback path, the last integrator can achieve both integration and active summation. Noise-coupled technique can also be utilized in the proposed modulator. To verify the effectiveness of this topology, a third-order noise-coupled delta-sigma modulator is analyzed and simulated.

### **High-Speed Low-Power Decimation Filter for Wideband Delta-Sigma ADC** ..... 591

*Yi Xie (Chinese Academy of Sciences), Minglei Zhang (Chinese Academy of Sciences), Baoyue Wei (Chinese Academy of Sciences), Xiaohua Fan (Chinese Academy of Sciences)*

This paper discusses the design of high-speed low-power decimation filter for wideband Delta-Sigma ADC. It presents a low power decimation filter with programmable decimation ratios (32, 64 and 128) and sampling rates (624MHz, 312MHz and 208MHz) for LTE application. The decimation filter has five different operating modes and consists of three sinc filters, two halfband filters and a FIR filter. It uses power efficient polyphase decomposition filter with a wise clock distribution approach to minimize power consumption. The decimation filter is implemented in 130 nm CMOS process, which consumes 0.46 mm<sup>2</sup> cell area. Simulation results show that when Sigma-Delta modulator output sampling frequency is 624MHz, 312MHz and 208MHz, it consumes less than 4.6mW, 2.3mW and 1.5mW from 1.2V supply respectively. In addition, they all achieve a Signal-to-Noise Ratio of 69dB over the signal bandwidth.

### **A Passive 2nd-Order Sigma-Delta Modulator for Low-Power Analog-to-Digital Conversion** ..... 595

*Angsuman Roy (University of Nevada-Las Vegas), R. Jacob Baker (University of Nevada-Las Vegas)*

A passive 2nd-order sigma-delta modulator based on a cascade of first-order lowpass filters was designed, fabricated, and tested. A lumped RC filter is added in the loop of a conventional 1st-order passive sigma-delta modulator in order to improve the linearity of its transfer function. A low power edge-triggered comparator was designed and fabricated along with lumped components in ON Semiconductor's C5 500 nm process. The implementation achieved a THD below 1% for all frequencies between 10 Hz and 5 kHz. With a 5 V supply the power consumption of the sigma-delta modulator is 64.5 uW to 150 uW depending on the input signal.

## Session B3L-B: RF Power Amplifiers

**Chair:** Kamran Entesari, *Texas A&M University*

**Time:** Tuesday, August 5, 2014, 13:10 - 14:50

**Location:** Ballroom – 5

### **A Built-in Calibration System to Optimize Third-Order Intermodulation Performance of RF Amplifiers** ..... 599

*Yongsuk Choi (Northeastern University), Chun-Hsiang Chang (Northeastern University), Hari Chauhan (Northeastern University), In-Seok Jung (Northeastern University), Marvin Onabajo (Northeastern University), Yong-Bin Kim (Northeastern University)*

A digital built-in calibration system is presented to automatically adjust the linearity of a tunable 2.4GHz low-noise amplifier (LNA). An envelope detector enables the extraction of linearity characteristics at low frequencies. The output of the detector is digitized before the spectrum calculation with an integrated fast Fourier transform (FFT) for estimation of the third-order intermodulation distortion of the LNA. The calibration scheme is demonstrated with simulations using a two-tone test signal, a 512-point FFT engine, a 10-bit analog-to-digital converter model, and digital blocks (implemented in 0.13um CMOS technology) operating with a 51.2MHz clock frequency. The total calibration time is 485us.



**A Load-Pull Approach using Multi-Frequency Harmonic Tuners for Enhancing PAE and Device Model Accuracy** ..... 603

*Mohamed El Mahalawy (Iowa State University and Rockwell Collins Inc.), Neven Misljenovic (Focus Microwaves Inc.), Ayman Fayed (Iowa State University)*

A load-pull process for characterizing and modeling devices used in switching microwave circuits is presented. The process employs state-of-the-art Multi-Harmonic Impedance Tuners that have the ability to control and sweep terminations at multiple harmonics simultaneously. As a result, the set of optimum harmonic terminations obtained from the proposed load-pull process results in higher PAE than the set obtained by the commonly-used load-pull processes that employ single-harmonic impedance tuners. Experimental results of a 0.25  $\mu\text{m}$  GaN device operating at 10 GHz show that an improvement of 11% in PAE is achieved with the optimum harmonic terminations obtained by the proposed approach.

**PWM with Differential Class-E Amplifier for Efficiency Enhancement at Back-Off Power Levels** ..... 607

*H.R. Khan (NED University of Engineering & Technology), A.R. Qureshi (NED University of Engineering & Technology), F. Zafar (NED University of Engineering & Technology), Qamar Ul Wahab (Linköping University)*

A simplified output matching network for pulse width modulated Class-E Power Amplifier for efficiency enhancement at back-off power level is proposed. The shunt capacitance and the series inductance in the Class-E PA are realized through capacitor banks that are tuned according to the duty cycle to meet ZVS conditions. The differential PA design is implemented in 130 nm CMOS technology achieving maximum Pout of 24.8 dBm at 1.8 GHz with PAE better than 38% at 50% duty cycle. The output power is modulated with the input duty cycle and provides 6.2 dB back-off power level keeping PAE almost constant around 38%.

**A 39.7 dBm and 18.5% PAE Compact X to Ku Band GaN Travelling Wave Amplifier** ..... 611

*Victor Dupuy (Université de Bordeaux), Eric Kerhervé (Université de Bordeaux), Nathalie Deltimple (Université de Bordeaux), Jean-Philippe Plaze (Thales Systèmes Aéroportés), Philippe Duême (Thales Systèmes Aéroportés), Benoit Mallet-Guy (Thales Systèmes Aéroportés), Yves Mancuso (Thales Systèmes Aéroportés)*

This article presents an 8GHz to 18GHz Travelling Wave Amplifier (TWA) averaging 39.7dBm of output power and 18.5% Power Added Efficiency (PAE). At 11 GHz, the TWA reaches a peak output power 40.4dBm and a peak PAE of 22%. The proposed architecture consists in the combination of two TWAs in parallel to increase output power. An innovative low loss compact power combiner is proposed to reduce the overall die size and keep high PAE. The amplifier presented here has the advantage to be very compact compared to similar MMICs High Power Amplifiers (HPA). An innovative design methodology based on a strong correlation between the amplifier and the combiner design is introduced.

**Compact Verilog-A Modeling of Silicon Traveling-Wave Modulator for Hybrid CMOS Photonic Circuit Design** ..... 615

*Kehan Zhu (Boise State University), Vishal Saxena (Boise State University), Wan Kuang (Boise State University)*

A compact Verilog-A model of silicon-based junction traveling-wave Mach-Zehnder interferometer (MZI) modulator is developed for hybrid CMOS and photonic system-level simulation in Cadence environment. Critical device functions such as the voltage dependent change of refractive index, small signal RLGC parameters for the MZI arms are extracted from the photonic device characterization from OpSIS foundry. Thermo-optical coefficient is also considered in the model. Simulation results including electro-optic S21 is characterized for the phase modulator's bandwidth. Also, transient MZI operation with non-return to zero (NRZ) data transmission at 10-Gb/s and 20-Gb/s rates are demonstrated.

**Session B3L-C: Systems and Hardware/Software Co-Design**

**Chair:** Zoran Stamenkovic, *IHP, Frankfurt*

**Time:** Tuesday, August 5, 2014, 13:10 - 14:50

**Location:** North & South 40

**Optimization of a Dot Product Accelerator** ..... 619

*Amitava Biswas (Cisco Systems)*

Vector dot product is an important computation which needs hardware accelerators. We present an optimized accelerator chip that has larger capacity than our prior designs. This design can compute product for 10000 component vectors within 1000 clock cycles, with average being 80 cycles. Our design has superior speed compared to other accelerators.



**A System-Level Design Approach for SDR-Based MPSoC in LTE Baseband Processing** ..... 623

*Shan Huang (Chinese Academy of Sciences), Ziyuan Zhu (Chinese Academy of Sciences),  
Yongtao Su (Chinese Academy of Sciences), Jinglin Shi (Chinese Academy of Sciences)*

This paper presents a system-level design approach from application perspective for an SDR based MPSoC in LTE baseband processing. A 0-1 knapsack model is proposed for hardware-software partition to enhance flexibility. A two-level frequency requirement is formed according to the characteristics of baseband processing to reduce power. Under this approach, the complex symbol based computation can be all realized on ASIP and the same MPSoC can serve LTE-A application by software programming. Moreover, the frequency of the ASIPs can be scaled down according to the requirement to get a power reduction from 6% to 90%.

**Trace-Driven Performance Estimation of Multi-Core Platforms** ..... 627

*Kyoungwon Kim (University of California, Irvine), Daniel D. Gajski (University of California, Irvine)*

Transaction Level Model (TLM) Estimation that uses TLM simulation is as fast as native simulation, cycle-approximate and applicable to both software and custom hardware so general. However, the entire platform is simulated for every platform selection and mapping. Trace-driven estimation reduces the simulation overhead but is not applicable to custom hardware and often requires Cycle Accurate Models (CAMs), which may not available for the whole platform. We present Trace-Driven Performance Estimation (TDPE) of multi-core designs. TDPE is a trace-driven estimation but also applicable to custom hardware and does not require CAMs, as accurate as but orders faster than TLM Estimation.

**Hierarchy-Aware Mapping of Pipelined Applications** ..... 631

*Kyoungwon Kim (University of California, Irvine), Daniel D. Gajski (University of California, Irvine)*

This paper presents hierarchy-aware mapping of a pipelined application to the heterogeneous platform. The applications we target are executed in a pipelined manner and can be captured with Model of Computations (MoCs) with explicit representations of pipelined execution. We minimize execution time. Balancing pipeline stages in the MoC is crucial. Previous works do not consider complex hierarchy in a stage of a general MoC. The primary contribution is to balance pipeline stages in the MoC by even partitioning hierarchically described pipeline stages. We compare ours to Hierarchy-Unaware mapping found by exhaustive search.

**A Kinect based Vibrotactile Feedback System to Assist the Visually Impaired** ..... 635

*Kumar Yelamarthi (Central Michigan University), Brian P. Dejong (Central Michigan University),  
Kevin Laubhan (Central Michigan University)*

This paper presents a Microsoft Kinect based vibrotactile feedback system to aid in navigation for the visually impaired. The lightweight wearable system interprets the visual scene and presents obstacle distance and characteristic information to the user. The scene is converted into a distance map using the Kinect, then processed and interpreted using an Intel Next Unit of Computing (NUC). That information is then converted via a microcontroller into vibrotactile feedback, presented to the user through two four-by-four vibration motor arrays woven into gloves. The system is shown to successfully identify, track, and present closest objects, closest humans, multiple humans, and perform distance measurements.

**Session B3L-D: BioSignal Processing**

**Chair:** Hoda S. Abdel-Aty-Zohdy, *Oakland University*

**Co-Chair:** Marvin Onabajo, *Northeastern University*

**Time:** Tuesday, August 5, 2014, 13:10 - 14:50

**Location:** Ballroom – 6

**Adaptive Signal Processing Techniques for Extracting Fetal Electrocardiograms from Noninvasive Measurements** ..... 639

*W.K. Jenkins (Pennsylvania State University), H. Ding (Pennsylvania State University), M. Zenaldin (Pennsylvania State University), A.D. Salvia (Pennsylvania State University), R.M. Collins (Bucknell University)*

In clinical medicine fetal electrocardiograms (ECGs) are useful for monitoring fetal health during pregnancy. This research investigates a variety of adaptive filtering techniques to remove maternal interference from fetal ECGs and to determine which techniques are most effective under varying circumstances. Experimental results suggest that a sequential combination of adaptive linear prediction coding (LPC), adaptive noise cancellation (ANC), and IIR comb filtering provides an effective strategy to remove maternal interference from fetal ECGs. It is shown how digital comb filters can be used effectively to separate maternal and fetal signal components based on distinct spectral content of the two signals.

**A 2.5-Mbps, 170-cm Transmission Distance IntraBody Communication Receiver Front End Design and its Synchronization Technique Research** ..... 643

*Hao Wang (Chinese University of Hong Kong), Jianfeng Wang (Chinese University of Hong Kong), Chiu Sing Choy (Chinese University of Hong Kong)*

This paper presents an IntraBody Communication (IBC) based receiver front end design combining conventional Binary Signal Recovery (BSR) module with Blind Oversampling Clock and Data Recovery (BOCDR) technique. The proposed receiver front end achieves high data speed-2.5Mb/s and long transmission distance-170cm with only  $1.84 \times 10^{-6}$  Bit Error Rate (BER). The measurement result shows its competitive performance to other similar work. The proposed IBC receiver front end scheme is also successfully applied to an FPGA based audio player, which will play a significant role of IBC application and commercialization.

**Wide Dynamic Range 653 nW CMOS Neurophysiological Signal Recording Micro-Brain-Implant with Opamp Sharing Technique** ..... 647

*Mohammad Poustinchi (McGill University), R. Greg Stacey (McGill University), Sam Musallam (McGill University)*

In this paper we present a low power, low noise CMOS micro-brain-implant which records both brain's electrical and chemical activities. We minimized the power consumption and silicon area by exploiting shared opamp technique. This wide dynamic range (85 dB) micro device consists of a single nano-watt power amplifier for both micromolar neurotransmitter sensing and micro voltage action-potential recording. It digitizes the signal to ten bits using a first order delta-sigma analog-to-digital-converter, all fabricated in TSMC CMOS-0.18 technology. This microsystem is validated applying neurophysiological signals.

**Design and Testing of D4 Wavelets Integrated Chip Preprocessor for Chemical Classifications** ..... 651

*Stephanie Roth (Oakland University), Hoda S. Abdel-Aty-Zohdy (Oakland University)*

The Daubechies 4 wavelet is used for compressing and filtering non-periodic signals and is use in our system for pre-processing data from 32 sensors, which is sent to a spiking neural network for chemical classification. The preprocessor features a Daubechies 4 wavelet processor and SPI bus, providing a standard interface for use with other components. Experimental measurements of mixed gases, including IEDs, are presented. This paper discusses the design evaluated on a VHDL platform, implementation on a tinychip, and testing of the final design and chip. Design details, simulations, and experimental results are presented with good sensitivity, stability, and tolerance.

**Session B3L-E: Circuits Tolerant to Radiation Effects**

**Chair:** Ricardo Reis, *Universidade Federal do Rio Grande do Sul, Brazil*

**Time:** Tuesday, August 5, 2014, 13:10 - 14:50

**Location:** Ballroom – 7

**Bulk and FDSOI SRAM Resiliency to Radiation Effects** ..... 655

*Walter Calienes (Universidade Federal do Rio Grande do Sul), Ricardo Reis (Universidade Federal do Rio Grande do Sul), Costin Anghel (Institut Supérieur d'Electronique de Paris), Andrei Vladimirescu (Institut Supérieur d'Electronique de Paris)*

The radiation is an ongoing problem with the contents the memory cells, because the density of transistors is increasing. New technologies must deal with this problem. This paper presents the simulation results of two different memory cell technologies: 32nm Bulk CMOS and 28nm FDSOI against the effect of Single-Event Upset (SEU) caused by the heavy ion impact with different Linear Energy Transfer characteristic (LET).

**Hardware Trojan Detection in Soft Error Tolerant Macro Synchronous Micro Asynchronous (MSMA) Pipeline** ..... 659

*Faiq Khalid Lodhi (National University of Sciences and Technology), Syed Rafay Hasan (Tennessee Technological University), Osman Hasan (National University of Sciences and Technology), Falah Awwad (United Arab Emirates University)*

Glitches due to soft errors have become a major concern in circuits designed in ultra-deep-sub-micron technologies. Most of the soft error mitigation techniques require redundancy and are power hungry. Recently many soft-error tolerant low power null conventional logic (NCL) based asynchronous circuits have been proposed. This paper leverages low-power soft-error-tolerant asynchronous technique in conventional synchronous circuits. The idea is to accommodate asynchronous standards cells in within synchronous pipeline, giving rise to macro synchronous micro asynchronous (MSMA) pipeline. An important application of such design is in detecting the hardware Trojans, as NCL based MSMA pipeline lead to unique timing based signatures.

**Architectural Measures against Radiation Effects in Multicore SoC for Safety Critical Applications** ..... 663

*Oliver Sander (Karlsruher Institut für Technologie), Falco Bapp (Karlsruher Institut für Technologie), Timo Sandmann (Karlsruher Institut für Technologie), Viet Vu Duy (Karlsruher Institut für Technologie), Steffen Bähr (Karlsruher Institut für Technologie), Juergen Becker (Karlsruher Institut für Technologie)*

It is well known that microelectronics sensitivity for radiation effects steadily increases for smaller structure sizes. Additionally lowering the supply voltage decreases safety margins even further. In conclusion modern System-on-Chip (SoC) devices, which typically come as heterogeneous multicores, can be affected by radiation effects not only in space but also in much lower altitudes or even on ground level. This is especially important for safety critical systems, such as automotive or avionics electronics. In order to cope with this issue measures during all phases of development need to be taken into account. This contribution presents and discusses techniques on architectural level, which help to detect faults on the SoC, which might be caused by (but not solely) radiation effects. Additionally these techniques have to be lightweight in terms of resources and costs as safety critical applications typically target cost sensitive markets.

**Analytical Methods to Assess Transient Faults Effects in Logic Circuits** ..... 667

*Lirida Alves de Barros Naviner (Telecom ParisTech)*

This work addresses transient faults in deep sub micron technologies. We focus on reliability assessment approaches highlighting those based on analytical models. The paper includes a comparative study of solutions reported in the literature and discuss their suitability from a reliability improvement perspective.

**Analysis of Fin Height on FinFET SRAM Cell Hardening** ..... 671

*Hector Villacorta (Instituto Nacional de Astrofísica, Óptica y Electrónica and Universitat de les Illes Balears), Jaume Segura (Universitat de les Illes Balears), Sebastià Bota (Universitat de les Illes Balears), Victor Champac (Instituto Nacional de Astrofísica, Óptica y Electrónica)*

Radiation soft reliability is showing a declining with technology scaling. Because of this new techniques are required to add resilience to the chips. In this work, we analyze the impact of increasing the fin height of FinFET transistor as a device-circuit co-design approach to improve FinFET SRAM cell hardening. TCAD simulations of the memory cell are carried-out. Results are presented for a 10nm-SOI Tri-Gate FinFET technology. We show that increasing the fin height of FinFET transistors of the cross-coupled inverters of an SRAM cell may improve hardening to heavy ions with low Linear Energy Transfer (LET) values.

**Session B4P-G: Image Processing and Multimedia Systems III**

**Chair:** Joseph Chang, *Nanyang Technological University, Singapore*

**Time:** Tuesday, August 5, 2014, 14:50 - 15:40

**Location:** Poster Area

**Extraction of Geometrical Corners of Buildings for Infrared Imaging Sequence** ..... 675

*Jinshen Wang (Beijing University of Aeronautics and Astronautics), Fugen Zhou (Beijing University of Aeronautics and Astronautics), Bindang Xue (Beijing University of Aeronautics and Astronautics), Xiangzhi Bai (Beijing University of Aeronautics and Astronautics)*

In this paper, we describe a fully automatic approach for detecting and matching geometrical corner feature correspondences between aerial images with larger scale and view variations. The main premise of the approach is the fact that many man-made environments contain a large number of parallel linear features. We exploit this observation towards efficient detection and estimation of vanishing points. Given the vanishing points within an image, building geometrical corner features are obtained by the intersections of pairs of building outlines corresponding to different vanishing points. The experiments performed on the infrared aerial image sequences evaluate the stability and distinctiveness of the proposed features which are undergone appearance changes due to projective deformation.

**Computer Vision based Real-Time Vehicle Tracking and Classification System** ..... 679

*Raúl Humberto Peña-González (Universidad Politécnica de Victoria), Marco Aurelio Nuño-Maganda (Universidad Politécnica de Victoria)*

Detect, classify and keep track, in real-time, on different kinds of objects or vehicles that are moving on a road is crucial for traffic managements systems, among other research areas. In this paper, a vision based system to detect, track, count and classify moving vehicles, on any kind of road, is shown. The data acquisition system consists of a HD-RGB camera placed on the road, while the information processing is performed by clustering and classification algorithms. The system obtained an efficiency score over the 95 percent in test cases, as well, the correct classification of 85 percent of the test objects. Also, the system achieves 60 fps in image processing with a resolution of 720p.

**A Retina-Inspired Robust On-Focal-Plane Multi-Band Edge-Detection Scheme for CMOS Image Sensors** ..... 683

*Nikola Katic (École Polytechnique Fédérale de Lausanne), Alexandre Schmid (École Polytechnique Fédérale de Lausanne), Yusuf Leblebici (École Polytechnique Fédérale de Lausanne)*

An edge-detection scheme suitable for machine vision and digital motion detection applications is presented. The scheme is inspired by the human visual system (human retina) and modified for a compact and scalable CMOS hardware implementation. In addition, the pixel circuit and the implementation of the scheme on CMOS image sensor focal-plane are proposed and the simulation results are presented. The proposed acquisition technique and the corresponding CMOS circuit can easily be adjusted to various imaging applications and scaled towards new CMOS technology nodes and high resolution image sensors.

**Session B4P-H: Digital Signal Processing II**

**Chair:** Joseph Chang, *Nanyang Technological University, Singapore*

**Time:** Tuesday, August 5, 2014, 14:50 - 15:40

**Location:** Poster Area

**Analysis of l2-Sensitivity for Two-Dimensional State-Space Digital Filters by Taking into Account 0 and  $\pm 1$  Elements** ..... 687

*Yoichi Hinamoto (Kagawa National College of Technology), Akimitsu Doi (Hiroshima Institute of Technology)*

Analysis of l2-sensitivity for two-dimensional (2-D) state-space digital filters is performed more precisely by taking into account 0 and  $\pm 1$  elements. First, the improved version of an l2-sensitivity measure is developed for the Roesser local state-space model. Next, that of an l2-sensitivity measure is explored for the Fornasini-Marchesini second local state-space model. Finally, numerical examples are presented to evaluate the improved l2-sensitivity measures for the considered two local state-space models by means of the proposed methods.

**Binormalized Data-Reusing Filtered-Reference Algorithm for Impulsive Active Noise Control** ..... 691

*Muhammad Tahir Akhtar (University of Electro-Communications)*

The filtered-x least mean square (FxLMS) algorithm for active noise control (ANC) systems is based on the second order moment of the error signal. In this paper we consider ANC for impulsive noise having peaky distribution with heavy tail. Such impulsive noise can be modeled using non-Gaussian stable process for which the second order moments do not exist, and hence, the FxLMS algorithm becomes unstable. Recently, we have proposed variants of the FxLMS algorithm where an improved performance has been realized by thresholding the input data or by efficiently normalizing the step-size. In this paper, we propose a modified binormalized data-reusing (BNDR) algorithm for impulsive ANC. The proposed algorithm is derived by minimizing a modified cost function, and is based on reusing the past and present samples of data. The computer simulations are carried out to demonstrate the effectiveness of the proposed algorithm. It is shown that an improved performance has been realized with a reasonable increase in computational complexity.

**Oscillator based Complex Adaptive Notch Filters** ..... 695

*Shotaro Nishimura (Shimane University), Aloys Mvuma (University of Dodoma),*

*Takao Hinamoto (Hiroshima University)*

In this paper, a new complex adaptive notch filters based on oscillator based algorithm has been proposed. The approach presented for second-order real coefficient IIR filters has been applied to derive a coefficient-update algorithm for a first-order complex adaptive notch filter. Convergence characteristics of the proposed algorithm have been analyzed. Unbiased frequency estimation of a complex sinusoid has been achieved by thinning the notch bandwidth. Computer simulations show the effectiveness of the proposed algorithm.

**Applications of Corrector Filters to Improve Magnitude Response of Comb Decimation Filter** ..... 699

*J.R. Garcia Baez (Instituto Nacional de Astrofísica, Óptica y Electrónica),*

*G. Jovanovic Dolecek (Instituto Nacional de Astrofísica, Óptica y Electrónica)*

This paper presents the applications of simple multiplierless filters to decrease the passband droop and to increase the alias rejection in the folding bands of comb filters. The comparisons with some methods proposed in the literature, are also included to show the benefit of the proposed approach. It is also shown that the method is convenient for the traditional non-recursive comb structure with the decimation factor which is the power of two. In that way the magnitude characteristic of the structure is significantly improved while keeping the power efficiency of the original structure, by placing three simple filters in last two stages.



**Estimation of Gait Stability based on Accelerometer Signals** ..... 703

*Hector Moncada-Gonzalez (Universidad Autónoma de San Luis Potosí), Ruth M. Aguilar-Ponce (Universidad Autónoma de San Luis Potosí), J. Luis TecpanecatI-Xihuitl (Universidad Autónoma de San Luis Potosí)*

an estimation of gait stability based on accelerometer signal is presented. The walking process of a human body is a complex task that involves the muscular, joint and nervous systems. The gait cycle is divided into swing and stance phases. Gait stability is defined as repetition of the gait cycle with minimum variability. In order to assess the gait stability a series of parameters are estimated, such parameters include, duration of the gait cycle, length of the left and right step, average speed of the gait and number of samples per cycle. The first step toward establish gait stability is estimated the beginning and ending of a cycle. This process is achieved by a series of filter that isolated 2Hz component that is produced by heel strike. Once the cycles have been localized, the rest of the parameters are estimated. The algorithm was tested on a set of 40 healthy persons from ages 20 to 59. The results show that the stability decreases with age, as expected, since our neuromotor system deteriorates with age

**An RNS based FIR Filter Design using Shift and Add Approach** ..... 707

*Srinivasa Reddy Kotha (Birla Institute of Technology and Science), Sumit Bajaj (Birla Institute of Technology and Science), Sahoo Subhendu Kumar (Birla Institute of Technology and Science)*

In this work, an efficient finite impulse response (FIR) filter using Residue Number System (RNS) is proposed. The moduli set used in this work is  $\{2^k - 1, 2^k, 2^{k+1} - 1\}$ . The proposed filter architecture is compared with an earlier proposed version of reconfigurable RNS FIR filter. The filters are synthesized using Cadence RTL compiler in UMC 90nm technology. The performance of the filters are compared in terms of Area (A), Power (P), and Delay (T). The results show that the proposed architecture offers significant improvement in terms of area, delay and area-delay product(AT). Proposed approach is also verified functionally using Altera DSP Builder.

**Session B4P-J: Communication and Wireless Systems**

**Chair:** Faramarz Bahmani, *Broadcom Co.*

**Time:** Tuesday, August 5, 2014, 14:50 - 15:40

**Location:** Poster Area

**An Inductorless Continuous Time Equalizer with Programmability for Gigabit Links** ..... 713

*Sushrant Monga (Cadence Design Systems), Shouri Chatterjee (Indian Institute of Technology, Delhi)*

A continuous-time inductorless non-linear equalizer is presented which can be programmed for different channels for very high speeds. The design can effectively equalize the channel by feeding back the post-cursor voltage at multi-Gigabit frequency with most-optimized area and power consumption. The circuit can be adapted to a given link environment (noisy channel and the termination) by controlling the amount of feedback and thereby defining the high-frequency and low-frequency response. The architecture is scalable to higher speeds with technology. Measurement results depict the successful equalization of channels having an attenuation of upto -19dB at 10-GHz. The circuit is fabricated in 0.13 um CMOS technology and consumes a current of 39-mA (max.) at (Vdd = 1.32V).

**A Digital Predistortion Technique based on a NARX Network to Linearize GaN Class F Power Amplifiers** ..... 717

*L.M. Aguilar-Lobo (Centro de Investigación y de Estudios Avanzados del Instituto Politécnico Nacional),*

*A. Garcia-Osorio (Centro de Investigación y de Estudios Avanzados del Instituto Politécnico Nacional),*

*J.R. Loo-Yau (Centro de Investigación y de Estudios Avanzados del Instituto Politécnico Nacional),*

*S. Ortega-Cisneros (Centro de Investigación y de Estudios Avanzados del Instituto Politécnico Nacional),*

*P. Moreno (Centro de Investigación y de Estudios Avanzados del Instituto Politécnico Nacional), J.E. Rayas-*

*Sanchez (Instituto Tecnológico y de Estudios Superiores de Occidente - The Jesuit University of Guadalajara),*

*J.A. Reynoso-Hernández (Centro de Investigación y de Estudios Avanzados del Instituto Politécnico Nacional)*

This work presents a novel Digital Predistortion (DPD) scheme based on a NARX network, suitable for linearizing power amplifiers (PAs). The NARX network is a Recurrent Neural Network (RNN) with embedded memory that allows efficient modeling of nonlinear systems. Its neural architecture is very effective to model long term dependencies, such as the typical memory effects of PAs. To demonstrate the feasibility of the NARX network as a DPD system, a GaN class F PA with two LTE signals with 5 MHz of bandwidth is used. Experimental results show a distortion correction better than 10 dB.



**Optoelectronic Multiplexing of Microwave Sub-Carriers for High-Speed Wireless Transmissions** ..... 721

*Celso Gutiérrez-Martínez (Instituto Nacional de Astrofísica, Óptica y Electrónica and CRECTEALC), Adolfo Morales-Díaz (CRECTEALC), Jacobo Meza-Pérez (Instituto Nacional de Astrofísica, Óptica y Electrónica and CRECTEALC), Alfredo Torres-Fórtiz (Instituto Nacional de Astrofísica, Óptica y Electrónica and CRECTEALC), Joel Santos-Aguilar (Centro de Investigación y Educación Superior de Ensenada)*

In the rf domain, multiplexed transmission of microwave subcarriers is implemented by associating microwave oscillators, mixers and rf filters in order to accommodate and isolate the modulated subcarriers before being transmitted by different media as metallic and optical cables, earth atmosphere or free space. In an alternative approach, an optoelectronic multiplexing scheme for grouping high-data rate modulated microwave subcarriers is reported in this paper. This scheme avoids the use of microwave filters and the multiplexing scheme is based on the sharp band-pass microwave filtering response of a multimode laser associated to a length of dispersive standard single mode optical fiber. The multiplexing of 2, 100mbps data-modulated microwave subcarriers in the band between 5 to 9 ghz (the ultra wide-band (uwb) radio over fiber links) is demonstrated in his work.

**A Wideband Class E PA with more than 40% PAE and over 800 MHz Bandwidth** ..... 725

*Praveen Gunturi (University of Maine), David E. Kotecki (University of Maine)*

A Power Amplifier (PA) for wireless applications operating between 2.6 GHz and 3.4 GHz with power added efficiency (PAE) of more than 40% is presented in the paper. By varying the width of the PA transistor, the performance of the PA in terms of PAE and stability is studied for 800 MHz bandwidth. The PAE is more than 40% for the bandwidth of 800 MHz. The input matching circuit is implemented using on-chip transmission lines and the input reflection coefficient is less than -8dB over the bandwidth. The output power and PAE are 15.5dBm and 52% at 2.7 GHz. The power amplifier is implemented in 180nm CMOS technology and the total area is approximately equal to 1mm<sup>2</sup>. It includes electrostatic discharge (ESD) protection.

**AOA Target Tracking with New IMM PF Algorithm** ..... 729

*Dah-Chung Chang (National Central University), Meng-Wei Fang (National Central University)*

The state estimation technique based on the Kalman filter (KF) is widely used in many communication applications. The KF is only optimal for linear modeling with independent and identically distributed (i.i.d.) random variables and Gaussian noises. In some complicated problems, the system model is not unique and the measurement equation is nonlinear. The particle filter (PF) along with interacting multiple models (IMM) becomes an attractive solution. In this paper, a new particle resampling method is proposed for the PF to alleviate the degeneracy effect of particle propagation. The new IMM PF algorithm is developed for an angle-of-arrival (AOA) tracking problem with bearings-only measurements. Simulation results show that the IMM PF algorithm outperforms the IMM extended KF algorithm and achieves a root mean square tracking performance which is quite close to the posterior Cramer-Rao lower bound (CRLB).

**Temperature and Supply Voltage Insensitive OOK Transmitter for UWB Outdoor Communications** ..... 733

*Praveen Gunturi (University of Maine), David E. Kotecki (University of Maine)*

Most of the literature on Ultra Wide Band (UWB) transmitters is focused on indoor communications. This paper presents the architecture of an Impulse Radio Ultra Wide Band (IR-UWB) transmitter for outdoor communications which complies with the FCC spectral limits. The transmitter consists of a pulse generator (PG) and a driver circuit and has an operating frequency between 3.1 GHz and 6.4 GHz. The pulse output amplitude is 700mV peak-to-peak into a 50 ohm resistive load. The maximum data rate that can be achieved by the transmitter is 250Mbps at an overall power efficiency of 6.3%. The transmitter is compensated for voltage and temperature (VT) variations. The output pulse energy changes by less than 24% as the temperature varies from -55 C to 100 C, and by less than 5% as the supply voltage varies between 2.3 and 3.6V. The design is implemented in 180nm CMOS process and the simulation results with extracted R, L, C parasitics are presented.

**Session B4P-K: Neural Networks**

**Chair:** Kamran Entesari, *Texas A&M University*

**Time:** Tuesday, August 5, 2014, 14:50 - 15:40

**Location:** Poster Area

**Design Robustness Analysis of Digital Spiking Neural Circuits** ..... 737

*Ahmad Bashairah (Texas A&M University), Peng Li (Texas A&M University)*

A method to evaluate the impact of process and environmental variations on the overall performance of biologically inspired spiking neural networks, implemented predominantly in digital CMOS. In this method, transistor-level and behavioral level analysis are carried out. Then, the results of the transistor-level simulation are projected on the application layer to determine the effect of variability on the performance of the system. The experimental results have demonstrated the robustness of the networks with respect to the targeted variation effects.

**An Integrated Active-Pixel-Sensor and Memristive Platform for Neural-Inspired Image Learning and Recognition** ..... 741

*Wenbo Chen (University of Toledo), Wenchao Lu (University of Toledo), Yibo Li (University of Toledo), Kaitlyn Alexander (University of Toledo), Rashmi Jha (University of Toledo)*

In this paper, we report our studies on integrated active pixel sensor (APS) array and memristor crossbar neural network to perform image learning and recognition in an unsupervised fashion. APS modules encode light intensity/gray value of grayscale images into APS sensing current feeding into  $N_2 \times M$  crossbar array. The memristor is used as a synapse and can be trained through an adaption of spike timing dependent plasticity (STDP). After training, different images are stored into different post-synaptic neuron dendrites. In the image recognition stage, a simple pulse counter circuit was used to check the matched image. System level simulations show that the network can store grayscale image correctly and perform image recognition in a simple and efficient way.

**Session B4P-L: VCOs and Frequency Synthesizers**

**Chair:** Kamran Entesari, *Texas A&M University*

**Time:** Tuesday, August 5, 2014, 14:50 - 15:40

**Location:** Poster Area

**A Novel Approximated Solution for the Van der Pol Oscillator. Application to Pulsed Oscillations Modeling in Switched Cross-Coupled MOS Oscillators** ..... 745

*Clément Jany (CEA-Leti), Alexandre Siligaris (CEA-Leti), Pierre Vincent (CEA-Leti), Philippe Ferrari (Université de Grenoble-Alpes)*

The operation of a periodically switched cross-coupled oscillator is considered in this work. First, it is shown that this architecture corresponds to a Van der Pol oscillator. Based on that, a novel analytical solution is proposed for the Van der Pol equation taking into account the time-dependent amplitude and frequency variation at the starting of oscillation. In addition, an original specific model for the pulsed oscillations is presented. Comparison with numerical simulations of the Van der Pol equation shows very good accuracy. Finally, it is shown that synchronization of the oscillations pulses on the input signal can be obtained under specific conditions.

**A 3.45-4.22 GHz PLL Frequency Synthesizer with Constant Loop Bandwidth for WLAN Applications** ..... 749

*Xiaolong Liu (Tsinghua University), Lei Zhang (Tsinghua University), Li Zhang (Tsinghua University), Yan Wang (Tsinghua University), Zhiping Yu (Tsinghua University)*

A fully integrated phase-locked loop (PLL) frequency synthesizer for WLAN applications is designed in a 0.13- $\mu\text{m}$  CMOS process. In order to make the loop bandwidth constant across the whole operating frequency range, a switched varactor array based LC-VCO is used to achieve a low KVCO variation, the charge pump current is programmed proportional to division ratio, and the variation on LPF resistance is cancelled by a matched reference resistance in a band-gap. By combination of these techniques, a constant loop bandwidth is achieved over the entire output frequency range. The proposed PLL attains less than  $\pm 4\%$  variation in loop bandwidth over an operating frequency range from 3.45 to 4.22 GHz. The chip consumes 21.1 mW of power while occupying an area of 0.88 mm<sup>2</sup>.

**Session B5L-A: Delta-Sigma Techniques II**

**Chair:** R. Jake Baker, *University of Nevada, Las Vegas*

**Time:** Tuesday, August 5, 2014, 15:40 - 17:20

**Location:** Mockingbird

**LMS-Based Digital Background Linearization Technique for VCO-Based Delta-Sigma ADC** ..... 753

*Fu-Chien Huang (National Taiwan University), Shou-Chen Hsu (National Taiwan University), Yi-Lin Tsai (National Taiwan University), Yung-Yu Lin (MediaTek Inc.), Tsung-Hsien Lin (National Taiwan University)*

This paper presents a digital background linearization technique for VCO-based delta-sigma ADC. The nonlinearity of the VCO in the main ADC is mitigated with the aid of the reference OP-based delta-sigma ADC and the digital least-mean square (LMS) correction algorithm. The reference ADC provides sufficient linearity performance as the calibration reference to form an inverse transfer function of the nonlinear voltage-to-frequency characteristic while the LMS-based calibration scheme shortens the correction time to reduce energy consumption. The simulated SFDR/SNDR of 70.2 dB/62.7 dB over a bandwidth of 10 MHz is achieved, which is 23.3 dB/16.6 dB better than the SFDR/SNDR of uncalibrated ADC. A prototype first-order VCO-based ADC is designed in 90-nm CMOS process and dissipates 2.89 mW from a supply voltage of 1.2 V.

**DLL-Based Pulse-Width Modulation Digital-to-Analog Converter for Continuous-Time Sigma Delta Modulators** ..... 757

Zong-Yi Chen (National Chiao Tung University), Chung-Chih Hung (National Chiao Tung University)

In this paper, the DLL-based pulse-width modulation (PWM) digital-to-analog converter (DAC) is proposed to convert the output of multi-bit quantizer to a single-bit pulse-width modulated signal in the modified continuous-time sigma-delta modulators (CT-SDMs) with improved signal transfer function (STF). The DLL-based PWM DAC is more robust to clock jitter and excess loop delay (ELD) effects than conventional multi-bit DAC and other PWM DAC with similar speed and power requirements of the integrators in CT-SDMs. Furthermore, the proposed PWM DAC is based on inherently linear single-bit DAC, so the dynamic-element matching (DEM) techniques, which increase the circuit complexity and power consumption to compensate the mismatch of unit elements in the multi-bit DAC, can be removed in CT-SDMs

**A 3.86mW 106.4dB SNDR Delta-Sigma Modulator based on Switched-Opamp for Audio Codec** ..... 761

Zhongyi Huang (Zhejiang University), Menglian Zhao (Zhejiang University), Xiaolin Yang (Zhejiang University), Liyu Lin (Zhejiang University), Xiaobo Wu (Zhejiang University)

A low-power high-resolution Delta-Sigma modulator for audio codec, designed in Global-Foundries BCD 0.18 $\mu$ m 1P4M CMOS process, is presented. The modulator employs a fourth-order single-loop feedforward topology with a 3bit-quantizer. A novel structure of Switched-Opamp (SO) utilizing current-starvation and Slew-Rate (SR) boosting is adopted to meet the requirements of high performance and fast-settling time. The opamp-shared technique and two-step summation are used to reduce power dissipation further. Meanwhile, to improve the resolution, chopper-stabilisation (CHS) and pseudo data-weighted-averaging (PDWA) circuits are employed in this paper. The proposed modulator achieves 3.86mW power consumption and 106.4dB Signal-to-Noise Distortion Ratio (SNDR).

**Blocker Tolerant Wideband Continuous Time Sigma-Delta Modulator for Wireless Applications** ..... 765

Hemasundar Mohan Geddada (Texas A&M University), Chang-Joon Park (Texas A&M University), José Silva-Martinez (Texas A&M University), Aydin İlker Karsilayan (Texas A&M University)

A continuous-time low-pass Delta-sigma (DS) ADC equipped with design techniques to provide robustness against saturation due to blockers is presented. An integrated low pass blocker filter that reduces the most critical adjacent/alternate channel blockers by 7/11 dB, respectively is implemented at the input of the ADC. The blocker filter is power efficient, highly linear and its noise is shaped out of signal band. Measurement results show that the proposed ADC implemented in a 90-nm digital CMOS process achieves 69 dB dynamic range over a 20 MHz bandwidth with a sampling frequency of 500 MHz and 17.1 mW of power consumption. The alternate channel blocker tolerance at the most critical frequency is "12.5 dBFS in the presence of a -12 dBFS in-band signal while the conventional modulator becomes unstable for "23.5 dBFS blocker power. The proposed integrated blocker filter is non-invasive, low power (1.4mW) and does not degrade the stability of the DS loop.

**Session B5L-B: Switching and Linear Power Conversion Techniques**

**Chair:** Ayman Fayed, *Iowa State University*

**Co-Chair:** Hoi Lee, *University of Texas, Dallas*

**Time:** Tuesday, August 5, 2014, 15:40 - 17:20

**Location:** Ballroom – 5

**A 140W 97%-Efficiency 4MHz Two-Phase Buck Converter with Quasi-Square-Wave ZVS Scheme** ..... 769

Lin Cong (University of Texas at Dallas), Jing Xue (University of Texas at Dallas), Hoi Lee (University of Texas at Dallas)

This paper presents a high-frequency high-efficiency two-phase buck converter with quasi-square-wave (QSW) ZVS scheme for high-voltage automotive applications. A set of auxiliary inductor and capacitor is shared between two-phase sub-converters to realize ZVS for all power FETs and minimize converter switching power loss under high-voltage and high-frequency conditions. The proposed two-phase structure reduces the required current ripple in the auxiliary inductor, thereby reducing the core loss at high switching frequency. The sizes of the main inductor and the output capacitor are also reduced due to the current ripple cancellation in the two-phase converter. With enhancement-mode GaN FETs, simulation results show that the proposed two-phase QSW-ZVS converter can operate at 4 MHz and achieve peak power efficiency of 97% at a full power of 140 W.

**Novel Buck Converter Architectures for Large Step-Down Conversion Ratio** ..... 773

*Mohammed Fouly Mostafa (Cairo University), Mohamed M. Aboudina (Cairo University),  
Faisal A. Hussien (Cairo University)*

Ultra low duty-cycle clock signal is required in buck converters with large step-down voltage conversion ratio. Given the maximum achievable rise and fall time as well as the minimum ON time of the transistors, this sets a maximum limit on the operating frequency. Different buck converter architectures are proposed to achieve the same voltage conversion ratio with a larger duty cycle. Therefore, the constraints on the minimum transistor ON time and the maximum operating frequency are relaxed. The proposed converters are completely independent on mutual coupling and, as a consequence, they do not suffer from any leakage inductance and do not need any protection or clipping circuits. The analysis produces the relation between the duty-cycle and the voltage gain and shows how much the enhancements are.

**Switch-Less Adaptive Feed-Forward Supply Noise Cancellation Technique for Capacitor-Less LDR** ..... 777

*Fan Yang (Hong Kong University of Science and Technology), Philip K.T. Mok (Hong Kong  
University of Science and Technology)*

An adaptive feed-forward power supply noise cancellation technique for low-dropout regulator (LDR) which requires no switches is proposed in this paper. By utilizing replica, transconductances ( $g_m$ ,  $g_{ds}$ ) of the large pass transistor are linearly reproduced to construct a load-current-dependent ratioed feed-forward path from supply to gate of pass transistor. The power supply rejection (PSR) capability is enhanced by adaptively feeding compensation charging current to gate parasitic capacitor of the pass transistor, which is effective in a wide load range. The idea of the PSR enhancement technique is implemented in an output capacitor-less LDR in a standard 65-nm CMOS process. The total on-chip capacitance for compensation and low-pass filtering is 40pF. The output is 1.0V and delivers a maximum current of 50mA at 200mV drop-out. Simulations verify that the PSR is further enhanced in mid-frequency range (~100kHz~10MHz) compared with conventional techniques, without feed-forward ratio selection via switches, and it generates ignorable effects on stability and 200-ns full load transient response.

**Ripple-Port Integrated PFC Rectifier with Fast Dynamic Response** ..... 781

*Bo Tian (Texas A&M University), Souhib Harb (Texas A&M University), Robert S. Balog (Texas A&M University)*

A new control strategy for Power Factor Correction (PFC) rectifier which has double-line frequency ripple decoupling capability is presented and experimentally implemented. Based on the commonly used Boost PFC regulator, an integrated non-cascading ripple-port on the DC-side completely filters the double-line frequency ripple. Hence, the output capacitance required is significantly reduced and high reliability film capacitors can be used to replace the bulky, low reliability electrolytic ones. The proposed control scheme for the ripple-port guarantees the ripple cancellation under various load conditions. Furthermore, comparing to conventional PFC rectifier, the proposed rectifier has improved transient response to load dynamics.

## **Session B5L-C: Digital Signal Processing I**

**Chair:** Ricardo Reis, *Universidade Federal do Rio Grande do Sul, Brazil*

**Co-Chair:** Majid Ahmadi, *U of Windsor*

**Time:** Tuesday, August 5, 2014, 15:40 - 17:20

**Location:** North & South 40

**Joint Optimization of High-Order Error Feedback and Realization for Roundoff Noise**

**Minimization in State-Estimate Feedback Controllers** ..... 785

*Takao Hinamoto (Hiroshima Institute of Technology), Akimitsu Doi (Hiroshima Institute of Technology),  
Wu-Sheng Lu (University of Victoria)*

Joint optimization of high-order error-feedback and state-space realization to minimize roundoff noise at the output of a closed-loop system with a state-estimate feedback controller subject to  $l_2$ -scaling constraints is investigated. The problem is converted into an unconstrained optimization problem by using linear-algebraic techniques. The unconstrained optimization problem at hand is then solved iteratively by employing an efficient quasi-Newton algorithm with closed-form formulas for key gradient evaluation. Analytical details are given as to how the proposed technique can be applied to the case where high-order error-feedback matrices are diagonal. A numerical example is presented to illustrate the utility of the proposed technique.

**Nonlinear Active Noise Control using Diagonal-Channel LMS and RLS Bilinear Filters** ..... 789

*Li Tan (Purdue University North Central), Jean Jiang (Purdue University North Central)*

This paper proposes an adaptive bilinear filter with a diagonal-channel structure for nonlinear active noise control. Based on the diagonal-channel structure, the diagonal-channel bilinear filtered-X least mean square (DBFXLMS) and recursive least square (DBFXRLS) algorithms are derived. In order to reduce the computational load for the DBFXRLS algorithm, the DBFXRLS algorithm with a sequential channel update (DBFXRLS-SEQ) is proposed. Computational complexity for each algorithm is examined. Computer simulations demonstrate the control performance improvement using the proposed algorithms.



**Design of Hardware Efficient Modulated Filter Bank for EEG Signals Feature Extraction** ..... 793

*Jiajia Chen (Singapore University of Technology and Design), Weiao Ding (Singapore University of Technology and Design), Juan Zhou (Duke-NUS Graduate Medical School)*

We propose a new efficient design algorithm to synthesize low complexity FIR filters, which has been applied to EEG signals feature extraction filter bank. A prudently defined bit-level frequency response sensitivity function is designed as a measure for the quantization decision making. Common subexpressions sharing is maximized with instant checking and updating of common subexpressions statistics. By this new algorithm, the filter coefficients are quantized into optimal patterns. The effectiveness of the proposed algorithm is demonstrated using two design examples where the solution saves about 82.6% and 48.5% of hardware complexity over the baseline implementation and other competing methods.

**Zero-Rotation-Based Nonrecursive Comb Structure** ..... 797

*Erika Y. Teran Bahena (Instituto Nacional de Astrofísica, Óptica y Electrónica), Gordana Jovanovic Dolecek (Instituto Nacional de Astrofísica, Óptica y Electrónica)*

This paper presents a comb-based nonrecursive decimation structure with improved magnitude characteristics, where the decimation factor  $M$  is a power of two. A rotated cosine filter is introduced to increase the attenuation in the folding bands. Additionally, the passband droop is decreased by using a simple multiplierless compensation filter which works at low rate. The multiplierless rotated term is also introduced. The method is illustrated with examples and the comparisons with other methods are provided.

**A Scheme for Copy-Move Forgery Detection in Digital Images based on 2D-DWT** ..... 801

*S.A. Fattah (Bangladesh University of Engineering and Technology), M.M.I. Ullah (Bangladesh University of Engineering and Technology), M. Ahmed (Bangladesh University of Engineering and Technology), I. Ahmmed (Prime Silicon Technology Inc.), C. Shahnaz (Bangladesh University of Engineering and Technology)*

In this paper, a copy-move image forgery detection scheme is developed based on a block matching algorithm. Instead of considering spatial blocks, 2D-DWT is performed on the forged image and then DWT domain blocks are considered, where only approximate DWT coefficients are utilized. In order to reduce the computational burden, unlike conventional approaches, instead of performing block matching operation among all blocks, some candidate blocks are first selected from the non-overlapping blocks based on a similarity measure. In the next stage, all overlapping blocks are compared with the candidate blocks. A similarity criterion is introduced to finally detect the forged blocks. Extensive simulation is carried out on several forged images and it is found that proposed algorithm can efficiently detect copy-move forgery.

## **Session B5L-D: Image Processing and Multimedia Systems II**

**Chair:** Moataz Abdelwahab, *Alexandria Academy*

**Time:** Tuesday, August 5, 2014, 15:40 - 17:20

**Location:** Ballroom – 6

**Human Action Recognition based on Two-View Optical Flow in the Transformed Domain** ..... 805

*Mohamed A. Abdelwahab (Egypt-Japan University of Science and Technology), Moataz M. Abdelwahab (Egypt-Japan University of Science and Technology)*

In this paper a human action recognition algorithm based on two-view of optical flow in multiple layers per camera employing the transform domain and 2DPCA is presented. This method explores more distinctive features between actions. It is not sensitive to translation, alignment and noise. In addition the use of 2DPCA maintains the spatial relation between pixels and increases the recognition accuracy. Experimental results performed on the Weizmann action and the INIRIA IXMAS datasets confirm these excellent properties compared to recent reported methods.

**Joint Noise Distribution Parameter Estimation and LDPC Decoding using Variational Bayes** ..... 809

*Y. Mohammad Taheri (Concordia University), M. Omair Ahmad (Concordia University), M.N.S. Swamy (Concordia University)*

In this work, we investigate the problem of estimating time-varying noise distribution parameter on a factor graph. A new message passing scheme is proposed by incorporating the variational Bayes (VB) into the belief propagation algorithm for estimating of time-varying noise distribution parameter in a low-density parity-check decoder. The scheme can also be used for the estimation of correlation noise model parameter in distributed video coding. A Bayesian estimator is used to estimate this parameter by obtaining its posterior distribution given the channel output. The VB algorithm is employed to approximate the complex form of the posterior distribution with a simple distribution. Finally, this distribution is used to derive a closed form expression for the messages on the augmented factor graph for online parameter estimation and decoding process at the same time.



**Building a Surface Atlas of Hippocampal Subfields from MRI Scans using FreeSurfer, FIRST and SPHARM** . 813

*Shan Cong (Indiana University-Purdue University Indianapolis), Maher Rizkalla (Indiana University-Purdue University Indianapolis), Eliza Y. Du (Indiana University-Purdue University Indianapolis), John West (Indiana University-Purdue University Indianapolis), Shannon Risacher (Indiana University-Purdue University Indianapolis), Andrew Saykin (Indiana University-Purdue University Indianapolis), Li Shen (Indiana University-Purdue University Indianapolis)*

A novel method for detailed surface based morphology study is proposed, and a pipeline is set up based on this idea, which provides a way to visually demonstrate hippocampal subfield distributions on the hippocampal surface. Advanced tools FreeSurfer and FSL are employed for subcortical segmentation, SPHARM is employed for 3D object modeling and reconstruction. This multi-tools based pipeline provides smooth and reliable results, can be applied on preclinical Alzheimer's disease and Mild Cognitive Impairment in the further studies.

**A Transform Domain Modular Approach for Facial Recognition using Different Representations and Windowing Techniques** ..... 817

*Ramy C.G. Chehata (University of Central Florida), Wasfy B. Mikhael (University of Central Florida), George Atia (University of Central Florida)*

A face recognition algorithm based on a newly developed Transform Domain Modular (TDM) approach is proposed. In this approach, the spatial faces are divided into smaller sub-images, which are processed using non-overlapping and overlapping windows. Each image is subsequently transformed using a compressing transform such as the two dimensional discrete cosine transform. This produces the TDM-2D and the TDM-Dia based on two-dimensional and diagonal representations of the data, respectively. The performance of this approach for facial image recognition is compared with the state of the art successful techniques. The test results, for noise free and noisy images, yield higher than 97.5% recognition accuracy. The improved recognition accuracy is achieved while retaining comparable or better computation complexity and storage savings.

**Session B5L-E: Printed Electronics and Electronics for Space**

**Chair:** Joseph Chang, *Nanyang Technological University, Singapore*

**Co-Chair:** Ge Tong, *Nanyang Technological University, Singapore*

**Time:** Tuesday, August 5, 2014, 15:40 - 17:20

**Location:** Ballroom – 7

**Radiation-Hardened Library Cell Template and its Total Ionizing Dose (TID) Delay Characterization in 65nm CMOS Process** ..... 821

*Joseph S. Chang (Nanyang Technological University), Kwen-Siong Chong (Nanyang Technological University), Wei Shu (Nanyang Technological University), Tong Lin (Nanyang Technological University), Jize Jiang (Nanyang Technological University), Ne Kyaw Zwa Lwin (Nanyang Technological University), Yang Kang (Nanyang Technological University)*

We propose a radiation-hardened library cell template based on a 65nm CMOS process for the development of a radiation-hardened-by-design (RHBD) cell library for space and satellite (S&S) applications. The proposed library cell template adheres to the fixed-height variable-width standard cell approach, and is designed to inherently embody a number of RHBD techniques at the device- and layout-level to mitigate the radiation effects. We further design a test circuitry embodying several library cells based on the RHBD template for total ionizing dose (TID) irradiation testing. With the test circuitry, we show that our RHBD library cells experience insignificant delay effects at TID dosage up to 500Krad, VDD = 0.9V-1.4V. The irradiating tests provide concrete experimental data that verify the robustness of our proposed RHBD cell template and the ensuing design methodologies (including library development) for S&S electronics.

**Fully-Additive Printed Electronics on Flexible Substrates: A Fully-Additive RFID Tag** ..... 825

*Tong Ge (Nanyang Technological University), Joseph S. Chang (Nanyang Technological University), Tong Lin (Nanyang Technological University), Zhang Lei (Nanyang Technological University), Lim Geok Soon (Nanyang Technological University)*

Printed electronics, particularly that printed on flexible substrates, is an emerging technology with gargantuan market potential " the current market is \$16.04 billion and is projected to grow to \$76.79 billion in a decade. Although the Printed Radio Frequency Identification (RFID) is projected to be ubiquitous, there is no fully-functional Printed RFID is yet available at this juncture. In this paper, we describe the challenges of realizing a printed RFID and report our efforts for it realization based our Fully-Additive printing process, including key functional blocks thereof that have been printed, measured and verified. This is the first demonstration of a Fully-Additive printed RFID.

**Flexible, Large-Area, and Distributed Organic Electronics Closely Contacted with Skin for Healthcare Applications** ..... 829

*Makoto Takamiya (University of Tokyo and JST/ERATO), Hiroshi Fuketa (University of Tokyo and JST/ERATO), Koichi Ishida (University of Tokyo), Tomoyuki Yokota (University of Tokyo and JST/ERATO), Tsuyoshi Sekitani (University of Tokyo and JST/ERATO), Takao Someya (University of Tokyo and JST/ERATO), Takayasu Sakurai (University of Tokyo and JST/ERATO)*

Flexible, large-area, and distributed sensor and/or actuator array closely contacted with the human skin are human-friendly and sophisticated tools for biomedical and healthcare applications. In this paper, new applications and design solutions in organic electronics are shown. In an insole pedometer with piezoelectric energy harvesters, an all-pMOS negative voltage generator for a pseudo-CMOS inverter is shown. In a surface electromyogram measurement sheet for the prosthetic hand control, a post-fabrication select-and-connect method to reduce the transistor mismatch is shown. In a flexible wet sensor sheet to detect the urination in diapers, ESD protection with organic schottky diodes is shown.

**Asynchronous Baseband Processor Design for Cooperative MIMO Satellite Communication** ..... 833

*Ehsan Rohani (Texas A&M University), Jingwei Xu (Texas A&M University), Tiben Che (Texas A&M University), Mehnaz Rahman (Texas A&M University), Gwan Choi (Texas A&M University), Mi Lu (Texas A&M University)*

The challenges in satellite communication (SatCom) include but not limited to the customary complications of telecommunication such as channel condition and signal to noise ratio (SNR). SatCom system is also prone transient and permanent radiations hazards. Hence, in spite of the harsh environmental factors, (weather phenomena, solar events, etc) a SatCom system must maintain reliable and predictable communication functions with limited source of power. This paper presents a SatCom system design for achieving both low-power and high fidelity communication. The design uses cooperative multiple input multiple output (MIMO) for spectral efficiency and diversity, low-density parity-check (LDPC) decoding for near Shannon-limit gain, and dynamic voltage and frequency scaling (DVFS)-assisted asynchronous circuit designs to achieve low-power and fault tolerance. The MIMO system permits uninterrupted service in the event of temporary/permanent link or unit failures. The results shows the perfect tolerably against the radiation that apply upto 25 fQ on critical path.

**6-GHz All-Pass-Filter-Based Delay-and-Sum Beamformer in 130nm CMOS** ..... 837

*Peyman Ahmadi (University of Calgary), M. Hossein Taghavi (University of Calgary), Leonid Belostotski (University of Calgary), Arjuna Madanayake (University of Akron)*

A broadband RF delay-and-sum (DAS) beamformer, which employs wide-band CMOS all-pass filters for achieving the desired time delays, is discussed in this work. The use of all-pass filters eliminates the need of I/Q mixers and transmission line-based delay stages used in the previously reported DAS beamformers. The proposed all-pass filter can achieve approximately linear-phase delay across GHz-range of frequencies, which is amendable for wide-band beamforming. The delay-and-sum section of the beamformer was designed and simulated for an array of 4 antennas, with the desired signal direction of arrival of 11deg from broadside direction. The performance of the wide-band DAS beamformer is obtained with simulations in IBM 130-nm CMOS technology. Moreover, experimental results for the main building block of the circuit, the voltage-mode all-pass filter with the nominal 33ps delay, are given to strengthen the feasibility of physical implementation of such a beamformer.

**Wednesday, August 6, 2014**

**Session C1P-G: Data Converters**

**Chair:** R. Jake Baker, *University of Nevada, Las Vegas*

**Time:** Wednesday, August 6, 2014, 9:20 - 10:10

**Location:** Poster Area

**12 Bits, 40MS/s, Low Power Pipelined SAR ADC** ..... 841

*Vahid Khojasteh Lazarjan (Sharif University of Technology), Khosrow Hajsadeghi (Sharif University of Technology)*

This paper presents a low power SAR ADC utilizing pipelining to increase the resolution up to 12 bits while maintaining a high speed sampling rate. Novel system level modifications and also new comparator architecture are proposed to optimize the power consumption. The ADC is designed and simulated in 0.18um CMOS technology by 1.2v supply voltage consuming 4.5mW power at 40MS/s sampling rate. The results indicates an effective number of bits (ENOB) of 11.04 bit and a challenging FOM of 54.9fj/conversion which verifies the competence of proposed method.

**A Low-Power, CT Sigma-Delta Modulator with a 2b/Cycle SAR Quantizer** ..... 845

*Lishan Lv (University of Electronic Science and Technology of China),*

*Qiang Li (University of Electronic Science and Technology of China)*

In this paper, a low power CTSDM is proposed. The power consumption of the quantizer is decreased by using a 2b/cycle SAR quantizer, which can operate at higher clock rate than conventional 1b/cycle SAR quantizer. And also, the switchback switching method is adopted to reduce the power consumption of quantizer. The transistor-level simulation results show that the CTSDM can obtain peak SNDR of 71.6dB and SFDR of 82.7dB within 5MHz bandwidth. The proposed SAR quantizer consumes power of 782 $\mu$ W.

**Nauta OTA in a Second-Order Continuous-Time Delta-Sigma Modulator** ..... 849

*Astria Nur Irfansyah (University of New South Wales and Institut Teknologi Sepuluh Nopember), Long Pham*

*(University of New South Wales), Andrew Nicholson (University of New South Wales), Torsten Lehmann*

*(University of New South Wales), Julian Jenkins (Perceptia Devices Australia, Pty. Ltd. and University of New*

*South Wales), Tara Hamilton (University of Western Sydney and University of New South Wales)*

This paper discusses and shows the use of Nauta operational transconductance amplifiers as integrator elements in a second-order continuous-time delta-sigma ADC. The structure is studied in order to take advantage of its potentially high bandwidth operation and simple inverter-based structure for wide output voltage range in current and future CMOS process. The second-order continuous-time delta sigma modulator circuit is implemented in CMOS 65nm, with simulation results showing that 63.29-dB SFDR, and an SNDR of 58.11-dB or 9.36 effective number of bits are achieved, with a signal bandwidth of 8 MHz and sampling frequency of 1.024 GHz. Challenges related to implementation issues and their trade-off are discussed.

**A Low-Power 10MHz Bandwidth Continuous-Time  $\Sigma\Delta$  ADC with Gm-C Filter** ..... 853

*Jin-Hua Hong (National University of Kaohsiung), Zong-Yi Chen (National University of Kaohsiung)*

In this paper, we design a high-speed and wide-bandwidth continuous-time sigma-delta modulator (CT-SDM). We emphasize the design of low power wide-bandwidth (10MHz) CT-SDM for WLAN Std. 802.11b receiver. In the application of wireless receiver, continuous-time sigma-delta ADC is more suitable than pipeline ADC. Instead of active-RC filter, we use Gm-C filter in our CT-SDM design because Gm-C filter consumes lower power and requires less limitation on op-amp. The CT-SDM is implemented with TSMC 0.35 $\mu$ m CMOS process. The proposed CT-SDM achieves a 43dB peak SNR and 48-dB DR with a 10-MHz bandwidth at a 1GHz sampling rate for WLAN Std. 802.11b. The power consumption is 17.3mW with 3.3V power supply.

## **Session C1P-H: Methodologies for Biomedical Signal Processing**

**Chair:** Hoda S. Abdel-Aty-Zohdy, *Oakland University*

**Time:** Wednesday, August 6, 2014, 9:20 - 10:10

**Location:** Poster Area

**A Novel Approach for High Speed Wireless Pre-Fall Detection Multisensory System** ..... 857

*Alfredo Lopez-Yunez (Alivo Medical Center), Diana Vasquez (Alivo Medical Center), Luis A. Palacio (Alivo*

*Medical Center), Nikhil Tiwari (Indiana University-Purdue University Indianapolis), Vinay Kumar Suryadevara*

*(Indiana University-Purdue University Indianapolis), Mobin Anandwala (Indiana University-Purdue University*

*Indianapolis), Maher Rizkalla (Indiana University-Purdue University Indianapolis)*

A hardware/software system for pre-fall detection was implemented and tested on human subjects,. The research led to efficient fast response pre-fall detection for elderly patient. The paper details the hardware and the practical results that were conducted on 10 human subjects for various fall positions. The detection of the threshold signal from the DSP unit was employed to trigger an electronic switch that turn on a mechanical safety device that inflate an airbag for patient protection.

**A New Noise Estimation Method for Neural Spike Detection** ..... 860

*Yin Zhou (Zhejiang University), Xiaolin Yang (Zhejiang University), Menglian Zhao (Zhejiang University),*

*Xiaobo Wu (Zhejiang University)*

The spike firing rate which could be rapidly changing in the recording experiment would make noise estimation inaccurate thus compromises the spike detection performance. In this paper, we propose a new noise estimation method for neural spike detection. Different from the traditional methods that deal with all the data points in the time domain, the proposed method estimates noise standard deviation by curve-fitting the neural data distribution. The experimental results show that the proposed method gives a better noise estimation accuracy under a wide range of SNRs and firing rates compared with the traditional methods and leads to a good spike detection performance.

**Design and Application of an Enhanced GA** ..... 864

*Hatem Elgothamy (Oakland University), Mohamed A. Zohdy (Oakland University),  
Hoda S. Abdel-Aty-Zohdy (Oakland University)*

This paper introduces an enhanced Genetic Algorithm GA that is faster and more efficient than the standard one. A simple 3D convex surface is optimized using different methods, Brute-Force, standard GA, and the enhanced GA. The enhanced GA is able to find the global minima within a certain range by using the least possible number of calculations which, means less processing time and is robust to parameter selections. Special software was developed using Java for this purpose; also MS-Excel was used to represent the data map as charts.

**Session C1P-J: Circuits for Processing Biomedical Signals**

**Chair:** Hoda S. Abdel-Aty-Zohdy, *Oakland University*

**Time:** Wednesday, August 6, 2014, 9:20 - 10:10

**Location:** Poster Area

**A Low Noise CMOS Readout Front End for MEMs BioPotential Sensor Applications** ..... 868

*Ahmed N. Mohamed (Military Technical College), Hesham N. Ahmed (Military Technical College)*

In this paper, a low-noise CMOS readout front end for MEMS biopotential acquisition applications is presented. The proposed circuit, implemented using 130 nm standard CMOS process, has a thermal noise floor of 10 nV/ $\sqrt{\text{Hz}}$ , a corner frequency of 300 mHz, and dissipates 3.2 $\mu\text{W}$  of power when powered using a 1 V supply. The designed circuit occupies a die area of 0.007mm<sup>2</sup> and thus renders itself as an excellent candidate for acquiring biopotential signals through MEMs sensors.

**A Novel High Speed, Low Power Intrabody Communication Receiver Front End based on Sampling Rate Boosting Switched-Capacitor Filter** ..... 872

*Hao Wang (Chinese University of Hong Kong), Chiu Sing Choy (Chinese University of Hong Kong)*

This paper presented a novel IntraBody Communication Receiver Front End (RFE) based on switched capacitor filter scheme and proposed sampling rate boosting technique. New technique aims to increase the oversampling ratio without rising system clock frequency to enhance the transmission performance. In this work, specifically, sampling rate is boosted 4 times with 50MHz system clock, which can reach 200MHz sampling frequency. Based on the measurement result, proposed RFE achieves a 2.5Mb/s data rate upon RZ coding, 170cm transmission distance and 4.14mW power. Measurement results demonstrate the effectiveness of proposed technique and its advantages compared to other conventional receiver front end circuits.

**A 128.7nW Neural Amplifier and Gm-C Filter for EEG, using gm/ID Methodology and a Current Reference without Resistance** ..... 876

*Samuel A. Gallegos (University of Texas - Pan American), Hasina F. Huq (University of Texas - Pan American)*

This paper presents a 128.7nW analog front-end amplifier and Gm-C filter for biomedical sensing applications, specifically for Electroencephalogram (EEG) use. The proposed neural amplifier has a supply voltage of 1.8V, consumes a total current of 71.59nA, for a total dissipated power of 128nW and has a gain of 40dB. Also, a 3th order Butterworth Low Pass Gm-C Filter with a 14.7nS transconductor is designed and presented. The filter has a pass band suitable for use in EEG (1-100Hz). The amplifier and filter utilize current sources without resistance which provide 56nA and (1.154nA x5) respectively. The proposed amplifier occupies an area of 0.26mm<sup>2</sup> in 0.3 $\mu\text{m}$  TSMC process.

**An Analog Front-End Circuit with Spike Detection for Implantable Neural Recording System Design** ..... 881

*Guanglei An (Oklahoma State University), Kanishka De (Oklahoma State University), Cheng Hao (Oklahoma State University), Rehan Ahmed (Oklahoma State University), Chriswell Hutchens (Oklahoma State University),  
Robert L. Rennaker II (University of Texas at Dallas)*

a low power, low noise implantable neural recording interface for use in a Radio-Frequency Identification (RFID) is presented in this paper. A two stage neural amplifier, selective reference thresholder and a serial peripheral interface for communication are integrated in this system. The midband gain of neural amplifier is 59.1dB with a 3dB bandwidth from 0.45 to 8 kHz. Input-referred noise and total power consumption are 8.7 $\mu\text{V}_{\text{rms}}$  and 3.19  $\mu\text{W}$  respectively. The thresholder detects the output signal at sampling rate of 20 kHz with four different references and the digital output is sent out through transmitter to drive light emitting diode (LED). The chip is designed and fabricated in 0.18- $\mu\text{m}$  process. The simulation result demonstrates the neural recording interface's suitability for in situ neural activity recording.



## Session C1P-K: Nanoscale Digital VLSI Design I

**Chair:** Yong-Bin Kim, *Northeastern University*

**Time:** Wednesday, August 6, 2014, 9:20 - 10:10

**Location:** Poster Area

### **SCL Design of a Pipelined 8051 ALU** ..... 885

*F.A. Parsan (University of Arkansas), J. Zhao (University of Arkansas), S.C. Smith (North Dakota State University)*

The design of a pipelined SCL 8051 ALU is elaborated. Two versions of SCL gates are considered for gate-level implementation: SCL gates with both nsleep and sleep signals and SCL gates without nsleep signal. In addition, the problem associated with pipelining the SCL 8051 ALU is explained and a solution is provided. The non-pipelined and pipelined SCL 8051 ALUs, implemented with both versions of SCL gates, are then simulated in transistor-level and compared in terms of area, speed, leakage power, dynamic power, and energy per operation.

### **Modified Fused Multiply-Accumulate Chained Unit** ..... 889

*Nasibeh Nasiri (University of Massachusetts Lowell), Oren Segal (University of Massachusetts Lowell), Martin Margala (University of Massachusetts Lowell)*

Fused multiply-add (FMA) units can reduce latency and increase energy efficiency in arithmetic operations. A modified architecture of a multiply-accumulation chained unit (MFMA) is described in this paper. The add/sub pipelined datapath of a traditional fused multiply-add unit is modified to save hardware resources, conserve energy and reduce latency in DSP applications. The proposed datapath for add/sub is flexible, generic and can be used in any IEEE-754 compatible floating point architecture as a replacement for the traditional multiply-accumulation chained unit. FMA and MFMA are both implemented in a nine-stage pipelined design. The clock limiting stage for both architectures is the normalization stage which remains unchanged in the proposed architecture. FPGA implementation for the proposed three-input add/sub and ASIC implementation for the MFMA is performed. In the FPGA implementation of the proposed add/sub datapath the area reduction is 19.56% and power reduction is 20.67% and the latency is halved compared to two cascaded two-input add/sub datapaths. In ASIC implementations of the classic FMA and MFMA the overall area reduction is 7.16% and power saving is 5.69%.

### **Robust Subthreshold 7T-SRAM Cell for Low-Power Applications** ..... 893

*Farshad Moradi (Aarhus University), Jens K. Madsen (Aarhus University)*

In this paper, a novel 7T-SRAM cell for ultra-low power applications is proposed. The proposed SRAM cell is fully functional at subthreshold voltages down to  $V_{DDmin}=200mV$ . In this technique, separate read/write bitlines and wordlines are used that makes read and write operation independent. The 7T-SRAM cell proposed in this paper, improves static read noise margin, write margin, and write time by 2.2X, 27%, and 6% in comparison to the standard 6T-SRAM cell. The 7T-SRAM cell proposed in this paper, improves write margin of the conventional 7T-SRAM cell, as well. The proposed 7T-SRAM cell is designed in 65nm CMOS technology.

### **Dynamic Power Reduction through Process and Design Optimizations on CMOS 80 nm Embedded Non-Volatile Memories Technology** ..... 897

*Jordan Innocenti (STMicroelectronics), Loic Welter (STMicroelectronics), Franck Julien (STMicroelectronics), Laurent Lopez (STMicroelectronics), Jacques Sonzogni (STMicroelectronics), Stephan Niel (STMicroelectronics), Arnaud Regnier (STMicroelectronics), Emmanuel Paire (STMicroelectronics), Karen Labory (STMicroelectronics), Eric Denis (STMicroelectronics), Jean-Michel Portal (Aix Marseille University), Pascal Masson (Université de Nice Sophia Antipolis)*

This paper describes different solutions to decrease dynamic consumption of circuits processed on an embedded non-volatile memories CMOS 80 nm technology. Up to 25 % in dynamic power reduction is demonstrated without degrading performances and static leakages of devices and above all, with full DMR compliancy. Ring oscillator designs are used to estimate the dynamic power gain, comparing new development process (B) to reference process (A) currently in use in manufacturing.

### **Dual Mode Digital Pulse Modulation (PWM & PFM) Generator ASIC for Laser Electro-Optic Q-Switching Application** ..... 901

*Ahmed M. Al-Muraeb (Oakland University and University of Baghdad), Hoda S. Abdel-Aty-Zohdy (Oakland University)*

A 4-bit Dual Mode (PWM/PFM) Digital Pulse Modulation (DMDPM) 40-pin chip was designed and simulated using MG tool. A compact design with optimized occupation area "of the unscaled chip- was achieved ( $1080\lambda \times 1105 \lambda = 324 \mu m \times 331.5 \mu m$ )  $\sim$  13.26% of the allowed area ( $3000\lambda \times 3000\lambda$ ) in a 0.5  $\mu m$ -process CMOS technology environment. The max frequency was found to be 150 MHz. A proposed system has been introduced to use our DMDPM chip for Laser Q-switching, deploying Pockels cell electro-optic modulator. It has been shown how the DMDPM chip can be used for various Lasers. Necessary system blocks has been introduced and discussed, with an illustrative design example of the proposed system/arrangement, for an Nd:YAG Laser operating at 1064 nm or 946 nm.



**A Novel Flexible 16-Core MP-SoC Architecture based on Parallel Skeletons for Image Processing Applications** .. 905

*Mohamed Amine Boussadi (Université Blaise-Pascal), Thierry Tixier (Université Blaise-Pascal), Alexis Landrault (Université Blaise-Pascal), Jean-Pierre Derutin (Université Blaise-Pascal)*

For many image processing systems, the computing power required can not be provided by a single sequential processor, this is why many designers appeal to multiprocessor systems (parallelism). This article proposes an original flexible MP-SoC (Multi-Processors System on Chip) architecture for image processing applications. Developing processors network systems tailored to a particular application domain is critical and design-time consuming in order to achieve high-performance customized solutions. This paper introduces a 16-core MP-SoC ASIC with a software configuration. In particular, each tile of the network can configure its communication links depending on the most relevant overall parallelism scheme for a targeted application. Results are shown in term of power, area and timing performance for a 65 nm CMOS technology ASIC design. A case study (grey scale histogram analyzes) is presented to illustrate the proposed flexible MP-SoC design methodology and enables to focus on architecture exploration, instantiated scheme of parallelization and timing performance.

**Leakage and Delay Analysis in FinFET Array Multiplier Circuits** ..... 909

*Joseph Whitehouse (University of Texas at San Antonio), Eugene John (University of Texas at San Antonio)*

This paper investigates the performance of array multipliers utilizing FinFET models for the following feature sizes: 20nm, 16nm, 14nm, 10nm and 7nm. Using basic array multiplier topology and standard cell 28 transistor full adders, the static power and delay of FinFET array multiplier circuits were investigated using HSPICE and low power Predictive Technology Models (PTM). Simulation results show an increase in static power and a decrease in delay as the feature size decreases. Comparisons between array multiplier sizes show nonlinear increases in both static power and delay as size increases from 4x4 up to 16x16. The results obtained in this research will provide a starting point for the design and analysis of more complex FinFET based arithmetic circuit designs.

**Session C1P-L: Nanoscale Digital VLSI Design II**

**Chair:** Carlos Silva Cardenas, *Pontificia Universidad Católica del Peru*

**Time:** Wednesday, August 6, 2014, 9:20 - 10:10

**Location:** Poster Area

**Data Retention Voltage Analysis of Various Low-Power SRAM Topologies** ..... 913

*Kester Leochico (University of Texas at San Antonio), Eugene John (University of Texas at San Antonio)*

In this paper, we analyze and compare five different low-power SRAM cell topologies in terms of their data retention voltages (DRV). The circuit simulation and analysis was carried out using HSPICE with the 45 nm, 32 nm, and 22 nm low-power Predictive Technology Model (PTM) transistor models by setting the SRAM cells to an initial state and bringing the supply voltage down to several different standby voltages. Based on these results, the standard 6T SRAM cell provides the lowest DRV out of all of the SRAM cells in this study at the 45 nm and 32 nm process nodes, but the 7T, 8T, and 10T SRAM cells provide better DRV performance at the 22 nm process node. These results give a first look at the effects that SRAM cell topology can have on DRV, and provide a starting point for future research into this topic.

**Performance Evaluation of FinFET Pass-Transistor Full Adders with BSIM-CMG Model** ..... 917

*Cecilia Garcia Martin (Illinois Institute of Technology), Erdal Oruklu (Illinois Institute of Technology)*

In this paper, multiple full adder circuits have been implemented using the FinFET device described by the BSIMCMG model. A variety of adders have been selected to compare the impact of this technology and evaluate the performance advantages that can be achieved. Full adder designs tested in this work include 28 transistor mirror adder, 10 transistor complementary and level restoring carry logic adder and ultra low power full adder (ULPFA) architectures which cover a broad spectrum of adder designs. Comprehensive simulation results demonstrate FinFET transistors' advantage in key design metrics, including reduced dynamic power, leakage current and delay. Overall, PDP gains of up to 83% is observed when compared to conventional CMOS circuits. However, FinFET pass-transistor circuits without level restorers are shown to be more vulnerable to voltage degradation compared to CMOS counterparts.

**Power Consumption Optimization Methodology (PCOM) for Low-Power/Low-Voltage 32-Bit Microprocessor Circuit Design via MTCMOS** ..... 921

*C.B. Hsu (National Taiwan University), J.B. Kuo (National Taiwan University)*

This paper presents a power consumption optimization methodology (PCOM) for low-power/ low-voltage single-cycle microprocessor circuit design via multi-threshold CMOS (MTCMOS) techniques. Based on the optimization methodology with the dual-threshold techniques, a 32-bit single-cycle MIPS microprocessor design has been optimized in terms of circuit design using dual-threshold HVT/SVT CMOS devices. According to SPICE simulation results, the power consumption of the 80,000-transistor 32-bit MIPS microprocessor, using a 90nm CMOS technology and operating at 1V with a 0.9-ns clock period, based on the optimization methodology with the dual-threshold technique, has been reduced by 27.23% during the standby period and 12.53% during the dynamic switching period as compared to the one using the conventional standard-threshold SVT CMOS devices.

**Comparison of 130 nm Technology 6T and 8T SRAM Cell Designs for Near-Threshold Operation** ..... 925

*Mika Kutila (University of Turku), Ari Paasio (University of Turku), Teijo Lehtonen (University of Turku)*

Power consumption is an important aspect of almost any electrical device design. Near-Threshold Computing (NTC) is a voltage scaling technique that makes it possible to reduce the power consumption of CMOS devices with the cost of speed and reliability. We are using NTC to design low-power cache memory circuit for a low-performance sensor-based system. Caches consume noteworthy portions of power and area of this kind of systems, and therefore reducing their power consumption has a meaningful impact on the overall power consumption of the whole system. In this paper, 8T SRAM and 6T SRAM memory cells are compared in order to establish guidelines for choosing SRAM cell constructions for NTC systems. 8T SRAM is traditionally concerned as a more reliable memory cell, but we have managed to design 6T SRAM which executes read operation with an acceptable reliability; read being the most vulnerable operation of conventional 6T SRAM cell. Also, our 6T SRAM cell has 31% smaller area and smaller power consumption.

**Applicability of Power-Gating Strategies for Aging Mitigation of CMOS Logic Paths** ..... 929

*Navid Khoshavi (University of Central Florida), Rizwan A. Ashraf (University of Central Florida), Ronald F. DeMara (University of Central Florida)*

Aggressive CMOS technology scaling trends exacerbate the aging-related degradation of propagation delay and energy efficiency in nanoscale designs. Recently, Power-gating has been utilized as an effective low-power design technique which has also been shown to alleviate some aging impacts. However, the use of MOSFETs to realize power-gated designs will also encounter aging-induced degradations in the sleep transistors themselves which necessitates the exploration of design strategies to utilize power-gating effectively to mitigate aging. In particular, Bias Temperature Instability (BTI) which occurs during activation of power-gated voltage islands is investigated with respect to the placement of the sleep transistor in the header or footer as well as the impact of ungated input transitions on interfacial trapping. Results indicate the effectiveness of power-gating on NBTI/PBTI phenomena and propose a preferred sleep transistor configuration for maximizing higher recovery.

## **Session C2L-A: Sensors**

**Chair:** Jin Liu, *University of Texas at Dallas*

**Time:** Wednesday, August 6, 2014, 10:10 - 11:50

**Location:** Mockingbird

**A CMOS Active-Pixel Image Sharpness Sensor** ..... 933

*Aditya Rayankula (New Mexico State University), Paul M. Furth (New Mexico State University)*

The technique of maximizing image sharpness is a powerful means of adaptively correcting phase aberrations in wavefronts. Crucial to this correction is a sensor that provides an accurate real-time estimate of image sharpness. In this paper, we introduce a novel image sharpness sensor using CMOS active pixel technology that computes image sharpness at a sample rate of 7.8 kHz. The sharpness sensor contains a 40x40 pixel array and is fabricated in a 0.5-um CMOS process through MOSIS. Power consumption is 12 mW. Each pixel is 24.5 x 24.5 um<sup>2</sup> with a fill factor of 20%. Experimental results obtained under open-loop static conditions show that the output value changes by 87.5% when the sensor is moved 1 cm away from the 50-cm focal point. This sensor finds potential applications in closed-loop adaptive optics systems.

**A Low-Voltage, Adaptive CMOS Centroid Image Sensor with Improved Bandwidth** ..... 937

*Kameshwar Kaushik Chavali (New Mexico State University), Paul M. Furth (New Mexico State University), Punith R. Surkanti (New Mexico State University)*

Conventional centroid architectures employ an image sensor sampled at high frame rates, analog-to-digital conversion, and digital signal processing to compute the image centroid. Latency and/or power dissipation may become prohibitively large. Therefore, fast single-chip centroid computation circuits are gaining importance in adaptive optics applications. To this end we present a fully-integrated centroid computation sensor with improved bandwidth using a transimpedance amplifier with a novel adaptive pole tracking technique. The circuit is designed to operate over five orders of magnitude of light intensity. The outputs are two signals representing the (x, y) centroid coordinates. A 48x48 pixel array was fabricated in a 0.5-um CMOS process. Chip measurements verify a bandwidth improvement of 6 times. The supply is 1.8 V, total power consumption is 2.16 mW, and core area is 2.18 mm<sup>2</sup>.

**An Improved High Speed Low Noise CMOS Image Sensor** ..... 941

*Swetha George (University of Rochester), Zeljko Ignjatovic (University of Rochester)*

We present the design and analysis of an analog CMOS image sensor as an improvement to the design presented in previous work. The current sensing and amplification is implemented using a current amplifier utilizing symmetric current mirrors which improves the bandwidth and hence the readout speed of the image sensor. In addition, faster settling time reduces the 1/f noise introduced by the in-pixel source-follower transistor of active pixel sensors with the help of the CDS circuit. We demonstrate a speed improvement of five times over the standard APS design for a current amplifier gain of five.

**A CMOS Interface for Differential Capacitive Sensors using a Time-to-Digital Converter** ..... 945

*Satomi Ogawa (University of Yamanashi)*

A high-accuracy CMOS interface for differential capacitive sensors using a time-to-digital converter (TDC) is presented for high-accuracy ratiometric operation. A capacitance-to-time converter (CTC) is developed based on a switched-capacitor (SC) sample/hold (S/H) circuit and an integrator. The proposed TDC achieves high resolution without using higher frequency clock signals. The Performances of the proposed CMOS interface are simulated by HSPICE. Simulated results have demonstrated that the proposed interface can convert the difference-to-sum ratio of sensor capacitors to digital numbers. The resolutions of 11.3 bits are achieved with calibration. The maximum nonlinear errors are smaller than 0.55 LSB. A prototype circuit built using discrete components has confirmed the principles of operation.

**Test Signal Generation for the Calibration of Analog Front-End Circuits in Biopotential Measurement Applications** ..... 949

*Li Xu (Northeastern University), Junpeng Feng (Northeastern University), Yuchi Ni (Northeastern University), Marvin Onabajo (Northeastern University)*

A test signal generator to calibrate analog front-ends for biopotential measurements is presented. The integrated signal generator enables detection of the input impedance at the front-end instrumentation amplifier based on current injection and amplitude detection. It can generate picoampere currents while ensuring a high output impedance of 2.9 gigaohms up to 100 Hz. The test signal generator was designed and simulated in 0.13 $\mu$ m CMOS technology and it consists of a temperature-compensated relaxation oscillator, a frequency divider, a limiter, and an operational transconductance amplifier.

**Session C2L-B: RF LNAs and TIAs**

**Chair:** Kamran Entesari, *Texas A&M University*

**Time:** Wednesday, August 6, 2014, 10:10 - 11:50

**Location:** Ballroom – 5

**A 3dB NF 0.1-6.6GHz Inductorless Wideband Low-Noise Amplifier in 0.13 $\mu$ m CMOS** ..... 953

*Shery Asaad Wahba Marzouk (Cairo University), Faisal A. Hussien (Cairo University), A.M. Shousha (Cairo University)*

An inductorless wide band LNA is designed with low NF and high linearity. It is based on the use of both the passive and active feedback with current reuse techniques to achieve the required low NF, high BW, and suitable gain. An auxiliary transistor is added to the differential implementation to achieve a high linearity. The circuit is designed in 0.13 $\mu$ m TSMC technology and exhibits a gain of 18.4dB over an entire bandwidth of 6.6GHz. Across the whole band of interest, the NF does not exceed 3dB, while the IIP3 is maintained above 6dBm, and it consumes 13.4mW DC power from a 1.5V supply.

**An Inductor-Less Ultra-Compact Transimpedance Amplifier for 30 Gbps in 28 nm CMOS with High Energy-Efficiency** ..... 957

*Laszlo Szilagyi (Technische Universität Dresden), Ronny Henker (Technische Universität Dresden), Frank Ellinger (Technische Universität Dresden)*

A transimpedance amplifier (TIA) for optical links with data-rate (DR) of up to 30Gbps, realized in a 28nm CMOS technology is presented. The design uses several bandwidth and gain enhancement techniques such as regulated common-gate, transimpedance boosting by current injection, transimpedance/transadmittance feedback and active inductor. The measured bandwidth is 22GHz with a power consumption of only 2mW, achieving a 0.067pJ/bit energy efficiency. The gain of the TIA is approximately 43dB $\Omega$  with only one stage. No passive planar inductors are used, therefore the area is only 0.0004mm<sup>2</sup> and is to our knowledge the smallest TIA reported to date in the 30Gbps DR range.

**A Low-Power DC-to-27-GHz Transimpedance Amplifier in 0.13- $\mu$ m CMOS using Inductive-Peaking and Current-Reuse Techniques** ..... 961

*Amir Hossein Masnadi Shirazi (University of British Columbia), Reza Molavi (University of British Columbia), Peter Sangpil Woo (University of British Columbia), Ge Yu (University of British Columbia), Shahriar Mirabbasi (University of British Columbia), Sudip Shekhar (University of British Columbia), André Ivanov (University of British Columbia)*

The growing demand for high-speed communication necessitates high-data-rate and power-efficient integrated optical link solutions. In this paper, a power-efficient CMOS transimpedance amplifier (TIA) is proposed which uses current-reuse and inductive-peaking techniques to achieve a wide bandwidth, a low input impedance, and a high gain. As a proof-of-concept, a DC-to-27-GHz TIA is designed and laid out in a 0.13- $\mu$ m CMOS process. Post-layout simulation results show that in the presence of a photo diode with a capacitance as large as 500 fF, the TIA achieves a 3-dB bandwidth of 27.3 GHz and a gain of 50 dB $\Omega$  while consuming 14.3 mW from a 1.2-V supply.

**A 40-GHz Bandwidth Transimpedance Amplifier with Adjustable Gain-Peaking in 65-nm CMOS** ..... 965

Ran Ding (University of Delaware), Zhe Xuan (University of Delaware), Tom Baehr-Jones (University of Delaware), Michael Hochberg (University of Delaware and University of Singapore)

We present the design and characterization of a broadband, low-noise transimpedance amplifier (TIA) with adjustable gain-peaking, implemented in 65-nm CMOS. The TIA exhibits 40-GHz bandwidth, 20-dB gain and consumes 107 mW power. An additional continuously-tunable 12-dB gain-peaking near 40 GHz is available through a simple yet effective tuning mechanism, consuming only 14% more power. The adjustable gain-peaking functionality incorporated in the TIA can potentially reduce power consumption and complexity of an optical receiver and is highly desirable for adaptively-equalized receiver architectures. 50 Gb/s operation is demonstrated electrically as well as in an optical testbed. A low input-referred noise current of 2.5 uArms is achieved, suggesting an average optical power sensitivity of -14.6 dBm with a 0.5 A/W PD.

**Session C2L-C: Low-Power Wireless Circuits**

**Chair:** Fan Xiaohua, *Institute of Microelectronics of Chinese Academy of Sciences*

**Co-Chair:** Bo Xia, *Feeltel Corporation*

**Time:** Wednesday, August 6, 2014, 10:10 - 11:50

**Location:** North & South 40

**A Power Reduction Technique for Wideband Common Gate Low Noise Amplifiers** ..... 969

Minghua Wang (Chinese Academy of Sciences), Minglei Zhang (Chinese Academy of Sciences), Xiaohua Fan (Chinese Academy of Sciences and Nanjing CSM-IC Inc.), Yu Liu (Chinese Academy of Sciences)

In this paper, a power reduction technique for wideband common gate low noise amplifiers (LNA) is proposed for low power application. Stacked current reused complementary capacitive cross coupling (CCCC) concept is proposed to improve LNA power efficiency. As a proof of the concept, the improved broadband differential common-gate LNAs (CG-LNA) designed in 0.18 $\mu$ m CMOS technology. The LNA achieves a 21.2dB peak voltage gain over 3dB bandwidth from 53MHz - 3.3GHz, 2.95dB minimum noise figure (NF) and -2.2dBm IIP3. The current consumption of the LNA core from 1.8V supply is 368uA.

**Practical Design Consideration in a Bluetooth Transceiver Design** ..... 973

Bo Xia (Feeltel Corp.), Yue Wu (Feeltel Corp.), Li Kang (Feeltel Corp.), Xinlong Ma (Feeltel Corp.), Xiaodong Yang (Feeltel Corp.)

The ever increasing dynamic range requirement for the RX path and maximum transmission power requirement for the TX path add difficulty in the Bluetooth transceiver design. The tradeoff between noise and linearity performance is carefully examined to meet the RX dynamic range requirement. RX anti-interference performance is improved by careful system level planning. TX non-idealities are addressed in design to achieve large usable output power. A transceiver with -92dBm sensitivity and 9dBm maximum TX power is implemented following the proposed methodology.

**RF Channelizer Architectures using Iterative Downconversion for Concurrent or Fast-Switching Spectrum Analysis** ..... 977

Harish Krishnaswamy (Columbia University), Karthik Tripurari (Columbia University), Yang Xu (Columbia University), Linxiao Zhang (Columbia University), David Gidony (Columbia University), Branislav Jovanovic (Columbia University), Peter R. Kinget (Columbia University)

We propose an RF channelizer architecture that uses the concept of 3-way Iterative Down-Conversion (IDC) to channelize a wideband incident spectrum while only using a fixed LO synthesizer. The proposed architecture can realize a concurrent channelizer that can analyze channels simultaneously, or a fast-switching channelizer that can analyze channels sequentially but with very short switching times between channels. We present an RF channelizer demonstrator prototype that was fabricated in a 65nm CMOS process. It implements a partially-concurrent architecture with the ability to concurrently down-convert a subset of channels while being able to switch very quickly between the non-concurrent channels. It splits an input spectrum of 0.6GHz-9GHz into 7 channels each of 1.2GHz bandwidth. Channelizer performance depends on the selected operation mode. The measured channel switching duration can be as fast as 8ns, and is always under 1 $\mu$ s. The chip occupies an area of 2mm x 1mm and consumes an average power of 435mW while offering a dynamic range between 58dB to 63dB based on noise and linearity performance.



**RF Digital Predistorter Implementation using Polynomial Optimization** ..... 981

*Hojat Parta (University of California, Los Angeles), Miloš D. Ercegovac (University of California, Los Angeles), Sudhakar Pamarti (University of California, Los Angeles)*

The research presented focuses on implementation of RF digital predistorters using polynomial optimization techniques. By representing the system with a set of two polynomials, we have been able to apply algebraic techniques resulting in reduction in cost of implementing digital predistorters. To test this approach we have used model of a communication channel using traveling wave tube amplifier and we have compared our method with the direct and buffered evaluation of Volterra series representing this system. Our design decreases the number of multiplications by 35% and the number of adders by 12.9% in comparison with the best technique previously used. The FPGA implementation also demonstrated decrease of 29% in DSP usage and decrease of 71.5% in logic blocks. We saw an increase of 30% in speed comparing to the previous attempts due to smaller bit-width operations and lower routing complexity of our optimized solution.

**Session C2L-D: Nanoelectronics and Neural Networks**

**Chair:** Rashmi Jha, *University of Toledo*

**Time:** Wednesday, August 6, 2014, 10:10 - 11:50

**Location:** Ballroom – 6

**Graphene and CNT based Flash Memory: Impacts of Scaling Control and Tunnel Oxide Thickness** ..... 985

*Nahid M. Hossain (University of Missouri-Kansas City), Masud H. Chowdhury (University of Missouri-Kansas City)*

For flash memory devices the thicknesses of the control and tunneling oxides in the floating gate transistor (FGT) are critical parameters. We recently proposed a floating gate transistor using multilayer graphene nanoribbon (MLGNR) and carbon nanotube (CNT). In this paper, we have analyzed the impacts of scaling the thickness of the control and tunneling oxides in the proposed MLGNR/CNT based FGT. According to ITRS, semiconductor industry has already adopted 6nm thick tunneling oxide for 18-nm and 22-nm technology nodes. By 2020, technology is expected to move to 10nm node, and 5nm tunnel oxide is predicted for 8nm-14nm nodes. For less than 20nm technology nodes, ultra-thin tunnel oxide would lead to higher tunneling current density that will affect the reliability of the flash memory cell. Based on our analysis we have provided some recommendations about the scaling of oxide thickness in the proposed MLGNR/CNT floating gate transistor.

**Impact of Coupling Capacitance on Read Operation of RRAM Devices in 1D1R Crossbar Architectures** ..... 989

*Yibo Li (University of Toledo), Wenbo Chen (University of Toledo), Wenchao Lu (University of Toledo), Rashmi Jha (University of Toledo)*

This paper presents a simulation-based study to understand the impact of coupling capacitance on the read operation of nanoscale RRAM devices in 1D1R crossbar memory architectures. Our simulation results show that the coupling capacitances can form additional sneak paths which can lead to RRAM HRS read failure. Increase in the coupling capacitance increases the transient charging current when an ultra-fast read pulse is used for the read operation. The transient charging current causes temporal reduction in LRS:HRS read current ratio which puts a limit on the read speed. This issue can be alleviated by using larger read pulses, however, this comes at the cost of higher read energy. Finally, the signature of coupling capacitance becomes more severe as the size of the crossbar increase.

**An Enhanced HSPICE Macromodel of a PCM Cell with Threshold Switching and Recovery Behavior** ..... 993

*Linbin Chen (Northeastern University), Fabrizio Lombardi (Northeastern University), Jie Han (University of Alberta)*

This paper proposes a new macromodel that takes into account the threshold switching and the resistance recovery processes in addition to the drift behavior of a Phase Change Memory (PCM). Simulation results are provided for both DC and drift behaviors; they show that the proposed macromodel is very accurate at a small error when compared with data from experimental devices. A sensitivity analysis of the macromodel is also performed to show its operation with respect to parameter variations. The model is suitable for circuit design based on PCM devices.

**Unsupervised Neuron Selection for Mitigating Catastrophic Forgetting in Neural Networks** ..... 997

*Ben Goodrich (University of Tennessee), Itamar Arel (University of Tennessee)*

Catastrophic forgetting is a well studied problem in artificial neural networks in which past representations are rapidly lost as new representations are constructed. We hypothesize that such forgetting occurs due to overlap in the hidden layers, as well as the global nature in which neurons encode information. We introduce a novel technique to mitigate forgetting which effectively minimizes activation overlapping by using online clustering to effectively select neurons in the feedforward and back-propagation phases. We demonstrate the memory retention properties of the proposed scheme using the MNIST digit recognition data set.

**A Hardware-Based Approach for Implementing Biological Visual Cortex-Inspired Image Learning and Recognition** ..... 1001

*Wenchao Lu (University of Toledo), Wenbo Chen (University of Toledo), Yibo Li (University of Toledo), Ahmed Kaake (University of Toledo), Rashmi Jha (University of Toledo)*

In this paper we report a simulation based study of large-scale image learning and recognition using neural network consisting of active pixel sensor (APS), LIF neurons, and memristive devices as synapses in crossbar array. Our studies indicate that images can be efficiently encoded into spiking-patterns using the proposed model which can be used to train the memristive devices based on spike-timing-dependent-plasticity (STDP). The proposed scheme provides a robust approach for encoding, learning, and recognizing the large-scale images using hardware-based neural-circuits.

**Session C2L-E: Surviving Challenges in Design Automation**

**Chair:** Peng Li, *Texas A&M University*

**Co-Chair:** Esteban Tlelo-Cuautle, *Institute for Astrophysics, Optics and Electronics*

**Time:** Wednesday, August 6, 2014, 10:10 - 11:50

**Location:** Ballroom – 7

**Input-Aware Statistical Timing Analysis for VLSI Delay Test and Average Design** ..... 1005

*Bao Liu (University of Texas at San Antonio)*

Nanoscale VLSI systems are subject to an ever increasing performance variability, which hinders performance scaling and increases verification complexity. In this paper, we study an often neglected source of performance variability, namely logic inputs or system workload. We present input-aware statistical timing analysis, which gives not only critical path delays but also critical path activating input patterns and critical path activation probabilities. We further present its applications in delay test for improved fault coverage and better-than-worst- case design for improved average performance.

**Homotopy-Based Direct Current Analysis with Formal Stop Criterion** ..... 1009

*H. Vazquez-Leal (Universidad Veracruzana), B. Benhammouda (Abu Dabi Men's College), K. Boubaker (Université de Tunis), Y. Khan (Zhejiang University), U. Filobello-Nino (Universidad Veracruzana), R. Castaneda-Sheissa (Universidad Veracruzana), R. Ruiz-Gomez (Universidad Veracruzana)*

Circuit simulation aids to predict and improve analog circuits performance. Direct current (DC) simulation highlights as a key tool to analyse linear and nonlinear circuits. Then, during the recent decades homotopy continuation methods (HCM) have been proposed as replacement for Newton-Raphson method (NR) to obtain operating points (OP) of nonlinear circuits. HCM has the ability to find multiple OP with global convergence, whilst NR method can only find one OP due to its characteristic of local convergence. Nonetheless, HCM lacks of a formal stop criterion to end DC simulations. Therefore, in this work, we propose a new double bounded homotopy (DBH) as a tool to find multiple OP of nonlinear circuits with a reliable mathematical stop criterion based on its property of forming closed trajectories. This kind of homotopy joins the other two reported DBH. Hence, we will show a performance comparison between the proposed method and the other two existent DBH; resulting in a better performance by the proposed HCM for a benchmark study case circuit having nine OP and containing bipolar transistors as nonlinear elements.

**A New Segmentation-Based GPU-Accelerated Sparse Matrix-Vector Multiplication** ..... 1013

*Kai He (University of California, Riverside), Sheldon X.-D. Tan (University of California, Riverside), Esteban Tlelo-Cuautle (Instituto Nacional de Astrofísica, Óptica y Electrónica), Hai Wang (University of Electronic Science and Technology of China), He Tang (University of Electronic Science and Technology of China)*

In this paper, we propose a new fast parallel sparse matrix- vector multiplication (SpMV) algorithm on GPU platforms. The new algorithm, called segSpMV, is based on the compressed sparse row (CSR) format and can be applied to wide computational applications with both structured and unstructured matrices. The SpMV operation has very low computing to communication ratio and is bandwidth- limited. The new SpMV algorithm tries to reduce the memory access by partitioning the rows, whose nonzero patterns are irregular in general, into a number of fixed-length segments. As a result, both multiplication and summation phases now can enjoy the coalesced memory access and they can be finished in one kernel launch. The summation phase can also be further improved by using GPU reduction techniques for large segment lengths. The resulting SpMV method constantly outperforms all published algorithms and the SpMV method in the recent CUSPARSE library based on a set of public matrix benchmarks.

**LEMA: A Tool for the Formal Verification of Digitally-Intensive Analog/Mixed-Signal Circuits** ..... 1017

*Andrew N. Fisher (University of Utah), Satish Batchu (Qualcomm Inc.), Kevin Jones (Lockheed Martin Corporation), Dhanashree Kulkarni (Intel Corporation), Scott Little (Intel Corporation), David Walter (Virginia State University), Chris J. Myers (University of Utah)*

The increasing integration of analog/mixed-signal (AMS) circuits into system designs has further complicated an already difficult verification problem. Recently, formal verification, which has been successful in the purely digital domain, has made some in-roads in the AMS domain. This paper describes one such formal verification tool for AMS circuits, LEMA. In particular, LEMA is capable of generating a formal model from simulation traces that, when coupled with a formal property provided in our new property language, can be model checked with one of three model checkers within LEMA. This paper briefly describes the capabilities of the LEMA AMS verification tool flow.

**Case Studies on Variation Tolerant and Low Power Design using Planar Asymmetric Double Gate Transistor** .... 1021

*Amrinder Singh (Texas A&M University), Jiang Hu (Texas A&M University)*

In nanometer technologies, low power and process variation control have emerged as the first order design goal after high performance. Short channel effects (SCEs) deteriorate the MOSFET performance and lead to higher leakage power. Process variations cause high variability in power consumption and performance of an IC which affects the overall yield. Double gate devices suppress SCEs and are potential candidates for replacing Bulk technology in nanometer nodes. Threshold voltage control in planar asymmetric double gate transistor (IGFET) using a fourth terminal provides an effective means of combating process variations and low power design. In this paper, we analyze the suitability of IGFET for variation control and low power design. We present extensive comparison between IGFET and Bulk for reducing variability, improving yield and leakage power reduction using threshold voltage modulation. BSIM-IMG models were used for IGFET based simulations. Experimental results show that IGFET is highly suitable for adaptive applications and performs better than Bulk while substantially reducing leakage power.

**Session C3L-A: Filters**

**Chair:** Ayman Fayed, *Iowa State University*

**Co-Chair:** Wei Fu, *Iowa State University*

**Time:** Wednesday, August 6, 2014, 13:10 - 14:50

**Location:** Mockingbird

**Design of Minimally-Invasive All-Pole Analog Lowpass Filters** ..... 1025

*Saiteja Damera (Texas A&M University), Aydin Ilker Karsilayan (Texas A&M University), José Silva-Martinez (Texas A&M University)*

A new design technique for minimally-invasive all-pole analog lowpass filters is introduced. The proposed method has minimal impact on the in-band signal in terms of added noise and nonlinearity, whereas it has comparable performance for out-of-band signals with smaller number of active devices. Simulation results for third and fifth order lowpass filters show approximately 30dB improvement in in-band linearity when compared to conventional filter topologies.

**A Low-Power 84-dB Dynamic-Range Tunable Gm-C Filter for Bio-Signal Acquisition** ..... 1029

*Junjie Lu (University of Tennessee), Tan Yang (University of Tennessee), M. Shahriar Jahan (University of Tennessee), Jeremy Holleman (University of Tennessee)*

A tunable Gm-C filter is presented for bio-signal acquisition application. It incorporates linear tunable trans-conductors utilizing MOSFETs biased in the triode region. Both the filter architecture and transconductor circuit design are optimized for good tuning, linearity and noise performance with low power consumption. The filter was fabricated in a 0.6 um BiCMOS process, occupying 0.17 sqmm. Measurement results show a tuning range of cut-off frequency from 2.5 kHz to 10 kHz. At 5 kHz cut-off frequency, the filter achieves a dynamic range of 85 dB with 1% THD, and consumes 75.9 uW from 3.3 V supply.

**Low-Power Duty-Cycle Tuned Filters** ..... 1033

*Xin Meng (Oregon State University), Gabor C. Temes (Oregon State University)*

Duty-cycle tuned switched-resistor-MOSFET-C filters can achieve excellent linearity and wide tuning range. In this letter, a switched-capacitor circuit is described which can provide the required bias voltage for the opamp, and relax the driving requirement of the previous block. Correlated double sampling circuit is also realized by the switched-capacitor circuit, to effectively suppress the offset voltage and flicker noise of the amplifier.

**Reduced Clock Harmonic Distortion Technique in Maximum Tunable Switched-R-MOSFET-C Filters** ..... 1037

*Arunvenkatesh Alagappan (Texas A&M University), Sergio Soto-Aguilar (Texas A&M University),  
Edgar Sánchez-Sinencio (Texas A&M University)*

In this paper a method to reduce the harmonic distortion caused by the switching operation in switched-R-MOSFET-C filters is presented. The technique is demonstrated through simulations and backed by analytical expressions for first order active RC and second order biquad filters; the improvement in clock distortion is presented and compared with previously reported architectures. The proposed harmonic cancellation technique shows an improvement of more than 33 dB over previous architectures without compromising the tuning range.

**A Fully-Differential CMOS Low-Pass Notch Filter for Biosignal Measurement Devices with High Interference Rejection** ..... 1041

*Kainan Wang (Northeastern University), Chun-Hsiang Chang (Northeastern University),  
Marvin Onabajo (Northeastern University)*

A fifth-order fully-differential CMOS low-pass notch filter with high interference rejection is presented to provide an interface to the instrumentation amplifier in biopotential and bioimpedance measurement devices. The filter employs operational transconductance amplifiers with differential difference input stage. Designed in 0.13 $\mu$ m CMOS technology, it has a simulated bandwidth of 47.7Hz, covering the electroencephalography (EEG) frequencies from 1 to 40Hz with a notch of 73.2dBc at the 60Hz power line frequency. The fully-differential structure provides high common-mode rejection and power supply rejection as demonstrated by system simulations (amplifier and filter) resulting in a CMRR of 101.3dB and a PSRR of 64.7dB.

**Session C3L-B: Design Techniques for ADCs**

**Chair:** Vishal Saxena, *Boise State University*

**Time:** Wednesday, August 6, 2014, 13:10 - 14:50

**Location:** Ballroom – 5

**Double-Sampled Wideband Delta-Sigma ADCs with Shifted Loop Delays** ..... 1045

*Xin Meng (Oregon State University), Tao He (Oregon State University), Yi Zhang (Oregon State University),  
Gabor C. Temes (Oregon State University)*

Double sampling for delta-sigma ADCs is an effective technique for wideband and low-power data conversion. This paper proposes a double-sampled delta-sigma modulator topology with shifted loop delays. Compared with existing double-sampled modulators, this architecture implements the inherent quantization delay by shifting the delay from the last integrator to the quantizer, and it relaxes critical timing for DEM by shifting the delay from the first integrator to the feedback path. Also, by inserting one more delay in the signal path, the proposed modulator keeps the low-distortion property. To verify the effectiveness of the proposed topology, a second-order double-sampled delta-sigma modulator was designed and simulated.

**PN-Assisted Deterministic Digital Calibration of Split Two-Step ADC to Over 14-Bit Accuracy** ..... 1049

*Sudipta Sarkar (University of Texas at Dallas), Yuan Zhou (University of Texas at Dallas),  
Yun Chiu (University of Texas at Dallas)*

A digital calibration technique to linearize capacitor mismatch, residue amplifier gain, and nonlinearity in a two-step ADC based on the split-ADC technique [1] is presented. Although multiple publications have been reported before on the split-calibration of pipelined ADC's, none of them is comprehensive, meaning capacitor mismatch, residue gain, and linearity are never treated in one work at the same time. We extend the offset double conversion technique [2] to adapt it to the split- ADC architecture for seamless calibration of all static nonlinearities in a split pipelined two-step ADC. Behavioral simulation results demonstrate the effectiveness of the technique, in which the SNDR and SFDR performance of a 15-bit two-step ADC are improved from 42 dB and 50 dB to 88 dB and 103 dB on average, respectively.

**A 1.1mW, 63.7dB-SNDR, 10MHz-BW Hybrid Voltage-Time Domain ADC** ..... 1053

*Amit Kumar Gupta (University of Texas at Austin and Texas Instruments Inc.), Krishnaswamy Nagaraj (Texas  
Instruments Inc.), T.R. Viswanathan (University of Texas at Austin)*

In this paper we present the design of a Nyquist rate VCO based ADC implemented in 65nm CMOS process. The design achieves a peak SNDR of 63.7dB and a SFDR of 76dB in 10MHz bandwidth while consuming 1.1mW of power and occupying only 0.07mm<sup>2</sup> of active area. The pseudo-differential VCO implemented in the prototype achieves better than 9-bits linearity with the overall ADC linearity better than 12 bits. The figure of merit (FoM) is 44fJ/conversion and should improve when implemented in more advanced processes.



**A High Resolution Transimpedance Amplifier for use in a 10-Bit 200 MS/s Current Mode SAR ADC** ..... 1057  
*Abdelrahman Elkafrawy (Universität Ulm), Jens Anders (Universität Ulm), Maurits Ortmanns (Universität Ulm)*

An approach towards a high speed current mode SAR ADC is presented. Even though SAR ADCs based on charge redistribution have been significantly improved in efficiency and operating frequency, they are still limited by the settling requirements of the switched capacitor DAC. To overcome this limitation, we propose the use of a current mode SAR ADC incorporating a current steering DAC operating at 2 GS/s and an overall Nyquist rate conversion speed of 200 MS/s. In this paper, the main focus is placed on the design of a high-resolution low-input-impedance transimpedance amplifier (TIA) used as the comparator preamplifier in the proposed current mode SAR ADC. For high-speed operation, trade-offs between input resistance, noise and voltage headroom pose challenges in the design of the high-speed TIA. Our analysis is compared against a schematic level implementation in a 1.2 /1.8 V 90 nm CMOS technology. The TIA implementation is simulated on transistor level to achieve an overall resolution of 10 bit in the proposed current based SAR ADC together with the input Gm and current steering DAC over a Nyquist band from DC to 100 MHz.

**An Overview of Digital Calibration Techniques for Pipelined ADCs** ..... 1061  
*Bibhudatta Sahoo (Amrita University)*

As device dimensions and supply voltage are shrinking, the design of high-speed and high-resolution analog-to-digital converters (ADCs) is getting more and more challenging. Since the shrinking device sizes enable high-speed and low-power digital circuits, there has been a trend to use digital circuits to estimate and correct for the analog circuit nonidealities (i.e. calibrate) to realize high-performance ADCs. This summary paper enumerates some of the digital techniques that have been adopted in the past two decades to realize high-speed high-resolution pipelined ADCs, which are typically used in communication and imaging applications.

**Session C3L-C: On-Chip Built-In Test and Self-Calibration Techniques**

**Chair:** Marvin Onabajo, *Northeastern University*

**Co-Chair:** Yong-Bin Kim, *Northeastern University*

**Time:** Wednesday, August 6, 2014, 13:10 - 14:50

**Location:** North & South 40

**Design of Self-Healing Mixed-Signal/RF Systems and Support CAD Tools: A Scalable Approach** ..... 1065

*A. Chatterjee (Georgia Institute of Technology), H. Wang (Georgia Institute of Technology), A. Banerjee (Texas Instruments Inc.), D. Banerjee (Georgia Institute of Technology), V. Natarajan (Intel Corporation), S. Sen (Intel Corporation), S. Devarakond (Intel Corporation)*

Due to the proliferation of nanometer CMOS mixed-signal/RF circuits and a push towards high operating speeds (5-100 Ghz+), there has been renewed interest in the design of high-speed circuits and systems that can self-calibrate and self-heal post-manufacture and in the field. In the past, designers have invented self-healing mechanisms that are tailored towards specific (critical) mixed-signal/RF performance metrics of specific circuit architectures (transmitter, receiver, etc). What is desired, however, is the ability to monitor multiple performance metrics concurrently and trade them off against one another in an optimal manner, through performance tuning mechanisms, to satisfy system-level Quality of Service (QoS) guarantees. Further, the methods employed must be scalable across different device types/circuit architectures and supported by CAD tools that enable automation of self-healing design procedures. In this paper, recent research advances are presented that allow low cost and rapid self-healing of complex mixed-signal/RF systems and enable the development of design automation tools to support such activity across diverse performance metrics and circuit types.

**A Novel BIST Technique for LDMOS Drivers** ..... 1069

*Bruce Kim (City University of New York), Saikat Mondal (City University of New York), Friedrich Taenzler (Texas Instruments Inc.), Kenneth Moushegian (Texas Instruments Inc.)*

In this paper we describe a novel Built-in-Self-Test (BIST) method using a voltage comparator to detect gate-oxide and drain leakage current for LDMOS by applying a pulse test stimulus. A temperature calibration circuit was also designed for LDMOS-based motor drivers.

**On-Chip Sensor Selection for Effective Speed-Binning** ..... 1073

*Qihang Shi (University of Connecticut), Mohammad Tehranipoor (University of Connecticut), Xiaoxiao Wang (Freescale Semiconductors), LeRoy Winemberg (Freescale Semiconductors)*

Advance in technology nodes of IC fabrication has introduced increased variation. This presents new challenges for delay testing. To address this challenge, speed-binning based on on-chip delay sensor measurements has been proposed as alternative to current speed-binning methods. This practice requires advanced data analysis techniques for the binning result to be accurate. In this paper, based on experiments with silicon data collected from on-chip delay sensors in a commercial design using sub-65 nm process, we demonstrate that optimizing sensor selection can benefit speed-binning accuracy. An optimization algorithm is presented, and result showed it is capable of improving accuracy beyond 93%.

**On-Chip Intelligence: A Pathway to Self-Testable, Tunable, and Trusted Analog/RF ICs** ..... 1077  
*Dzmitry Maliuk (Yale University), Yiorgos Makris (University of Texas at Dallas)*

This paper introduces the concept of on-chip intelligence, in the form of an analog neural classifier integrated alongside an analog/RF circuit, as well as its applications in facilitating built-in self-test, post-production Performance calibration, as well as trust evaluation through hardware Trojan detection.

**Review of Temperature Sensors as Monitors for RF-MMW Built-In Testing and Self-Calibration Schemes** .... 1081  
*J. Altet (Polytechnical University Catalonia), E. Aldrete-Vidrio (Polytechnical University Catalonia),*

*F. Reverter (Polytechnical University Catalonia), D. Gómez (Broadcom Corporation), J.L. González (CEA-Leti), M. Onabajo (Northeastern University), J. Silva-Martinez (Texas A&M University), B. Martineau (STMicroelectronics), X. Perpiñà (Universitat Autònoma de Barcelona), L. Abdallah (CNRS, TIMA), H. Stratigopoulos (CNRS, TIMA), X. Aragonés (Universitat Politècnica de Catalunya), X. Jordà (Universitat Autònoma de Barcelona), M. Vellvehi (Universitat Autònoma de Barcelona), S. Dilhaire (Université Bordeaux I), S. Mir (CNRS, TIMA), D. Mateo (Universitat Politècnica de Catalunya)*

This paper presents an overview of the work done so far related to the use of temperature sensors as performance monitors for RF and mmW circuits with the goal to implement built-in testing or self-calibration techniques. The strategy is to embed small temperature sensors on the same silicon die as the circuit under test, taking advantage of empty spaces in the layout. This paper reviews the physical principles, and presents examples that reveal how temperature sensors can be used as functional built-in testers serving to reduce testing costs and enhance yield as part of self-healing strategies.

**Session C3L-D: Speech Processing**

**Chair:** Genevieve sapijaszko, *UCF/Devry*

**Co-Chair:** Waleed Alrasheed, *King Fahd U Saudi Arabia*

**Time:** Wednesday, August 6, 2014, 13:10 - 14:50

**Location:** Ballroom – 6

**Speech Enhancement based on a Modified Spectral Subtraction Method** ..... 1085  
*Md T. Islam (Bangladesh University of Engineering and Technology), C. Shahnaz (Bangladesh University of Engineering and Technology), S.A. Fattah (Bangladesh University of Engineering and Technology)*

In this paper, a noisy speech enhancement method based on modified spectral subtraction performed on short time magnitude spectrum is presented. Here the cross-terms containing spectra of noise and clean signals are taken into consideration which are neglected in the traditional spectral subtraction method on the basis of the assumption that clean speech and noise signals are completely uncorrelated which is not true for most of the noises. In this method, the noise estimate to be subtracted from the noisy speech spectrum is proposed to be determined exploiting the low frequency regions of noisy speech of the current frame rather than depending only on the initial silence frames. By employing the noise estimates thus obtained, a procedure is formulated to reduce noise from the magnitude spectrum of noisy speech signal. The noise reduced magnitude spectrum is then recombined with the unchanged phase spectrum to produce a modified complex spectrum prior to synthesizing an enhanced frame. It is shown through extensive simulations that the proposed method consistently outperforms one of the state-of-the-art methods of speech enhancement.

**An Approach to Vowel Recognition using 2D-DWT based Visual Information of the Lip Region** ..... 1089  
*S.A. Fattah (Bangladesh University of Engineering and Technology), A.H.M. Rubaiyat (Bangladesh University of Engineering and Technology), M.M. Hassan (Bangladesh University of Engineering and Technology)*

In this paper, a vowel recognition scheme using visual information is proposed based on two dimensional discrete wavelet transform (2D-DWT). First, a video frame corresponding to a steady vowel zone is selected utilizing the speech characteristics of audio frames. Next, a pixel-based method is proposed to identify the lip region of a given video frame, where intensity variation of different color planes is utilized. The 2D-DWT is then employed on a combined image plane extracted by using the weighted sum of red and green plane pixels of the lip image. Lower order wavelet coefficients obtained after second level decomposition and differences among those coefficients are used as proposed features. Leave one out cross validation technique is used to test the classification accuracy where a distance based classifier is used. Performance of the proposed method is tested on a publicly available standard audiovisual database and a high level of recognition accuracy is achieved using only extracted visual features.

**A Feature Extraction Scheme based on Enhanced Wavelet Coefficients for Speech Emotion Recognition** ..... 1093

*C. Shahnaz (Bangladesh University of Engineering and Technology), S. Sultana (Bangladesh University of Engineering and Technology)*

This paper proposes a feature extraction scheme for speaker-independent Speech Emotion Recognition. The feature is derived from the Teager energy operated wavelet coefficients of speech. The wavelet coefficients thus enhanced is used to compute entropy. The feature vector is fed to unsupervised K-means clustering in a nonhierarchical process and is then used in a supervised KNN classifier. It is seen that KNN classifier is more capable of distinguishing emotions when a hierarchical approach is followed. Detail simulations using EMO-DB German speech emotion database show that the proposed feature with supervised hierarchical classification approach provides the higher accuracy.

**Session C3L-E: Energy Efficient System Solutions**

**Chair:** Neeraj Magotra, *Energy Efficient System Solutions*

**Time:** Wednesday, August 6, 2014, 13:10 - 14:50

**Location:** Ballroom – 7

**Low Power Algorithms for Hearing Aid and Embedded Applications** ..... 1097

*Robert L. Brennan (ON Semiconductor)*

This paper is a concise overview of current low power hearing aid DSP architectures

**Design of a Speed Controller using Extended Kalman Filter for PMSM** ..... 1101

*Warsame H. Ali (Prairie View A&M University), Mamatha Gowda (Prairie View A&M University), Penrose Cofie (Prairie View A&M University), John Fuller (Prairie View A&M University)*

A novel design of a proportional-integral-differential equivalent controller using state observer based Extended Kalman Filter (EKF) for a Permanent Magnet Synchronous Motor (PMSM) is proposed. The EKF is constructed to achieve a precise estimation of the speed and current from the noisy measurement. Linear Quadratic Regulator (LQR) technique is used to construct a proportional integral derivative (PID) controller to achieve the speed command tracking performance. The proposed method greatly enhances the speed control performance. The simulation results for the speed response and variation of the states when the PMSM is subjected to the load disturbance are presented. The results verify the effectiveness of the proposed method.

**Designing an Energy Efficient Digital Signal Processing Hearing Aid System** ..... 1105

*Neeraj Magotra (Western New England University and Acoustic Acuity Inc.)*

This paper focuses on design issues related to the development of an energy efficient Digital Signal Processing (DSP) hearing aid system that can result in various DSP hearing aid products. The approach is predicated on utilizing commercially available DSP chips while meeting system requirements and end-user expectations. It describes how energy efficiency can be achieved at various levels, designing and tailoring the necessary algorithms to consume less power, selecting appropriate components with a focus on functionality "satisfying end-user expectations. The approach has led to the development of binaural DSP hearing aids in various form factors.

**Trends in Camera based Automotive Driver Assistance Systems (ADAS)** ..... 1110

*Shashank Dabral (Texas Instruments Inc.), Mihir Mody (Texas Instruments India Pvt Ltd.), Sanmati Kamath (Texas Instruments Inc.), Buyue Zhang (Texas Instruments Inc.), Vikram Appia (Texas Instruments Inc.), Umit Batur (Texas Instruments Inc.)*

Advance Driver Assistance Systems (ADAS), once limited to high end luxury automobiles are fast becoming popular with Mid and entry level segments driven in part by legislation coming in to effect in the latter part of this decade. These systems require support for a wide variety of applications, from surround-view visual systems to safety critical vision applications (eg Pedestrian Detect, automatic braking etc). In this white paper we describe some of the existing and emerging trends and applications in each of these segments along with the requirements and motivations for each of these features. We also highlight TI's automotive class TDA2x device, a state of the art automotive grade device capable of handling complex ADAS applications within a low power and cost budget.