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Technical Sessions

Monday, September 15 – Wednesday, September 17

2-2 10:30 am **A 50 - 64 Gb/s Serializing Transmitter With a 4-tap, LC-Ladder-Filter-Based FFE in 65-nm CMOS** pg. 6

Ming-Shuan Chen, Chih-Kong Ken Yang, University of California, Los Angeles

This paper presents a complete 50-64 Gb/s serializing transmitter including a 4-tap equalizer. The serializer is power-optimized by using a direct 4:1 multiplexer (MUX) at the final stage with a novel 4:1 MUX circuit design. In addition, an LC- based FFE structure that eliminates the need of multiple MUXs is proposed. The FFE improves the bandwidth of the delay line and the output combiner by applying the design methodology of LC-ladder filters. By properly arranging the output combiner, the required number of inductors and the area is minimized. Designed and fabricated in 65-nm CMOS technology, the transmitter achieves a maximum data rate of 64.5 Gb/s with an energy efficiency of 3.1 pJ/bit.

2-3 10:55 am **An 8GHz First-order Frequency Synthesizer based on Phase Interpolation and Quadrature Frequency Detection in 65nm CMOS** pg. 10

S. Saeedi, A. Emami, California Institute of Technology, Pasadena

An 8GHz low-power frequency synthesizer in 65nm CMOS is presented. The design features a new architecture and a novel quadrature frequency detection technique for fine-tuning. The output clock at 8GHz has an integrated rms jitter of 0.5ps and peak-to-peak periodic jitter of 2.9ps. The system consumes 2.49mW from a 1V supply at 8GHz.

2-4 11:20 am **A 12.5-Gb/s Self-Calibrating Linear Phase Detector-based CDR using 0.18µm SiGe BiCMOS** pg. 14

J. Walker, J. Kenney, J. Bankman, T. Chen, S. Harston, K. Lawas, A. Lewine, R. Soenneker, M. St. Germain, W. Titus, A. Wang, K. Tam, Analog Devices

A 12.5 Gb/s half-rate linear phase detector-based clock and data recovery circuit is described. Using a linear phase detector minimizes the number of latches required. To correct for static phase offsets, a low-overhead calibration scheme is used, improving measured high-frequency jitter tolerance by up to 0.2 UIpp.

2-5 11:45 am **A 6.5Mb/s to 11.3Gb/s Continuous-Rate Clock and Data Recovery** pg. 18

Jack Kenney, Terry Chen, Larry DeVito, Declan Dalton, Stuart McCracken, Richard Soenneker, Ward Titus, Todd Weigandt, Analog Devices Inc.

A continuous-rate CDR based upon a digital dual delay/phase locked loop is reported. This CDR is implemented in 0.13µm CMOS and operates from 6.5Mb/s to 11.3Gb/s. It exceeds all SONET jitter specifications from OC-3 to OC-192, with random jitter of 452fs at 9.95Gb/s. The die area is 2X2mm2, and is implemented in a 24-pin LFCSP.

Session 3 – Design Technology Co-optimization for 10 nm and Beyond pg.22

Monday, 9/15, 10:00 am
Fir Ballroom
Session Chair: Takamaro Kikkawa, Hiroshima University
Session Co-chair: Rajiv Joshi, IBM T.J. Watson Research Center

10:00 am **Introduction**

This session focuses on the dilemma in technology-circuit interaction beyond 10nm. Advanced devices and lithographic considerations are highlighted. This session further covers silicon carbide IC and carbon nanotube digital circuit design.

3-1 **Progress and Future Challenges of Silicon Carbide Devices for Integrated Circuits** **pg. 23**
10:05am *T. Kimoto, Kyoto University*

SiC is a wide bandgap semiconductor having superior physical properties. While discrete high-voltage SiC power devices have been developed, SiC is also attractive for advanced integrated circuits operating in high-temperature and radiation-hard circumstances. This paper reviews the present status and technological challenges of SiC devices and circuits.

3-2 **Robust Design and Experimental Demonstrations of Carbon Nanotube Digital** **pg. 29**
10:30 am **Circuits (Invited)**
Gage Hills, Max Marcel Shulaker*, Hai Wei*, Hong-Yu Chen*, H.-S. Philip Wong*, Subhasish Mitra*,**, *Department of Electrical Engineering, Stanford University, **Department of Computer Science, Stanford University*

Carbon nanotube field-effect transistors (CNFETs) are excellent candidates for building highly energy-efficient digital systems. However, carbon nanotubes (CNTs) are inherently highly subject to imperfections and variations that pose major obstacles to the design of robust and very-large-scale CNFET digital systems. This paper presents an overview of imperfection-immune design and robust CNT processing techniques that enabled the demonstration of the first CNT computer. We also present an overview of a systematic methodology that combines CNT process improvements and CNFET circuit design techniques to overcome CNT variations.

3-3 **Design Technology Co-optimization for N10 (Invited)** **pg. 37**
11:20 am *J. Ryckaert, P. Raghavan, R. Baert, M. G. Bardon, M. Dusa*, A. Mallik, S. Sakhare, B. Vandewalle, P. Wambacq, B. Chava, K. Croes, M. Dehan, D. Jang, P. Leray, T-T. Liu, K. Miyaguchi, B. Parvais, P. Schuddinck, P. Weemaes, A. Mercha, J. Bömmels, N. Horiguchi, G. McIntyre, A. Thean, Z. Tökei, S. Cheng, D. Verkest, A. Steegen, imec and *ASML Belgium*

Design-Technology co-optimization becomes key to enable CMOS scaling. We evaluate the technology options that are considered to enable N10 scaling by exploring their impact on representative designs such as standard cells, SRAM and analog contexts. This paper illustrates that design needs to be considered early in technology development.

Session 4 – Advanced Techniques for Power Amplifers and Duplexers N/A

Monday, 9/15, 10:00 am
Pine Ballroom
Session Chair: Ehsan Afshari, Cornell University
Session Co-chair: Hua Wang, Georgia Institute of Technology

10:00 am **Introduction:**

This session showcases recent advances in front-end circuits including power amplifiers and duplexers at RF and mm-wave frequencies in silicon technology.

4-1 **A New Wave of CMOS Power Amplifier Innovations: Fusing Digital and Analog** **pg. 45**
Techniques with Large Signal RF Operations (Invited)

10:05 am *Shouhei Kousai, Kohei Onizuka, Song Hu*, Hua Wang*, and Ali Hajimiri**, Toshiba Corp., *Georgia Institute of Technology, **California Institute of Technology*

This paper reviews several recently reported circuit design techniques of CMOS PAs. These techniques all take advantage of the computation and integration advantages of CMOS process and can potentially lead to competitive PA solutions compared to traditional III-V HBT PA solutions.

4-2 **A mm-Wave Class-E 1-bit Power Modulator pg. 53**
10:55 am *K. Datta, H. Hashemi, University of Southern California*

A Q-band Class-E 1-bit power modulator is demonstrated in a 0.13µm SiGe HBT BiCMOS process for high-speed digital polar transmitters at mm-waves. A double-stacked SiGe HBT `beyond BVCEO' switching Class-E architecture has been used to generate high power while maintaining high efficiency at mm-waves. Using a novel architecture of input switching in a Class-E architecture biased with negligible quiescent current, both high peak PAE under continuous wave operation as well as high average efficiency under OOK modulation are maintained. The fully integrated 46 GHz prototype demonstrates a measured saturated output power of 21.8 dBm with peak PAE ≈ 18.5% under static (continuous wave) operation as well as average power of 18 dBm under 1 Gbps OOK modulation with average PAE ≈ 10 %.

4-3 **A Millimeter-Wave Tunable Transformer-Based Dual-Antenna Duplexer with 50 dB pg. 57**
11:20 am **Isolation**
C. Lu, M. Matters-Kammerer, R. Mahmoudi, P. G.M. Baltus, Eindhoven University of Technology, The Netherlands

This paper presents a tunable millimeter-wave transformer-based duplexer with dual-antenna configuration. By using orthogonal linearly-polarized antennas and the transformer-based duplexer, the transmitter and receiver duplexes the two antennas with orthogonal circularly-polarized signals. Magnetic tuning is introduced to improve isolation in case of practical imbalances. Measurement results demonstrates an isolation of > 50 dB by the duplexer for a 1 GHz bandwidth. The achieved NF is 4.1 dB and insertion loss in the TX path is 3.1 dB.

4-4 **A 1.6-2.2GHz 23dBm Low Loss Integrated CMOS Duplexer pg. 61**
11:45 am *Mohamed Elkholy, Mohyee Mikhemar*, Hooman Darabi*, Kamran Entesari, Texas A&M University, *Broadcom Corp.*

This paper presents a tunable integrated electrical balanced duplexer as a compact alternative to multiple bulky SAW and BAW duplexers. A floating balancing network creates a replica of the TX signal for cancellation at the input of a single-ended LNA, thus enabling high power operation. It achieves around 50dB isolation within 1.6-2.2GHz range. The cascaded noise figure of the duplexer and LNA is 6.5dB, and the TXIL of the duplexer is about 3.2dB. The maximum achieved TX power is around 23dBm suitable for WCDMA transceivers. The duplexer and LNA are implemented in CMOS 0.18µm and occupy an active area of 0.35mm^2.

Educational Session

Educational Session 1 - Calibrated Time-Interleaved High-Speed ADCs pgs. 65-117

Monday, September 15, 10:00 am, Cedar Ballroom
Speaker: Aaron Buchwald, Entropic Communications

Software-defined RF front-ends and cognitive radios are now becoming a reality thanks to advances in ADC technology that allow quantization as close to the antenna as possible. Recent ADCs that take advantage of time-interleaving and rely heavily on calibration have enabled new receiver architectures where the entire spectrum is digitized. All tuner functions, including channelization and demodulation are then accomplished completely in the digital domain. Such systems that are "RF-to-Digital" have many advantages. However, the design of the requisite ADC remains a challenge to achieve wide-bandwidth and high dynamic-range at very low power. Other baseband systems at tens of gigasamples-per-second are also moving towards ADC-based solutions. These include 100-200- and 400 Gb/s optical as well as 100-Gb/s Serdes for backplanes and interconnect. Time-interleaved ADCs are necessary in these applications too, although the ADC requirements are different than for full-band capture frequency-domain multi-access channels. This talk introduces key concepts of calibrated time-interleaved ADCs at a tutorial level. Examples of specific solutions are presented. Advanced concepts are also introduced and the differences between requirements for broadband capture ADCs and baseband ADCs will be discussed.

Session 5 – Design for Data-Center, Low-Power and SoCs pg. 118

Monday, 9/15, 1:30 pm
Oak Ballroom
Session Chair: Rick Paul, Cisco Systems, Inc.
Session Co-chair: Aurangzeb Khan, Altia Systems

1:30 pm **Introduction:**

State-of-the-art processor/SoC results on 22nm SOI and 28nm bulk CMOS. Enabling technology for multi-terrabit interconnect bandwidth and new circuit techniques for ultra-low power.

5-1 1:35 pm **POWER8 Design Methodology Innovations for Improving Productivity and Reducing Power (Invited)** **pg. 119**
Matthew M. Ziegler, Ruchir Puri, Bob Philhower, Robert Franch, Wing Luk, Jens Leenstra, Peter Verwegen, Niels Fricke, George Gristede, Eric Fluhr, Victor Zyuban, IBM

The design complexity and power consumption of modern high performance processors calls for innovative design methodologies. This paper describes new design approaches employed by the POWER8 processor design team to address complexity and power consumption challenges.

5-2 2:25 pm **AMD SOC Power Management: Improving Performance/Watt Using Run-time Feedback** **pg. 128**
W.L. Bircher, S. Naffziger, AMD

This paper presents an analysis of four run-time power management features implemented in AMD's recent 28nM APU. These features optimize SOC performance by shifting power and frequency resources in response to workload characteristics. The Global Efficient APM (GEAPM), Core-Bound Boost (CBB) and Memory-Bound Boost (MBB) features are shown to provide a performance improvement of up to 76%, 4.3% and 12.5% respectively. The Local Efficient APM (LEAPM) feature is shown to reduce average CPU power consumption by 34% while reducing performance by less than 1%.

5-3 2:50 pm **A 0.42V Vccmin ASIC-Compatible Pulse-Latch Solution as a Replacement for a Traditional Master-Slave Flip-Flop in a Digital SOC** **pg. 132**
Sang H. Dhong, Richard Guo, Ming-Zhang Kuo, Ping-Lin Yang, Cheng-Chung Lin, Kevin

Huang, Min-Jer Wang, Wei Hwang, Taiwan Semiconductor Manufacturing Company and *National Chiao-Tung University*

A new pulse generator with a wide operating range and reduced dependence on the input rise-time and PVT variations is presented. It enables a simpler DCR design which drives pulse latches with robustness, opening a door to building a digital SOC with mostly pulse latches, saving area, power, and speed.

3:15 pm **BREAK**

5-4 3:30 pm **Thermal Modeling Methodology for Efficient System-Level Thermal Analysis** **pg. 136**
Cristiano Santos, Pascal Vivet**, Gene Matter***, Nicolas Peltier***, Sylvian Kaiser***, Ricardo Reis*, *UFRGS, **CEA-Leti, ***DOCEA Power Inc.*

This paper presents a thermal modeling approach which associates material homogenization and model reduction, enabling to handle fine-grain structures from 3D integration in multi-length scale systems. Comparisons between simulations and characterization data for a complete system including packaged 65nm memory-on-logic 3D circuit show an average error of 3.96%. The thermal impact of TSV arrays, stacking configuration and die thickness is also presented, demonstrating the presented thermal modeling approach enables quick system-level design exploration and what-if analysis for design and technology parameters.

5-5 3:55 pm **MBus: A 17.5 pJ/bit/chip Portable Interconnect Bus for Millimeter-Scale Sensor Systems with 8 nW Standby Power** **pg. 140**
Ye-Sheng Kuo, Pat Pannuto, Gyouho Kim, Zhiyoong Foo, Inhee Lee, Ben Kempke, Prabal Dutta, David Blaauw, Yoonmyung Lee, University of Michigan

We propose MBus, an ultra-low power interconnect bus for millimeter size wireless sensor nodes. Our bus uses only 4 IO pads, features "clockless" member nodes, and aggressively power gates. MBus is fully synthesizable with robust timing. We implement MBus in 180 nm technology and achieve 8 nW of standby power and 17.55 pJ/bit/chip.

5-6 4:20 pm **Highly Energy-efficient and Quality-tunable Inexact FFT Accelerators** **pg. 144**
Avinash Lingamneni , Christian Enz, Krishna Palem and Christian Piguet**; Rice University, *EPFL-Switzerland, **CSEM-Switzerland*

We present inexact Fast Fourier Transform (FFT) accelerators that can realize energy-accuracy tradeoffs taking advantage of various inexact design techniques in conjunction with machine-learning inspired waveform shaping technique. A 65nm ASIC test chip with inexact FFTs shows a reduction in datapath and total energy consumption upto 75% and 45% respectively when compared to a conventional exact FFT at marginal Signal-to-Noise Ratio losses between 0.0002 dB to 1 dB.

5-7 4:45 pm **Enabling Flexible Datacenter Interconnect Networks with WDM Silicon Photonics** **pg. 148**
G.A. Fish, D.K. Sparacin, Aurrion

The heterogeneous integration of InP material into a silicon photonics wafer flow enables high performance photonic integrated circuits to be fabricated using established silicon foundry infrastructure. Aurrion has established a library of photonic circuit elements which can be combined to form the single chip solutions for products next generation datacenter.

5-8 **CMOS (Sub)-mm-Wave System-on-Chip for Exploration of Deep Space and Outer** **pg. 154**

5:10 pm **Planetary Systems (Invited Paper)**
Adrian. Tang **, M.-C. Frank Chang**, G. Chattopadhyay*, Z. Chen**, T. Reck*, H. Schone*, Y. Zhao**, L. Du**, D. Murphy**, N. Chahat*, E. Decrossas* and I. Mehdi*, *NASA Jet Propulsion Laboratory **University of California Los Angeles*

This paper discusses the applicability of CMOS (sub)-mm-Wave System-on-Chips in space exploration of the solar system, especially planetary missions.

Session 6 – Power Management pg. 158

Monday, 9/15, 1:30 pm
Fir Ballroom
Session Chair: William McIntyre, Texas Instruments
Session Co-chair: Olivier Trescases, University of Toronto

1:30 pm **Introduction**

Effective power management requires innovative techniques to minimize system cost while maximizing efficiency. This session covers a wide array of advances in power management spanning switched capacitor power converters, LED display drivers, and energy harvesting.

6-1 1:35 pm **A Unified Framework For Capacitive Series-Parallel DC-DC Converter Design (Invited)** **pg. 159**
Ramesh Harjani, Saurabh Chaubey, University of Minnesota-Twin Cities

This paper presents a design framework to select the best topology and conversion ratio of operation for series-parallel capacitive buck/boost DC-DC converters. The framework models all converter families providing design insights and tradeoffs among the various topologies. We select the 10 optimal topologies that always performs better than any of the 96 permutations that are possible for series-parallel converters. A logical extension of the framework includes the impact of parasitics and other second order effects including partial charging of bucket capacitors and finite tank capacitor size. The paper includes a step by step design methodology. Finally, we analyze a number of prior designs and one new design and show how they fit into our framework.

6-2 2:25 pm **A 45-Ratio Recursively Sliced Series-Parallel Switched-Capacitor DC-DC Converter Achieving 86% Efficiency** **pg. 167**
Loai G. Salem, Patrick P. Mercier, University of California, San Diego

A recursive ternary switched-capacitor topology is presented that achieves 45 distinct ratios by recursively slicing three-ratio series parallel converters in cascade or in parallel. A test chip fabricated in 0.25µm achieves 86% peak efficiency and an output voltage range of 0.1-2.24V.

6-3 2:50 pm **Conductance Modulation Techniques in Switched-Capacitor DC-DC Converter for Maximum-Efficiency Tracking and Ripple Mitigation in 22nm Tri-gate CMOS** **pg. 171**
Rinkle Jain, Stephen Kim, Vaibhav Vaidya, James Tschanz, Krishnan Ravichandran, Vivek De, Circuit Research Lab, Intel Corporation

Active conduction modulation techniques are demonstrated in MIM-based multi-ratio switched-capacitor voltage regulator in 22nm tri-gate CMOS. A switch-size control experimentally validated across dies/ temperatures maximizes light-load-efficiency. A simple gate modulation of select switches yields load-independent output-ripple. Measurements

show efficiency boosts up to 15%, ripple, EMI/RFI benefits and, ease-of-integration in SoCs.

3:15 pm **BREAK**

6-4 3:30 pm **High Power-Density, Hybrid Inductive/Capacitive Converter with Area Reuse for Multi-Domain DVS** pg. 175

Sudhir Kudva, Saurabh Chaubey, Ramesh Harjani, University of Minnesota

This paper presents a fully integrated hybrid inductive/ capacitive converter that supports 70X output power range while maintaining high efficiency. This high efficiency is achieved by using an inductive converter for larger loads and a capacitive converter for lower loads. We have also shown the feasibility of implementing digital circuits under the inductor increasing the peak converter power density from 0.387 W/sq-mm to 4.1 W/sq-mm with only a minor hit on the efficiency. The maximum measured efficiency decreases from 76.4% to 71% when the digital circuits under inductor are present. The design has been fabricated in IBM's 32nm SOI technology.

6-5 3:55 pm **Inverting Buck-Boost DC-DC Converter for Mobile AMOLED Display with Real-Time Self-Tuned Minimum Power-Loss Tracking Scheme** pg. 179

Sung-Wan Hong, Gyu-Hyeong Cho, Samsung Electronics DMC R&D Center, *KAIST*

Introducing a new minimum power loss tracking scheme which implements theoretical equations at the circuit level, a proposed inverting buck-boost converter has maximum power efficiency of 91% at typical condition. Besides, this work maintains maximum power efficiency of around 90% though I/O voltages are varied in those whole ranges. This chip is implemented in 0.35μm BCD process and occupies 2.1x1.4mm^2.

6-6 4:20 pm **An Analog Optimum Torque Control IC for a 200W Wind Energy Conversion System with Over 99% MPPT Accuracy, 1.7% THDi and 0.99 Power Factor** pg. 183

Peng-Chang Huang, Wen-Chuen Liu, Yi-Chen Liu, Yeong-Chau Kuo, Tai-Haur Kuo, National Cheng Kung University, *National Kaohsiung First University of Science and Technology*

An optimum torque control IC is implemented for harvesting the most available energy from and prolonging the lifetime of a wind turbine generator. This IC achieves over 99% maximum power point tracking accuracy, 96.1% power conversion efficiency, 0.99 power factor, and 1.7% current total harmonic distortion.

6-7 4:45pm **An Ultra-Low Power Power Management Unit with -40dB Switching-Noise-Suppression for a 3x3 Thermoelectric Generator Array with 57% Maximum End-to-End Efficiency** pg. 187

Jorge Zarate-Roldan, Salvador Carreon-Bautista, Alfredo Costilla-Reyes, Edgar Sanchez-Sinencio, Texas A&M University

A Power Management Unit consuming below 3μW for an energy harvesting system based on a TEG array. A boost converter with a cascaded LDO regulator comprises the proposed PMU. The unit reaches maximum power transfer by matching the TEG's series resistance and provides adaptive noise rejection.

6-8 5:10 pm **A 10mV-Input Boost Converter with Inductor Peak Current Control and Zero Detection for Thermoelectric Energy Harvesting** pg. 191

*A. Shrivastava, *David Wentzloff, B. H. Calhoun, University of Virginia, *Psikick Incorporated*

A boost converter for thermoelectric energy harvesting in 130nm CMOS reduces the achievable input voltage by 50% to 10mV, which allows wearable body sensors to continue operation with thermal gradients below 1°C. The design uses a peak inductor current control scheme and duty cycled, offset compensated comparators to maintain high efficiency across a broad range of input and output voltages. The measured efficiency ranges from 60% at VI=20mV to a peak efficiency of 83%.

Session 7 – Low Power Transceivers and Oscillators pg. 195

Monday, 9/15, 1:30 pm
Pine Ballroom
Session Chair: Fa (Foster) Dai, Auburn University
Session Co-chair: Byunghoo Jung, Purdue University

1:30 pm **Introduction**

This session presents papers on low-power transceivers for BAN and near range communications. Also included are papers on low-power quadrature oscillators and THz signal generators

7-1 1:35 pm **A 33uW/node Duty Cycle Controlled HBC Transceiver System for Medical BAN with 64 Sensor Nodes (Invited)** pg. 196
H. Lee, H.Cho, H.Yoo, KAIST

A Low power HBC system with duty cycle control (DCC) is implemented in 0.13μm CMOS technology for low energy medical BAN. It's network operation is optimized by a proposed MAC scheduler with DCC. Thanks to DCC, only 2.77mW with 38% average duty and 96.6% QoS is achieved for 64 nodes.

7-2 2:25 pm **An Energy Harvesting 2×2 60GHz Transceiver with Scalable Data Rate of 38-to-2450Mb/s for Near Range Communication** pg. 204
Mazhareddin Taghivand, Yashar Rajavi*, Kamal Aggarwal, and Ada S. Y. Poon, Stanford University, *Qualcomm Atheros*

An integrated 2×2 OOK transceiver at 60GHz with energy harvesting transmitter (TX) and TX power scalable with data rate is demonstrated. The TX power scales from 100μW to 6.3mW at 5cm range and from 260μW to 11.9mW at 10cm range, supporting 38-to-2450Mb/s with a BER<5×10-4. Energy is harvested at 2.45GHz with an average efficiency of 33%. It occupies 1.62mm^2 in 40nm CMOS and the TX energy efficiency is 4.9pJ/b and 2.6pJ/b at 10cm and 5cm respectively.

7-3 2:50 pm **A 52% Tuning Range QVCO With a Reduced Noise Coupling Scheme and a Minimum FOMT of 196dBc/Hz** pg.208
Mohammad Elbadry, Sachin Kalia, Ramesh Harjani, University of Minnesota

A wide-tuning range QVCO with a novel complimentary-coupling scheme is presented. Two NMOS-only VCOs are coupled through, the complimentary, PMOS injection transistors. This shifts the injection current away from the zero-crossings of the output voltage, thereby reducing the sensitivity of the VCO to injection noise, which results in significant phase-noise improvement.

3:15 pm **BREAK**

7-4 3:30 pm **A 350 mV, 5 GHz Class-D Enhanced Swing Quadrature VCO in 65 nm CMOS with 198.3 dBc/Hz FoM** **pg. 212**

Ankur Guha Roy, Siladitya Dey, Justin Goins, Kartikeya Mayaram, Terri S. Fiez, Oregon State University

A low voltage (350 mV) enhanced swing class-D quadrature VCO is presented. The prototype 5-GHz VCO was fabricated in a 65 nm CMOS process. The measured phase noise is -137.1 dBc/Hz at 3-MHz offset frequency. This VCO achieves the best FoM (198.3 dBc/Hz) to date at the lowest supply voltage.

7-5 3:55 pm **A Multi-Phase Sub-Harmonic Injection Locking Technique for Bandwidth Extension in Silicon-Based THz Signal Generation** **pg. 216**

Taiyun Chi, Jun Luo, Song Hu, Hua Wang, Georgia Tech, *Tsinghua University*

This paper presents a multi-phase sub-harmonic injection locking technique to significantly extend the locking range of a multi-phase injection locking oscillator (ILO). Leveraging this technique, a scalable and cascadable "active frequency multiplier" chain architecture is proposed, which achieves THz signal generation from a low mm-wave frequency tone. We also propose a multi-ring topology to facilitate the design and the high-frequency routing. As a proof-of-concept, a cascaded 3-stage 3-phase 2nd-order sub-harmonic ILO chain is implemented in a SiGe BiCMOS process. It achieves 504 GHz signal generation from a 42 GHz tone with a 4.4% frequency tuning range, which is the largest tuning range among all the reported Si-based THz harmonic oscillator sources at the 0.5 THz band.

Panel Discussion

Monday, September 15, 1:30 pm
Silicon Valley Room
Panel Title: Academia vs. Industry

Educational Sessions

Educational Session 2 - Miniaturized Energy-Harvesting Piezoelectric Chargers pgs. 220-238

Monday, September 15, 1:30 pm, Cedar Room
Speaker: Gabriel A. Rincón-Mora, Georgia Tech

Wireless microsensors and other miniaturized electronics cannot only monitor and better-manage power consumption in emerging small- and large-scale applications (for space, military, medical, agricultural, and consumer markets) but also add energy-saving and performance-enhancing intelligence to old, expensive, and difficult-to-replace infrastructures and tiny contraptions in difficult-to-reach places (like the human body). The energy these smart devices store, however, is often insufficient to power the functions they incorporate (such as telemetry, interface, processing, and others) for extended periods. Still more, replacing or recharging the batteries of hundreds of networked nodes is costly, and invasive in the case of the human body. Harvesting ambient kinetic energy in motion to continually replenish a battery is therefore an appealing alternative, even if relevant technologies are still the subject of research today. This talk discusses the state of the art in miniaturized piezoelectric chargers that draw kinetic energy from motion to charge a battery.

Educational Session 3 - High-Performance Analog/Mixed-Signal Characterization Techniques pgs. 239-266

Monday, September 15, 3:30 pm, Cedar Room
Doug Garrity, Freescale Semiconductor

Almost all electronic systems ranging from power metering to automotive radar require an analog-to-digital converter (ADC) of some sort and it turns out that the better the performance of the ADC, the better (and more easy to implement) the system becomes. However, as ADC performance improves, ADC performance becomes significantly more difficult and more expensive to test and unless proper techniques and extreme attention to detail are carefully applied, the true performance of an ADC will be nearly impossible to determine. Using a 24-bit Analog Front End (AFE) as a demonstration vehicle, this tutorial will present best practices (from a test/characterization perspective) for IC design, basic lab set up and equipment, evaluation boards, and data analysis along with measured results and an extensive list of lessons learned.

Monday Poster Session

Monday, September 15, 5:00 pm – 7:00 pm
Donner, Siskyou, Cascade Ballroom

M-01 **A Robust Parasitic-Insensitive Successive Approximation Capacitance-to-Digital Converter** **pg. 267**
Hesham Omran, Muhammad Arsalan, Khaled N. Salama, King Abdullah University of Science and Technology (KAUST)

We present a capacitive sensor interface circuit using true capacitance-domain successive approximation that is independent of supply voltage. The interface circuit is insensitive to parasitic capacitances, offset voltages, and charge injection, and is not prone to noise coupling. The design achieves very low temperature sensitivity of 25ppm/oC and digitizes a wide capacitance range of 16pF with 12.5-bit resolution in a compact area of 0.07mm^2.

M-02 **Configurable Incremental Sigma-Delta ADC for DC Measure and Audio Conversion** **pg. 271**
Zhengyu Wang, Tay(Hui) Zheng, Dongtian Lu, Sasi Kumar, Xicheng Jiang, Broadcom Corporation

A configurable three-level sigma-delta ADC for both DC measurement and audio conversion is implemented. Dynamic Element Matching (DEM)is avoided. Three-level quantizer uses only one set of summer/comparator to save power and area. A simple formula accurately predicts DC measurement noise is presented. The ADC achieves 83dB SNR for audio, and 11-bit for DC measurements, at power of 0.5mW.

M-03 **A Hybrid SAR-VCO ΔΣ ADC with First-Order Noise Shaping** **pg. 275**
A. Sanyal, K. Ragab, L. Chen, T. R. Viswanathan, S. Yan, N. Sun, The University of Texas at Austin, *Silicon Labs*

A scaling-friendly, hybrid, two-stage ADC with a 5-bit SAR as first stage and a VCO as second stage is presented in this work. Since the VCO can provide fine quantization for small signals in the time-domain, it is used to directly quantize the SAR residue without OTA-based residue amplification. Also, having a small input swing obviates the need for VCO non-linearity calibration. The VCO phase overflow problem is solved by using a counter to record the number of overflows, thus allowing a variable sampling rate. Since the VCO phase and counter are never reset, the VCO's first-order noise-shaping capability is retained. A prototype ADC in an 180 nm process achieves 73 dB SNDR over 2.2 MHz bandwidth and consumes 5mW from a 1.8V supply while sampling at 35 MHz.

M-04 **A 0.45mW 12b 12.5MS/s SAR ADC with Digital Calibration pg. 279**
W. Li, T Wang, J. A. Grilo**, G. C. Temes, Oregon State University, *Broadcom, **MaxLinear*

This paper presents a 12-bit 12.5-MS/s SAR ADC in 40 nm technology. A power saving strategy is proposed. Also, several foreground calibration methods are proposed to reduce the power dissipation and enhance the conversion accuracy. Measurement results showed a SFDR of 87.5 dB and a THD improvement of 24.3 dB.

M-05 **A Voltage-Scalable 10-b Pipelined ADC with Current-Mode Amplifier pg. 283**
Y. Suh, S. Choi, B. Kim, H.-J. Park, J.-Y. Sim, Pohang University of Science and Technology (POSTECH), *Samsung Electronics*

This paper presents an energy-efficient 10-b pipelined ADC with a current-mode amplifier. The proposed amplifier achieves high gain, low static power consumption and supply voltage scalability without any calibration or timing control. The fabricated ADC in 65-nm CMOS process achieves FOMs of 14.3-to-36.9 fJ/c-s with a supply voltage range from 0.6-V to 1.0-V.

M-06 **A Supply-Scalable Differential Amplifier With Pulse-Controlled Common-Mode Feedback pg. 287**
Chun-Wei Hsu, Peter R. Kinget, Columbia University

This paper describes a 0.6V-1.2V fully-differential amplifier with a pulse-controlled CMFB. The pulse-controlled CMFB provides a low-cost solution for supply-scalable operation. The amplifier prototype in a 65nm low power/leakage CMOS process has an active area of $0.01mm^2$ and a power consumption of 1.21mW at 0.6V and 3.07mW at 1.2V.

M-07 **Low drain voltage S/H type PWM LED current driver for BLU in mobile LCD pg. 291**
Changbyung Park, Tae-Hwang Kong, Gyu-Hyeong Cho, KAIST

A pulse-width-modulation light emission diode (LED) current driver for Back Light Unit in mobile liquid crystal display with minimum operable drain voltage of 360mV and 3σ current accuracy of 3% without trimming is proposed in 0.35μm BCD process. S/H type structure with sequential channel driving scheme reduces power consumption as reference current of current mirror with accurate output current. High reference current is just applied for the enhanced matching in sampling phase, while reference current is minimized in holding phase. The proposed triggered buffer amplifier enables fast and accurate PWM current driving.

M-08 **A 1.6nJ/bit, 19.9μA Peak Current Fully Integrated $2.5mm^2$ Inductive Transceiver for Volume-Constraned Microsystems pg. 295**
M. H. Ghaed, S. Skrzyniarz, D. Blaauw, D. Sylvester, University of Michigan

A 1.6nJ/bit inductive transceiver targeting volume-constrained systems is presented. The transceiver uses a protocol in which the external unit sends the same packet multiple times to move the power consumption burden to the external TRX unit and relaxes the jitter requirements on the mm-scale receiver. The $2.5mm^2$ transceiver draws 19.9μA at 40.7kbps.

M-09 **A Fully Integrated Electroencephalogram (EEG) Analog Front-End IC with Capacitive Input Impedance Boosting Loop pg. 299**
Seunghyun Lim, Changho Seok, Hyunho Kim, Haryong Song, and Hyoungho Ko, Chungnam National University

A biopotential chopper stabilized AFE IC for electroencephalogram is presented. The proposed capacitive input impedance boosting loop (CIIBL) forms a positive feedback loop without additional power consumption, increases the input impedance from 644 MΩ to 3.5 GΩ, and enhances the CMRR from 133.4 dB to 139.1 dB.

M-10 **A 27μW subcutaneous single-chip wireless biosensing platform with optical power and data transfer** **pg. 303**

Kannan Sankaragomathi, Luis Perez, Ramin Mirjalili, Babak Parviz, Brian Otis, University of Washington, Seattle

We present a batteryless, 27μW barely subcutaneous sensing platform using optical power and data links. We demonstrate an 8.1 mm x 3.2 mm implantable tag powered by an 850nm infrared source through the skin barrier. Measurements using pig skin indicate that optical power transfer through skin achieves a 4.9% efficiency, which is higher than mm scale inductive power links. As a proof-of-concept demo, we sense and transmit temperature to an external body worn reader using a fully optical power and data link.

M-11 **3D Multi-Gesture Sensing System for Large Areas based on Pixel Self-Capacitance Readout using TFT Scanning and Frequency-Conversion Circuits** **pg. 307**

Y. Hu, T. Moy, L. Huang, W. Rieutort-Louis, J. Sanz Robinson, S. Wagner, J. C. Sturm, N. Verma, Princeton University

A flexible gesture-sensing sheet for interactive spaces achieves sensing to 16cm, with multi-gesture support enabled by array (4x4) of pixels. For pixel scalability, TFT oscillators perform capacitance-to-frequency conversion and inductive coupling to a readout IC. 22dB SNR is achieved at 10cm with 240Hz scan rate and power of 26mW.

M-12 **A 0.4 V 75 kbit SRAM Macro in 28 nm CMOS Featuring a 3-Adjacent MBU Correcting ECC** **pg. 311**

A. Neale, M. Sachdev, University of Waterloo

A 0.4V, 75-kbit SRAM macro protected with a MBU correcting ECC is fabricated in a 28nm LP-CMOS process. Simulations show the code provides up to 2.35x corrected-SER improvement over a BCH DEC code for 3 fewer check-bits. Measurements confirm an average active energy of 0.015fJ/bit and leakage current of 10.1pA/bit.

M-13 **Independent N and P Process Monitors for Body Bias Based Process Corner Correction** **pg. 315**

Lawrence T. Clark, David Kidd, Vineet Agrawal, Sam Leshner, Gokul Krishnan, SuVolta Inc.

Independent N and P Process Monitors for Body Bias Based Process Corner Correction are presented. Performance and Power correction is demonstrated for digital and SRAM circuits. Ring oscillators and CPUs demonstrate 71% reduction in in worst case leakage. SRAM read current variability and leakage are reduced by 55% and 72%.

M-14 **A Tri-Stack Buck Converter with Gate Coupling Control (GCC) and Quasi Adaptive Dead Time Control (QADTC)** **pg. 319**

J-.H. Choi, S-.H. Park, G.H. Cho, KAIST

A DC-DC buck converter handling three times the nomal transistors' nominal voltage is implemented with 1.8V I/O devices in a 65nm digital process with the aim of creating an analog intellectual property that is robust, easily reconfigurable and cost effective. Moreover,

the maximum current density and the efficiency of the powering block reach to 1.28A/mm^2 and 93.8%, respectively, with the help of the high mobility of the transistor.

M-15 **A Fully-Integrated, 90% Peak-Efficiency, 0.99 Power Factor, AC-DC LED Driver with On-Chip Direct-AC Connect Series Startup Pre-regulator** **pg. 323**

Percy Neyra, Mohammad Al-Shyoukh, TSMC

In this paper, a fully-integrated AC-DC flyback converter for LED lighting applications is demonstrated. With the exception of passives, magnetics and rectification diodes, the entire AC-DC power converter including the ultra high voltage (UHV) power FET, control loop, current sensing, and startup functions have been integrated on the same monolithic bulk-CMOS silicon die. The startup function employs an 800V depletion-mode pass device as part of a direct-AC connect self- biased series pre-regulator. The entire AC-DC converter occupies an active area of 12.7mm^2 on silicon, and has a peak efficiency of 90% for a 15W LED load. A control loop architecture employing critical conduction mode (CrM) with line voltage feed-forward enables near-unity power factor performance.

M-16 **A 3.15pJ/cyc 32-bit RISC CPU with Timing-Error Prevention and Adaptive Clocking in 28nm CMOS** **pg. 327**

M. Hiienkari, J. Teittinen, L. Koskinen, M. Turnquist, M. Kaltiokallio*, J. Mäkipää**, A. Rantala**, M. Sopanen**, University of Turku, *Aalto University, **VTT Technical Research Centre of Finland*

This paper presents an ASIC implementation of a 32-bit RISC CPU in 28nm CMOS employing timing-error prevention with clock stretching. Measurements show 1.67pJ/cyc energy consumption at 400mV, which corresponds to 40% energy savings and 84% EDP reduction compared to operation based on static signoff timing.

M-17 **A Coprocessor for Clock-Mapping-Based Nearest Euclidean Distance Search with Feature Vector Dimension Adaptability** **pg. 331**

Fengwei An, Toshinobu Akazawa, Shogo Yamazaki, Lei Chen, Hans Juergen Mattausch, Hiroshima University

A coprocessor fabricated in 180nm for word-parallel nearest-Euclidean-distance search is developed using a distance-clock-mapping concept. The test chip, for parallel search among 32 references achieves low power dissipation of 5.02 mW at 42.9MHz clock frequency and 1.8 V supply voltage. Applications with up to 2048-dimensional vectors can be handled.

M-18 **An Efficiency-Enhanced 2.4GHz Stacked CMOS Power Amplifier with Mode Switching Scheme for WLAN Applications** **pg. 335**

Yun Yin, Baoyong Chi, Xiaobao Yu, Wen Jia, Zhihua Wang, Tsinghua University, *Research Institute of Tsinghua University in Shenzhen*

This work proposes an efficiency-enhanced CMOS PA with mode switching scheme for 2.4GHz WLAN applications, which not only improves the efficiency at high back-off power but also achieves the high output power by means of transistor stacking and self-biasing techniques, while needing the minimum area overhead for low-cost WLAN-enabled terminals.

M-19 **A Capacitive-Coupling Technique with Phase Noise and Phase Error Reduction for Multi-Phase Clock Generation** **pg. 339**

Feng Zhao, Fa Foster Dai, Department of Electrical and Computer Eng., Auburn University

This paper presents a capacitive-coupling technique for multi-phase oscillators. The proposed capacitive coupling techniques can improve the phase noise performance while maintain good phase accuracy over wide frequency range for multi-phase oscillators. A prototype two-phase VCO is analyzed using injection-locking theory and implemented to demonstrate the effectiveness of the capacitive-coupling technique for low-power and low-noise multiple phase clock generation. The 4.3-5.3 GHz two-phase VCO prototype was implemented in a 130nm CMOS technology and achieved a measured phase noise of -120 to -124.04dBc /Hz @ 1MHz offset and a measured phase error of 0.23-0.91° across the 1GHz tuning range.

M-20 **A 127-140GHz Injection-locked Signal Source with 3.5mW Peak Output Power by Zero-phase Coupled Oscillator Network in 65nm CMOS** **pg. 343**
Yang Shang, Hao Yu, Peng Li, Xiaojun Bi, Minkyu Je*, Nanyang Technological University, *Institute of Microelectronics (A-STAR)*

A high output-power and high-efficiency injection-locked millimeter-wave signal source is demonstrated by zero-phase coupled-oscillator-network in CMOS-65nm process. The proposed source has a compact core chip area of 0.13mm^2, and it is measured with 3.5mW peak output power, 9.7% frequency-tuning-range centered at 133.5GHz, 2.4% power efficiency and 26.9mW/mm^2 power density.

M-21 **A 0.4-V, 500-MHz, ultra-low-power phase-locked loop for near-threshold voltage operation** **pg. 347**
Joung-Wook Moon, Sung-Geun Kim, Dae-Hyun Kwon, Woo-Young Choi, Yonsei University

We present a 500-MHz, ultra-low-power PLL realized with 0.4-V supply in 65-nm CMOS technology. Our PLL employs a new charge pump circuit structure that can greatly reduce up/down current mismatch and their variation with VCO control voltages. The PLL consumes only 127.8 μW, corresponding power efficiency of 0.256 mW/GHz.

M-22 **A 75mW 50Gbps SerDes Transmitter with Automatic Serializing Time Window Search in 65nm CMOS technology** **pg. 351**
Ke Huang, Ziqiang Wang, Xuqiang Zheng, Chun Zhang, Zhihua Wang, Tsinghua University

This paper presents a 50Gbps SerDes transmitter with automatic serializing time window search. The serializing timing is guaranteed and circuits running at highest speed such as latches for retiming and clock tree buffers for delay matching are eliminated.The transmitter running at 50Gbps consumes only 75mW power under 1.2V.

M-23 **A Blind ADC-Based CDR with Digital Data Interpolation and Adaptive CTLE and DFE** **pg. 355**
C. Ting, M. S. Jalali, A. Sheikholeslami, M. Kibune, H. Tamura*, University of Toronto, *Fujitsu Laboratories Limited*

This paper proposes replacing the analog phase interpolator in a phase-tracking ADC-based receiver with a digital data interpolator following the ADC. This allows for a blind ADC-based receiver that has a simpler adaptive DFE implementation. Our measurements from a 65nm CMOS testchip confirm 7Gb/s operation for a 17dB channel loss.

Session 8 – Amplifiers and Filters pg. 359

Tuesday, 9/16, 9:00 am
Oak Ballroom
Session Chair: Eric Naviasky, Cadence

Session Co-chair: Ken Suyama, Epoch Microelectronics

9:00 am **Introduction**

This session has 3 papers on advances in Class D amplifier design for high performance audio applications. There will also be two papers on high frequency amplifiers for base-band application, a new technique for increasing stage gain in advanced low voltage processes, and a high performance programmable active filter.

8-1 **A 85-225MHz Chebyshev-II Active-RC BPF with Programmable BW and CF** **pg. 360**
9:05 am **Achieving Over 30dBm IIP3 in 40nm CMOS**
B. Wu, Y. Chiu, University of Texas at Dallas

A zero-capacitance-spread 8th-order Chebyshev-II active-RC BPF that enables integrator frequency compensation is reported. With op-amps employing split-path feed-forward compensation, significant power savings is achieved in a 40nm CMOS prototype that measures a center frequency of 85-225MHz and programmable bandwidth-to-center frequency ratios of 5%-40% with a peak in-band IIP3 of 31dBm.

8-2 **A High Gain Operational Amplifier via an Efficient Conductance Cancellation** **pg. 364**
9:30 am **Technique**
Bin Huang† and Degang Chen*, *Iowa State University, †Maxim Integrated*

An efficient conductance cancellation method is introduced to achieve high gain operational amplifiers.The measurement results show that the proposed technique maintains at least 26.4dB DC gain enhancement under output voltage swing between 0.1V and 1.4V, while power consumption and area overhead are respectively less than 2% and 3%.

8-3 **High Linearity PVT Tolerant 100MS/s Rail-to-Rail ADC Driver With Built-in Sampler** **pg. 368**
9:55 am **in 65nm CMOS**
Rakesh Kumar Palani, Ramesh Harjani, University of Minnesota

A novel completely inverter-based ADC driver is proposed that relaxes the gain and unity gain bandwidth requirements of the negative feedback loop by making it not see the closed loop gain. This ADC driver has a built-in first order anti alias filter and uses a passive amplifier to provide a rail-to-rail (2Vpp diff) sampled output signal. This design exploits the linearity of current mirrors and achieves 65dB of linearity at the Nyquist rate for a rail-to-rail output. A semi-constant current biasing circuit for inverters has been proposed to minimizing PVT variations in lower technologies. As a proof of concept an ADC driver is designed and implemented in TSMC's 65nm GP CMOS technology. The measured design operates at 100MS/s and has an OIP3 of 40dBm at the Nyquist rate, provides a gain of 8, and samples the signal onto a 1pF output capacitance while drawing 2mA from a 1V supply.

8-4 **A 1.2V 110-MHz-UGB Differential Class-AB Amplifier in 65nm CMOS** **pg. 372**
10:20 am *Akshay Visweswaran, John R. Long, R. Bogdan Staszewski, Delft University of Technology*

A wideband, fully differential, 3-stage class-AB amplifier capable of operation at rates beyond 100 Mbps is described. Common-mode feedback is applied to increase output drive capability and reduce bias-dependent crossover distortion when operating in class-AB from a low supply voltage. Drawing 3.9mA from a nominal VDD of 1.2V in 65nm CMOS, the 0.052mm^2 amplifier delivers 1.6V swing across a 50Ω load with THD+N of 82.6dB in the unity-gain configuration.

10:45 am **BREAK**

8-5 **A Stereo 110 dB Multi-rate Audio ΔΣ DAC with Class-G Headphone Driver pg. 376**
11:05 am *Min Gyu Kim, Dongtian Lu, Todd Brooks, Young Ju Kim, Vinay Chandrasekhar, Dale Stubbs, Steven Maughan, Bartomeu Servera Mas, David Yu, Broadcom Corporation*

A multi-rate, multibit ΔΣ audio DAC is proposed to overcome THD+N limitations due to out-of-band noise, clock jitter, and DAC latch error. The DAC, combined with a Class-G headphone driver and pop/click noise suppression, achieves 110 dB dynamic range and 4.03 mW/channel. Measured pop-and-click noise is 155 μV.

8-6 **An Open-Loop Class-D Audio Amplifier with Increased Low-Distortion Output Power pg. 380**
11:30 am **and PVT-Insensitive EMI Reduction**
S.-H. Chien, L.-T. Wu, S.-Y. Chen*, R.-D. Jan*, M-Y Shih*, C.-T. Lin*, T.-H. Kuo, National Cheng Kung University, *NeoEnergy Microelectronics, Inc.*

This work implements a class-D audio amplifier with the proposed adaptive-coefficient delta-sigma modulator (ACDSM) and low-EMI control method. The ACDSM simultaneously achieves a wide stable input range and high in-band noise suppression, resulting in a 20% increase of low-distortion output power. Moreover, the low-EMI control method eases the PVT-sensitive issues.

8-7 **A 105dBA SNR, 0.0031% THD+N Filter-less Class-D Amplifier with Discrete Time pg. 384**
11:55 am **Feedback Control in 55nm CMOS**
M. Kinyua, R. Wang, E. Soenen, TSMC Technology Inc.

It is traditionally difficult to implement higher order PWM closed loop class-D amplifiers using analog techniques. This paper describes a mixed signal approach, implementing a 4th order amplifier in 55nm CMOS. It achieves 105dBA SNR, 0.0031% THD+N, 92dB PSRR and 85% efficiency when supplying 1W.

Session 9 – Implantable Systems N/A

Tuesday, 9/16, 9:00 am
Fir Ballroom
Session Chair: Christophe Antoine, Analog Devices
Session Co-chair: Emmanuel Quevy, Silicon Laboratories

9:00 am **Introduction**

This session is focused on implantable biomedical systems as they hold strong promises for continuous monitoring, as well as diagnostic and treatment of defective body or brain functions.

9-1 **Circuit Techniques for Miniaturized Biomedical Sensors (Invited) pg. 388**
9:05 am *I. Lee, Y. Kim, S. Bang, G. Kim, H. Ha*, Y.-P. Chen, D. Jeon, S. Jeong, W. Jung, M. Ghaed, Z. Foo, Y. Lee, J.-Y. Sim*, D. Sylvester, D. Blaauw, University of Michigan, *Pohang University of Science and Technology*

Miniaturized biomedical sensors promise improved quality of medical diagnosis and treatment. However, the realization of such implantable devices faces challenges due to limited battery capacity and energy sources. This paper describes new circuit techniques for miniaturized biomedical sensors, with particular focus on bio-signals sensing front end, power

management, and communication.

9-2 9:55 am **A mm-Sized Implantable Device with Ultrasonic Energy Transfer and RF Data Uplink for High-Power Applications pg. 395**
J. Charthad, M. J. Weber, T. C. Chang, M. Saadat, A. Arbabian, Stanford University

We present a first proof-of-concept mm-sized implant based on ultrasonic power transfer and RF data uplink for high power applications. The implant supports a DC load power of 100 µW. It also transmits consecutive UWB pulses activated by an ultrasonic downlink, demonstrating sufficient power for a PPM transmitter in uplink.

9-3 10:20 am **A Multiple-Output Fixed Current Stimulation ASIC for Peripherally-Implantable Neurostimulation System pg. 399**
E. Lee, E. Matei, V. Giang, J. Shi, A. Zadeh, Alfred Mann Foundation

A multiple-output stimulation ASIC for a peripherally-implantable neurostimulation system was implemented in a 0.18µm CMOS process. The numbers of anodic outputs (NEA) and cathodic outputs (NEC) can be set between 1 and 8 with a fixed total output current up to 32.6mA, independent of NEA and NEC. Fast turn on technique was proposed for the stimulator design to achieve a settling time of <5.8µs. The ASIC includes a power management unit and an electrode monitoring circuit, which consists of a 10-b ADC for monitoring the high voltage (>15V) stimulator outputs.

10:45 am **BREAK**

Session 10– Wireline Transceivers pg. 403

Tuesday, 9/16, 9:00 am
Pine Ballroom
Session Chair: Azita Emami, Caltech
Session Co-chair: Kimo Tam, Analog Devices

9:00 am **Introduction**

This session presents various wireline transceivers including powerline communication, short reach links and Ethernet

10-1 9:05am **A 8.125-15.625 Gb/s SerDes Using a Sub-Sampling Ring-Oscillator Phase-Locked Loop pg. 404**
Socrates D. Vamvakos, Charles Boecker, Eric Groen , Alvin Wang, Shaishav Desai, Scott Irwin, Vithal Rao, Aldo Bottelli, Jawji Chen, Xiaole Chen, Prashant Choudhary, Kuo-Chiang Hsieh, Paul Jennings, Haidang Lin, Dan Pechiu, Chethan Rao, Jason Yeung, MoSys Inc.

The paper describes a 8.125-15.625Gbps SerDes, which employs a sub-sampling ring-oscillator PLL to obtain large frequency range with low-jitter. The transmitter uses a modified hybrid output driver and a multi-step duty-cycle corrector. The receiver uses BER-based calibration to optimize receiver voltage margin. The transmitter achieves 160fs RMS jitter at 15.625Gbps.

10-2 9:30 am **Wideband Flexible-Reach Techniques for a 0.5-16.3Gb/s Fully-Adaptive Transceiver in 20nm CMOS pg. 408**
Jafar Savoj, Hesam Aslanzadeh, Declan Carey, Marc Erett*, Wayne Fang, Yohan Frans,*

*Kenny Hsieh, Jay Im, Anup Jose, Didem Turker, Parag Upadhyaya, Daniel Wu, Ken Chang, Xilinx, Inc.., *Xilinx Ireland*

This paper describes the design techniques to achieve wideband flexible-reach operation in a fully-adaptive transceiver embedded in a 20nm CMOS FPGA. The receiver utilizes a bandwidth adjustable CTLE for programmable operation over both short-reach and long-reach channels. A modified 11-tap, 1-bit speculative DFE topology provides reliable operation across all data rates. The LC PLL feedback divider uses a synchronized CMOS down-counter without a prescaler to achieve a continuous divide ratio of 16-257. The transceiver achieves BER < 10^-15 over a 28dB loss backplane at 16.3Gb/s and over legacy channels with 10G-KR characteristics at 10.3125Gb/s. The transceiver meets jitter tolerance specifications for both PCIe Gen3 at 8Gb/s and PCIe Gen4 at 16Gb/s in both common-clock and spread-spectrum modes.

10-3
9:55 am **Design Considerations for Low-Power Analog Front Ends in Full-Duplex 10GBASE-T Transceivers (Invited) pg. 412**

J.R. Westra, J. Mulder, Y. Ke, D. Vecchi, X. Liu, E. Arslan, J. Wan, Q. Zhang, S. Wang, F. van der Goes, K. Bult, Broadcom Netherlands

The speed of Ethernet over copper cables has steadily increased by a factor of 10,000 over the last four decades, from 1Mb/s in the earliest Ethernet implementations to 10Gb/s in recent systems. This paper describes the design considerations on all levels of the 10GBASE-T design hierarchy that form the basis for the implementation of highly power-efficient AFEs in full-duplex 10GBASE-T transceivers. It also shows how these considerations are implemented in a practical design. At frequencies up to 400MHz, the transceiver presented in this paper achieves >62dBc transmitter SFDR, >62dBc echo cancellation (EC) SFDR and >60dB receiver SFDR. Achieving a bit-error-rate (BER) better than 10^{-15}, it dissipates less than 1.75W at full 10Gb/s traffic over a 100m cable, which is the lowest power for a 10GBASE-T AFE published to date.

10:45 am **BREAK**

10-4
11:05am **A HomePlugAV SoC in 40nm CMOS Technology (Invited) pg. 420**

K. Findlater, A. Bofill, X. Reves, J. Abad, Broadcom

A cost-optimized 40nm CMOS integrated powerline communications SoC is presented. This SoC includes all the analog and digital components required for the HomePlugAV standard. Circuit techniques for the RXPGA and TX line driver are described. The powerline SoC can achieve full HPAV 200Mbps PHY rate and operates with a 96dB channel dynamic range with low external component cost.

10-5 11:55 am **A 1.4-pJ/b, Power-Scalable 16x12-Gb/s Source-Synchronous I/O with DFE Receiver in 32nm SOI CMOS Technology** pg. 428

Timothy O. Dickson, Yong Liu, Sergey V. Rylov, Ankur Agrawal, Seongwon Kim, Ping-Hsuan Hsieh, John F. Bulzacchelli, Mark Ferriss, Herschel Ainspan, Alexander Rylyakov, Benjamin D. Parker, Christian Baks, Lei Shan, Young Kwark, Jose Tierno**, Daniel J. Friedman, IBM T.J. Watson Research Center, *now with National Tsing Hua University, **now with Apple*

A power-scalable 16x12-Gb/s I/O is reported in 32nm SOI CMOS. The I/O includes adjustable driver amplitude, RX equalization, and deskew modes, enabling support for a wide range of channels with varying power efficiency. Test chip measurements demonstrate 1.4-pJ/b efficiency over 0.75" Megtron-6 PCB traces, and 1.9-pJ/b efficiency over 20" traces.

Session 11– Embedded Tutorial: Test and Manufacturability for Silicon Photonics and 3D Integration pg. 432

Tuesday, 9/16, 9:00 am
Cedar Ballroom
Session Chair: Manoj Sachdev, University of Waterloo
Session Co-chair: Tetsuya Iizuka, University of Tokyo

9:00 am **Introduction**

Test and manufacturability challenges in Si-photonics and 3D integration are addressed. The first two papers explain Si-photonics for high-speed and high-performance interconnects. The last paper introduces 3D integration using inductive-coupling interface.

11-1 9:05 am **Hybrid Silicon Photonics Technology Platform for High Performance Optical Interconnect** N/A.

Peter De Dobbelaere, Luxtera Inc.

We will cover the various aspects of our silicon photonics technology platforms, including: wafer processing, photonic device library, design environment and automated test. Our approaches for electronic circuit and light source integration will be addressed. Finally, we will highlight some applications and potential roadmaps for further enhancement of our technology platform.

11-2 9:55 am **Photonic Integration in Data Communications** N/A

Odile Liboiron-Ladouceur, McGill University

In this tutorial, advancements in silicon photonic integrated circuits will be presented. Through integration, the transceivers can now reside in close proximity to CMOS circuits leading to enhanced off-chip throughput and increased bandwidth density. The integration of several photonic functions such as, modulation, detection, and interconnect, onto a single chip also provides new means to integrate optical switching in modern computing systems. Recent development in the field of Silicon Photonics and different experimental demonstrations will be discussed.

11-3 10:45 am **3D Integration by Inductive Coupling** N/A

Tadahiro Kuroda, Keio University

In this tutorial, inductive-coupling ThruChip Interface (TCI) will be presented. TCI is a digital CMOS circuit solution in a standard CMOS technology. It is cheaper than TSV but bears comparison in performance. Reliability will be covered as well as circuits and applications.

Test and manufacturability will be discussed for heterogeneous integration by multiple makers. Cost performance will be studied in the case of DRAM/SoC interface at 44GB/s. Scaling scenario and future direction will be described.

Forum 1 - Emerging Device/Material Technologies N/A

Tuesday, September 16, 9:00 am
Silicon Valley Room

Session 12– Biosystems at Gigahertz pg. 433

Tuesday, 9/16, 11:00 am
Fir Ballroom
Session Chair: Ed Lee, Alfred Mann Foundation
Session Co-chair: Mourad El Gamal, McGill University and Debbie Senesky, Stanford University

11:00 am **Introduction**

This session showcases the designs and applications of Gigahertz circuits in bio-systems, both in sensing interfaces and in wireless transmission.

12-1 11:05 am **A 0.18-µm CMOS Fully Integrated 0.7-6 GHz PLL-Based Complex Dielectric Spectroscopy System** pg. 434
Osama Elhadidy, Sherif Shakib, Keith Krenek, Samuel Palermo, and Kamran Entesari, Texas A&M University

A fully-integrated sensing system utilizes a ring oscillator-based phase locked loop (PLL) for wideband complex dielectric spectroscopy of materials under test (MUT). Characterization of both real and imaginary MUT permittivity is achieved with frequency-shift measurements between a sensing oscillator, with a frequency that varies with MUT-induced changes in capacitance and conductance of a delay-cell load, and an amplitude-locked loop (ALL)-controlled MUT-insensitive reference oscillator. Fabricated in 0.18-µm CMOS, the 0.7-6 GHz spectroscopy system occupies 6.25 mm^2 area and achieves 3.7% maximum permittivity error.

12-2 11:30 am **Matching the power density and potentials of biological systems: a 3.1-nW, 130-mV, 0.023-mm3 pulsed 33-GHz radio transmitter in 32-nm SOI CMOS** pg. 438
J. B. Choi, E. Aklimi, J. Roseman, D. Tsai, H. Krishnaswamy, K. L. Shepard, Columbia University

A 3.1nJ/bit pulsed millimeter-wave transmitter 300µm-by-300µm-by-250-µm in size operates on 130mV-voltage and 3.1nW-power, comparable to those present across cellular membranes. A link budget analysis dictates an optimal frequency of 33GHz for ultra-low-power communication. A 1-Hz signal is obtained by supply-switching an on-chip millimeter-wave LC-oscillator with a duty cycle of 1e-6.

12-3 11:55 am **A 239-281GHz Sub-THz Imager with 100MHz Resolution by CMOS Direct-conversion Receiver with On-chip Circular-polarized SIW Antenna** pg. 442
Yang Shang, Hao Yu, Chang Yang, Yuan Liang, Wei Meng Lim, Nanyang Technological University

A 239-281GHz imager by direct-conversion receiver is demonstrated in CMOS 65nm process with high spectrum resolution and high sensitivity for frequency-dependent sub-THz

biomedical imaging. The proposed direct-conversion receiver is measured with -2dBi conversion gain over 42GHz bandwidth, -54.4dBm sensitivity with 100MHz detection resolution bandwidth, 6.6mW power consumption and 0.99mm2 chip area.

Luncheon Keynote N/A

Tuesday, 9/16, 12:20 pm – 1:50 pm
Sierra Ballroom
Tickets for the luncheon are for sale at the Registration Desk

The Troubled Birth of Electrical Engineering: Lessons Learned from the First Transatlantic Telegraph Cable

Tom Lee, Stanford University

Electrical engineers are the children of a failure so vast and traumatic that we scarcely even talk about it. The first transatlantic telegraph cable was mainly designed by a medical doctor, with results one would expect on that basis. A British board of inquiry convened to assess the multiple failures noted that the electrical arts lacked even a basic vocabulary to describe the failure. William Thomson was named the new head of the project, and success followed in 1866. The volt, ohm and ampere were defined shortly thereafter and the profession of electrical engineering was born. Thomson, of course, became Lord Kelvin, and was arguably the first professional electrical engineer. This talk describes the heroic efforts required to span the 3,000km distance without any amplifiers of any kind.

Session 13 – Data Converter Techniques pg. 446

Tuesday, 9/16, 2:00 pm
Oak Ballroom
Session Chair: Jorge Grilo, Maxlinear
Session Co-chair: Xicheng Jiang, Broadcom

2:00 pm **Introduction**

This session presents seven papers covering advanced data converter techniques, from continuous-time delta-sigma modulators to VCO-based and SAR converters

13-1
2:05 pm **Advances in High-Speed Continuous-Time Delta-Sigma Modulators (Invited) pg. 447**
T. Caldwell, D. Alldred, R. Schreier, H. Shibata, Y. Dong, Analog Devices

The maximum clock rate of continuous-time delta-sigma modulators has increased dramatically over the past several years, showing that continuous-time systems can operate at higher rates than their discrete-time counterparts. This paper outlines the circuits and architectures that have led to these improvements, and presents an analysis of the maximum clock rate of continuous-time delta-sigma modulators when limited by the metastability error of the internal flash ADC. A circuit simulation technique is also presented that helps analyse high-speed continuous-time systems to identify and correct non-idealities in the modulator's transfer functions.

13-2
2:55 pm **A 11μW 250 Hz BW Two-Step Incremental ADC with 100 dB DR and 91 dB SNDR for Integrated Sensor Interfaces pg. 455**
Chia-Hung Chen, Yi Zhang, Tao He*, Patrick Y. Chiang**, Gabor C. Temes*, Mediatek USA, *Oregon State University*

A two-step incremental ADC (IADC) is proposed for low-bandwidth, micro-power sensor interface circuits. This architecture extends the order of a conventional IADC from N to (2N-1) by using a two-step operation, while requiring only the circuitry of an Nth-order IADC. The implemented third-order IADC achieves a measured dynamic range of 99.8 dB and an SNDR of 91 dB for a maximum input 2.2 VPP and 250 Hz bandwidth. Fabricated in 65 nm CMOS, the IADC's core area is 0.2 mm^2, and consumes only 10.7 µW. The FoMs are 0.76 pJ/conversion-step and 173.5 dB, both among the best reported results.

13-3
3:20 pm **An All Digital PWM-Based Delta Sigma ADC with an Inherently Matched Multi-Bit Quantizer/DAC pg. 459**

Wooyoung Jung, Yousof Mortazavi, Brian L. Evans, Arjang Hassibi, The University of Texas at Austin

A PWM-based 1st order 3-bit continuous-time ΔΣ ADC that performs the Σ, Δ, multi-bit quantization and DAC operations all is time domain using all digital circuits without switching to current or voltage domains. The system has a 52 dB dynamic range without calibration while consuming 2.7 mW of power using a 1.8V supply. The system occupies 0.027 mm^2 area in a 0.18µm digital CMOS process.

3:45 pm **BREAK**

13-4
4:00 pm **A VCO-based Current-to-Digital Converter for Sensor Applications pg. 463**

P. Prabha, S. Kim, K. Reddy, S. Rao, N. Griesert**, A. Rao**, G. Winter**, and P. Hanumolu*, Oregon State University, *University of Illinois, Urbana-Champaign, **Texas Instruments*

A current sensing VCO-based ADC is realized using a passive integrator, VCO quantizer, and digital circuits. A power efficient digital IIR filter is used to tackle VCO non-linearity in a scaling friendly manner. Designed for ambient light sensing, prototype achieves 900pA accuracy over an input current range of 4uA.

13-5
4:25 pm **Lookup-Table-Based Background Linearization for VCO-Based ADCs pg. 467**

J. McNeill, R. Majidi, J. Gong, C. Liu, Worcester Polytechnic Institute, *M/A-COM Technology Solutions*

A lookup-table digital correction technique using the "Split ADC" approach enables linearization of VCO-based ADCs. A 10b prototype in 180nm CMOS shows ENOB improved to 9.41b from an uncorrected 3.5b. The background LMS calibration tolerates different input signals and corrects linearity over the entire input signal excursion.

13-6
4:50 pm **A 1.2 V 2.64 GS/s 8bit 39 mW Skew-Tolerant Time-interleaved SAR ADC in 40 nm Digital LP CMOS for 60 GHz WLAN pg. 471**

S. Kundu, J. H. Lu, E. Alpman, H. Lakdawala**, J. Paramesh***, B. Jung*, S. Zur, E. Gordon, Intel Corp, *Purdue University, **Qualcomm Inc, ***Carnegie Mellon University*

A clock-skew tolerant 8-bit 16x time-interleaved (TI) SAR ADC is presented that meets WiGig standard requirements with only background offset and gain calibrations. By using a timing-calibration-free global bottom-plate sampling scheme, the ADC achieves 2.64GS/s >6 ENOB in the entire Nyquist band. The 40nm LP CMOS design dissipates 39mW from 1.2V. The TI-SAR ADC characterized with an integrated receiver front-end achieves -21.44dB EVM at sensitivity with an OFDM/ QAM16 signal.

13-7 **A 160 MS/s, 11.1 mW, Single-Channel Pipelined SAR ADC with 68.3 dB SNDR. pg. 475**
5:15 pm *V. Tripathi, B. Murmann, Stanford University*

A low-power, 160 MS/s, single-channel pipelined SAR ADC that employs two capacitive DACs to decouple the high-speed SAR operation from the low-noise residue generation is presented. Measured results show a peak SNDR of 68.3 dB with a Schreier FOM of 167dB. The converter core occupies 0.09 sq.mm in 65-nm CMOS.

Session 14 – Testability and Reliability Enhancement Techniques pg. 479

Tuesday, 9/16, 2:00 pm
Fir Ballroom
Session Chair: Mike Li, Altera
Session Co-chair: Gordon Roberts, McGill University

2:00 pm **Introduction**

This session starts with DFT techniques for All-Digital PLLs. The second paper proposes a low-leakage ESD clamp. Final two papers address measurement techniques for Plasma-Induced Damage and flicker noise, respectively.

14-1 **Design for Test of a mm-Wave ADPLL-Based Transmitter (Invited) pg. 480**
2:05 pm *Wanghua Wu, Marvell Semiconductor Inc.and Delft University of Technology, R. Bogdan Staszewski, John R. Long, Delft University of Technology*

This paper focuses on design-for-test (DFT) techniques applied to an ADPLL transmitter targeting mm-wave frequencies. System snapshotting via on-chip SRAM helps to identify the root cause of the design deficiencies accurately. Low-cost build-in self test (BIST) of an ADPLL performance enhances test coverage, and reduces test time and production cost.

14-2 **A Low-Leakage, Hybrid ESD Power Supply Clamp in 65nm CMOS Technology pg. 488**
2:55 pm *M. Elghazali, M. Sachdev and A. Opal, University of Waterloo*

In this work, a 65nm hybrid clamp that has static and transient clamps is presented. A NMOS based ESD clamp with level converter delay is used as a transient clamp, while diodes are used as a static clamp. Simulation and measurement results show the proposed clamp has excellent ESD characteristics.

14-3 **A Test Circuit Based on a Ring Oscillator Array for Statistical Characterization of pg. 492**
3:20 pm **Plasma-Induced Damage**
W. H. Choi, S. Satapathy, J. Keane, C. H. Kim, University of Minnesota, *Intel Corporation*

We propose a test circuit for characterizing Plasma-Induced Damage (PID) based on a ring oscillator array for collecting high-quality BTI statistics. The proposed circuit enables accurate PID-induced BTI lifetime prediction with high frequency measurement precision (>0.01%) in a short measurement time (>1μs). Measured frequency statistics from a 65nm test chip shows a clear shift in the average frequency as a result of PID.

3:45 pm **BREAK**

14-4 **Impact of Random Telegraph Noise on CMOS Logic Circuit Reliability (Invited) pg. 496**
4:00 pm *T. Matsumoto, K. Kobayashi*, H. Onodera, Kyoto University, *Kyoto Institute of Technology*

Recent researches on RTN and its impact on circuits are briefly summarized. Then the impact of RTN on CMOS logic circuit reliability is described based on our results from 65~nm and 40~nm test chips. The impact of RTN can be a serious problem even for logic circuits.

Session 15 – Challenges for Analog Nanoscale Technology pg. 504

Tuesday, 9/16, 2:00 pm
Pine Ballroom
Session Chair: Ramnath Venkatraman, LSI Corporation
Session Co-chair: Richard Guo, TSMC

2:00 pm **Introduction**

This session focuses on unique power performance for scaled technology. Analog circuit-design-manufacturing co-optimization for mobile SoCs, innovative 3IC wafer-level-system-integration and reliability are highlighted.

15-1 2:05 pm **TCAD Structure Synthesis and Capacitance Extraction of a Voltage-controlled Oscillator using Automated Layout-to-device Synthesis Methodology** pg. 505
Debajit Bhattacharya, Rajiv V. Joshi, Herschel A. Ainspan*, Ninad D. Sathaye**, Mohit Bajaj**, Suresh Gundapaneni**, Niraj K. Jha, Princeton University, *IBM Research, **IBM SRDC*

We present a TCAD structure-synthesis and capacitance-extraction methodology in a 22nm CMOS process and report parasitic capacitances of a 10-GHz VCO. We observe that front-end capacitances are dominant and quantify them along with their back-end counterparts using a novel layer-wise capacitance analysis. The estimated frequency tuning range agrees with that of a VCO hardware.

15-2 2:30 pm **The Challenges of Analog Circuits on Nanoscale Technologies (Invited)** pg. 509
G. Taylor, Intel Corporation

As SOCs integrate larger systems, the number and variety of analog/mixed signal circuits are growing. For reasons of cost, performance, and power die are being scaled to more advanced processes which do not deliver power or performance benefits for analog circuits. How are we going to bridge the gap?

15-3 2:55 pm **Technology-Design-Manufacturing Co-optimization for Advanced Mobile SoCs (Invited)** pg. 515
Geoffrey Yeap, Qualcomm Technologies Inc.

How to maintain the Moore's Law scaling beyond the 193 immersion resolution limit is the key question semiconductor industry needs to answer in the near future. Process complexity will undoubtfully increase for 14nm node and beyond, which brings both challenges and opportunities for technology development. A vertically integrated technology-design-manufacturing co-optimization flow is desired to better address the complicated issues new process changes bring. In recent years smart mobile wireless devices have been the fastest growing consumer electronics market. Advanced mobile devices such as smartphones are complex systems with the overriding objective of providing the best user-experience value by harnessing all the technology innovations. Most critical system drivers are better system performance/power efficiency, cost effectiveness, and smaller form factors, which, in turns, drive the need of system design and solution with More-than-Moore innovations. Mobile

system-on-chips (SoCs) has become the leading driver for semiconductor technology definition and manufacturing. Here we highlight how the co-optimization strategy influenced architecture, device/circuit, process technology and package, in the face of growing process cost/complexity and variability as well as design rule restrictions.

3:45 pm **BREAK**

15-4 4:00 pm **New System-in-Package (SiP) Integration Technologies (Invited) pg. 523**
Doug C.H. Yu, R&D, Taiwan Semiconductor Manufacturing Company

New System-in-Package (SiP) with innovative Wafer-Level-System-Integration (WLSI) technologies that leverage foundry core competence on wafer processes have been demonstrated. The WLSI technologies include Chip-on-Wafer-on-Substrate (CoWoS™) 3DIC and interposer, Integrated Fan-Out (InFO) and Chip-Scale Wafer-Level-Packaging. Wide application portfolio from very low I/O pin-count, low-cost devices, to medium, high and ultra-high pin-count are realized. Chip-partition followed by flexible powerful integration of single-chip or multi-chips, advanced or matured Si, logic and memory, SoC and sensor/MEMS. System values include low profile, low power, high bandwidth along with competitive cost can be readily achieved. With the chip-partition, we can sustain Moore's law longer.

15-5 4:50 pm **Reliability modeling of HK MG Technologies (Invited) pg. 529**
T. Nigam, A. Kerber, GLOBALFOUNDRIES

It has been demonstrated that the introduction of HfO_2 gate stacks into CMOS technologies provides the means to continue with traditional device gate length scaling. However, the introduction of HfO_2 as a new gate dielectric into the gate stack of FETs brings about new challenges for understanding reliability physics and qualification. This review summarizes recent advances in the modeling of charge trapping and defect generation in HfO_2 gate stacks. This paper relates the electrical properties to the chemical/physical properties of the high-κ dielectric and discusses implication for technology scaling.

Forum 2 - Wearable Electronics and Computing N/A

Tuesday, September 16, 2:00 pm
Silicon Valley Room

Organizers

Pedram Mohseni, Ph.D., Case Western Reserve University
Hua Wang, Ph.D., Georgia Institute of Technology
Edward Lee, Ph.D., Alfred Mann Foundation

2:00 pm **Wearable Computing, an Enabling Technology for Wireless Health, N/A**
Mehran Mehregany, Case Western Reserve University, Cleveland, OH

2:30 pm **Wearable Healthcare SoC and Systems, N/A**
Hoi-Jun Yoo, KAIST, Daejeon, Korea

3:00 pm **Ultra Low-Power SoC for Self-Powered Wearable ECG Sensor, N/A**
Yong Lian, National University of Singapore, Singapore

Wireless Communication for Cubic-mm Sensor Nodes, N/A

3:30 pm *David Wentzloff, University of Michigan, Ann Arbor, MI*

4:00 pm **Title to be determined, N/A**
Manos Tentzeris, Ph.D., Georgia Institute of Technology, Atlanta, GA

Educational Sessions

Educational Session 4 - Fractional-N PLLs for Frequency Synthesis pg. 537

Tuesday, September 16, 2:00 pm, Cedar Room
Speaker: Ian Galton, University of California, San Diego

Fractional-N phase-locked loops (PLLs) are widely used as RF local oscillators in wireless communication systems. Their performance is critical in such applications, so they are a subject of intensive research. This tutorial talk will provide explanations of analog, digital, and hybrid "mostly-digital" fractional-N PLLs as well as techniques that mitigate several practical implementation issues. Topics include architecture tradeoffs, phase noise models, non-ideal effects of particular concern in fractional-N PLLs, spurious tone mitigation techniques, phase noise cancellation, and frequency control methods for LC digitally controlled oscillators. Many of the concepts are presented in the context of fractional-N PLL integrated circuit case studies supported by measurement results.

Tuesday Poster Session

Tuesday, September 16, 5:00 pm – 7:00 pm
Donner, Siskyou, Cascade Ballroom

T-01 **Linear Current-Controlled Oscillator for Analog to Digital Conversion pg. 538**
K.R. Raghunandan, T. Lakshmi Viswanathan, T.R. Viswanathan, The University of Texas at Austin

Current-controlled oscillators (CCO) for A/D conversion need linear tuning-characteristics. A new CCO design in which the period of oscillation is defined by charging the timing capacitor to a reference voltage by the input current, is described. The sources of non-linearity in the tuning characteristics are identified and modeled and an analog technique of compensation is presented. The prototype circuit in 0.18um technology has 0.2% linearity from 0 - 100 degC for the frequencies upto 500 MHz.

T-02 **A Fully Integrated Translational Tracking Filter with >40dB Blocker Attenuation and >68dB Harmonic Rejection in 40nm for Digital TV Tuner Applications pg. 542**
Kun-Da Chu, Ying-Tsang Lu, Chao-Wei Wang, Chih-Ming Hung, Meng-Chang Lee, Shih-Chieh Yen, MediaTek Inc., *MStar Semiconductor Inc.*

A fully integrated tunable high-Q translational tracking filter (TTF) implemented in a 40nm CMOS for Digital TV tuners is presented. Combining feed-forward cancellation and harmonic rejection in a nested translational filter matrix, >40dB blocker suppression and >68dB harmonic rejection are achieved without any calibration at low current of 25mA.

T-03 **An Area-efficient 12-bit 1.25MS/s Radix-value Self-estimated Non-binary ADC with Relaxed Requirements on Analog Components pg. 546**
H. San, R. Sugawara, Masao Hotta, T. Matsuura, K. Aihara**, Tokyo City University, *Tokyo University of Science, **University of Tokyo*

A 12-bit algorithmic (cyclic) ADC is designed and fabricated in 90nm CMOS, and only

occupies as small active area as 0.037mm^2. With the proposed radix-value self-estimation scheme for a non-binary 1-bit/step architecture, the accuracy requirement on analog components is largely relaxed. Therefore, the implementation of analog circuits such as amplifier and comparator becomes simple, and high-density MOM capacitors can be used to achieve small area. Furthermore, the novel radixvalue self-estimation technique can be realized by only simple logic circuits without any extra analog input, so that the total active area of ADC is dramatically reduced.

T-04 **A 5mW 250MS/s 12-bit Synthesized Digital to Analog Converter pg. 550**
E. Ansari, D. D. Wentzloff, University of Michigan - Ann Arbor

This paper presents a low-power 12-bit, 250MS/s DAC completely implemented using standard digital design flows and automatic place and route. Calibration algorithms are implemented in order to compensate for the introduced mismatch. The DAC is fabricated in 65nm-CMOS technology, and achieves SFDR>50dBc at 100MHz input frequency while consuming only 5mW.

T-05 **Inherently Linear Time Symmetric Pulse Width Modulation pg. 554**
Y. Hu, Y. Xu, U. Moon, Oregon State University

This paper proposes a novel PWM scheme to avoid inherent harmonic distortion from conventional PWMs. An ADC structure is implemented utilizing the proposed technique and TDC quantizer. The successful operation of this architecture is demonstrated by the removal of harmonic distortion on the TDC output without using calibration or adding circuit complexity.

T-06 **A VCO-Based ADC Employing a Multi-Phase Noise-Shaping Beat Frequency Quantizer for Direct Sampling of Sub-1mV Input Signals pg. 558**
B. Kim, S. Kundu, S. Ko, C. H. Kim, University of Minnesota

A VCO-based ADC featuring a multi-phase beat frequency based quantization scheme with first order noise shaping is demonstrated in a 65nm CMOS process. The proposed ADC is unique in that it can achieve high resolution (e.g. 6-7ENOB) for signals with extremely small amplitudes (e.g. <1mV. This allows us to remove or simplify the pre-conditioning amplifiers, reducing power consumption as well as the overall system complexity. The proposed ADC achieves 43dB SNDR for a 1mV input signal while achieving a 10kHz bandwidth and 300kHz sample rate, and consumes 36μW at a 1.2V supply.

T-07 **A 65 nm CMOS Tunable 0.1-to-1.6 GHz Distributed Transmission Line N-Path Filter with +10 dBm Blocker Tolerance pg. 562**
C. Thomas, University of California, San Diego and L. Larson, Brown University

A distributed transmission line N-path bandpass filter is presented from 0.1 to 1.6 GHz with 30 MHz 3dB pass-band bandwidth, LO leakage < -60 dBm, 30 dB to 50 dB out-of-band rejection, in-band IIP3 of +23 dBm, and a +10.1 dBm out-of-band jammer tolerance in a 65 nm CMOS process.

T-08 **A 0.8V 140nW Low-Noise Energy Harvesting CMOS APS Imager with Fully Digital Readout pg. 566**
I. Cevik, S. U. Ay, University of Idaho

This paper presents a novel CMOS active pixel sensor (APS) imager with fully digital global

readout channel and continuous time on-chip energy harvesting. Imager captures low-noise images while consuming 140nW of power at 0.7 FPS. Imager has a 0.078% total FPN in dark. It generates 31µW power at bright daylight.

T-09 **A Bidirectional Neural Interface SoC with an Integrated Spike Recorder, Microstimulator, and Low-Power Processor for Real-Time Stimulus Artifact Rejection** **pg. 570**

K. Limnuson, H. Lu, H. Chiel, P. Mohseni, Case Western Reserve University

This paper presents a neural interface system-on-chip (SoC), featuring combined spike recording, electrical microstimulation and real-time stimulus artifact rejection (SAR) based on template subtraction for bidirectional interfacing with the central nervous system.

T-10 **Mixed-Signal Stochastic Computation Demonstrated in an Image Sensor with Integrated 2D Edge Detection and Noise Filtering** **pg. 574**

D. Fick, G. Kim, A. Wang, D. Blaauw, D. Sylvester, University of Michigan

We describe mixed-signal stochastic computing (MSSC) and demonstrate how it can be used to efficiently integrate computation into a signal path before data conversion. MSSC performs computation directly on the analog values output by sensors, which combines the area efficiency of traditional stochastic computing with the performance of analog computation.

T-11 **A 14pJ/Pulse-TX, 0.18nJ/b-RX, 100Mbps, Channelized, IR-UWB Transceiver for Centimeter-to-Meter Range Biotelemetry** **pg. 578**

A. Ebrazeh, P. Mohseni, Case Western Reserve University

This paper presents an energy-efficient, customizable, high-data-rate, impulse radio ultra wideband (IR-UWB) transceiver, operating in three channels within 3–5GHz for centimeter-to-meter range biotelemetry. The transceiver integrates an all-digital transmitter and a non-coherent receiver with front-end RF amplification/filtering, self-correlation for energy detection and baseband clock and data synchronization.

T-12 **SRAM Read Performance Degradation under Asymmetric NBTI and PBTI Stress: Characterization Vehicle and Statistical Aging Data** **pg. 582**

X. Wang, W. Xu, C.H. Kim*, Intel Corp., *University of Minnesota*

In this paper, we propose the first known on-chip reliability monitor to accurately characterize the impact of asymmetric BTI in SRAM peripheral circuit on the read speed. Measurement results from a 32nm test chip have been presented to demonstrate the statistical behavior of read frequency degradation under different stress conditions.

T-13 **A Methodology for Yield-Specific Leakage Estimation in Memory** **pg. 586**

Subho Chatterjee, Pramod Kolar, Wei Jian Chan, Jae Y Ko, Gunjan H. Pandya, Intel Custom Foundry

A simulation based pre-silicon yield-specific leakage estimation methodology for SRAM is proposed. It comprehends the impact of die to die and within die variations. Comparative studies between different bit cells show that relative leakage could be up to 53% different if we do not use the methodology. Finally results from the methodology are shown to match measured silicon data at 22nm tri-gate CMOS technology to within 12% accuracy over the region of interest.

T-14 **Anti-ESL/ESR Variation Robust Constant-on-time Control for DC-DC Buck Converter in 28nm CMOS Technology pg. 590**

Hsin-Chieh Chen, Wei-Chung Chen, Ying-Wei Chou, Meng-Wei Chien, Chin-Long Wey, Ke-Horng Chen, Ying-Hsi Lin, Tsung-Yen Tsai*, and Chao-Cheng Lee*, National Chiao Tung University, *Realtek Semiconductor Corp.*

Conventional constant-on-time (COT) control for DC-DC buck converter is apt to be affected by the noise caused by parasitic effect including not properly specified and temperature dependent equivalent series resistance (ESR) and equivalent series inductance (ESL). As a result, the safety operation area (SOA) of the COT is limited by the selection of external components. In this paper, the calibrated anti-ESL (CAESL) technique and the calibrated gain and BW (CGB) technique for alleviating ESL and ESR variation, respectively, are proposed to ensure a robust COT control. Furthermore, degraded output regulation caused by enlarged ESL effect due to input battery voltage variation is also solved by the CAESL technique. The proposed COT converter fabricated in 28nm CMOS technology uses an output capacitor with an ESR smaller than 1mΩ, output ripple of 20mV, and high efficiency higher than 95%. The CAESL circuit can tolerate ESL voltage variation from 0 to 50mV even when operation temperature varies from -40 to 120℃.

T-15 **Impact of Inductive Integrated Voltage Regulator on the Power Attack Vulnerability of Encryption Engines: A Simulation Study pg. 594**

M. Kar, D. Lie, M. Wolf, V. De, and S. Mukhopadhyay,Georgia Institute of Technology, *Intel Labs*

This paper shows that inductive integrated voltage regulators (IVR) provide significant immunity to traditional power attacks on crypto encryption engines based on time-domain analysis of the chip current. Frequency-domain analyses of envelope and duty cycle of the current are identified as new attack modes. The security-aware IVR design is discussed.

T-16 **True Random Number Generator Circuits Based on Single- and Multi-Phase Beat Frequency Detection pg. 598**

Q. Tang, B. Kim, Y. Lao, K. K. Parhi, and C. H. Kim, University of Minnesota

A fully-digital True Random Number Generator (TRNG) measures the frequency difference between two free-running ring oscillators, or in other words the beat frequency, to extract random frequency jitter. For generating a continuous stream of random bits with a high entropy level, the lower significant bits meeting the NIST randomness criteria are concatenated. The generation efficiency is further improved by utilizing a multi-phase structure. The proposed circuit fabricated in 65nm achieves an energy efficiency of 15.1Mb/mW at 0.8V. Experimental data collected from eight TRNG test chips passed all 15 NIST tests without the use of any feedback or tracking scheme.

T-17 **Energy-efficient Mixed-mode Support Vector Machine Processor with Analog Gaussian Kernel pg. 602**

Kyeongryeol Bong, Gyeonghoon Kim, Hoi-Jun Yoo, KAIST

In this work, mixed-mode svm processor is proposed. Analog gaussian kernel datapath enables the energy efficient and reconfigurable svm processing with a digital controller. Digitally-assisted calibration shapes the gaussian to remove non-uniformity under temperature variation. Completion detection circuit optimally controls the 2-stage pipeline between analog datapath and digital controller.

T-18 **Characterization of Radiation-Induced SRAM and Logic Soft Errors from 0.33V to 1.0V in 65nm CMOS pg. 606**

R. Pawlowski, J. Crop, M. Cho, J. Tschanz*, V. De*, T. Fairbanks**, H. Quinn**, S. Borkar*, P.Y. Chiang, Oregon State University, *Intel Corporation, **Los Alamos National Laboratory*

This work presents a radiation test chip, fabricated in 65nm CMOS, designed to characterize radiation-induced soft errors during near-threshold operation. A variety of memory and logic test structures are included to provide a comprehensive assessment of circuit sensitivities to radiation. Results and analysis from neutron and alpha experiments are detailed.

T-19 **A Wideband RF Receiver with >80 dB Harmonic Rejection Ratio pg. 610**

R. Liu, L. Pileggi, J. A. Weldon, Carnegie Mellon University

A wideband RF receiver design with harmonic rejection (HR) is presented. Both gain mismatch and phase mismatch of the HR mixer have been calibrated independently. After calibration, both the 3rd order harmonic rejection ratio (HRR) and the 5th order HRR are greater than 80 dB and 70 dB respectively.

T-20 **85-to-127 GHz CMOS Transmitter for Rotational Spectroscopy pg. 614**

N. Sharma, J. Zhang, Q. Zhong, W. Choi, K. K. O, J. P. McMillan, C. F. Neese*, F. C. De Lucia*, University of Texas at Dallas, *Ohio State University*

A transmitter for rotational spectroscopy using a fractional-N PLL (FNPLL) that generates frequency shift keyed signals from 85 to 127 GHz (39% tuning range) with a fine frequency step of ~570 Hz and settling time of ~10 μS is demonstrated. Implemented in 65-nm CMOS, the FNPLL delivers greater than 5 μW of output power, and achieves measured phase noise of less than -70 dBc/Hz in-band and less than -102 dBc/Hz at 10-MHz offset over the output frequency range while consuming 80 mW. The transmitter output is radiated using a bond-wire antenna and successfully utilized in a spectrometer for detection of gas molecules.

T-21 **A 135GHz SiGe Transmitter With A Dielectric Rod Antenna-In-Package For High EIRP/Channel Arrays pg. 618**

N. Saiz, N. Dolatsha, A. Arbabian, Stanford University

A 135 GHz antenna-in-package (AiP) with high equivalent isotropic radiated power is presented. The radiating element is realized by a dielectric rod antenna and a D-Band SiGe transmitter is mounted on the AiP. The operating frequency of the system is 125-140 GHz with a measured EIRP of 15.57dBm at 135GHz.

Session 16 – Analog Techniques pg. 622

Wednesday, 9/17, 9:00 am
Oak Ballroom
Session Chair: John McNeill, Worcester Polytechnic Institute
Session Co-chair: Mohammad Ranjbar, Inphi Corporation

9:00 am **Introduction**

This session includes an invited paper with in-depth analysis of the classic regenerative comparator circuit, techniques for high-accuracy time-to-digital conversion and clock generation, and low power approaches for voltage reference design and sensor monitoring.

Understanding the Regenerative Comparator Circuit (Invited) pg. 623

16-1
9:05 am

A. Abidi, H. Xu, University of California, Los Angeles

The regenerative comparator circuit which lies at the heart of A/D conversion, slicer circuits, and memory sensing, is unstable, time-varying, nonlinear, and with multiple equilibria. That does not mean, as this paper shows, that it cannot be understood with simple equivalent circuits that reveal its dynamics completely, and enable it to be designed to specifications on static and dynamic offset and noise. The analysis is applied to the StrongArm latch.

16-2
9:55 am

A 9-bit 215-MS/s Folding-Flash Time-to-Digital Converter Based on Redundant Remainder Number System pg. 631

B. Wu, S. Zhu, Y. Zhou, Y. Chiu, University of Texas at Dallas

A novel folding-flash TDC based on the remainder number system is presented. Time quantization is performed with two free-running ring oscillators without any counter. A proof-of-concept 45-nm CMOS prototype TDC, consisting of 84 delay elements, achieves a resolution of 8.94 bits, 215 MS/s and an LSB size of 9.4 ps.

16-3
10:20 am

A 0.010mm^2 9.92ps$_{rms}$ Low Tracking Jitter Pixel Clock Generator with a Divider Initializer and a Nearest Phase Selector in 28nm CMOS Technology pg. 635

Kangyeop Choo, Sung-Jin Kim, Wooseok Kim, Jihyun Kim, Taeik Kim, Hojin Park, Samsung Electronics

A single loop low tracking jitter pixel clock generator is demonstrated in 28nm CMOS process. The proposed architecture only consists of a conventional single loop wide bandwidth fractional-N PLL and two synchronization skills which suppress the tracking jitter and bring out the delay control function like a DLL. When a 250MHz pixel clock is generated and synchronized with a 10kHz HSYNC, the measured tracking jitter is 9.92ps$_{rms}$. The total power consumption is 9.7mW and the silicon area is only 0.010mm^2 in 28nm CMOS process.

10:45 am **BREAK**

16-4
11:05 am

A -115dB PSRR CMOS Bandgap Reference With a Novel Voltage Self-Regulating Technique pg. 639

Y.M. Zhu, F. Liu, Y.J. Yang, G.C. Huang, T. Yin, H.G. Yang, Institute of Electronics, Chinese Academy of Sciences, Beijing, China

A novel high PSRR bandgap reference is presented. The circuit employs a self-regulating technique to significantly suppress the supply noise over a broad frequency range. Measurement results show that the PSRR of the voltage reference has achieved -115dB@DC and -90dB@10MHz.

16-5
11:30 am

A 500nA Quiescent Current, Trim-Free, ±1.75% Absolute Accuracy, CMOS-Only Voltage Reference based on Anti-Doped N-Channel MOSFETs pg. 643

Mohammad Al-Shyoukh, Alex Kalntisky, TSMC

In this paper, an ultra low power CMOS-only voltage reference is presented. The reference exploits the work function difference between anti-doped (flipped-gate) and standard-doped nMOS devices. These devices require no additional processing and are realizable from the basic N+ and P+ implants used to implement the standard enhancement mode MOS devices on the process. The reference is implemented as a temperature-compensated Δ_{gs} between anti-doped and standard-doped nMOS devices. Integrated on 0.18µm CMOS, the reference

occupies less than 0.04mm^2 on silicon, requires less than 500nA of quiescent current, and has a trim-free accuracy of ±1.75% which is comparable to that of the most well-behaved voltage references employing BJTs.

16-6 11:55 am **A 5.8nW, 45ppm/°C On-Chip CMOS Wake-up Timer Using a Constant Charge Subtraction Scheme pg. 647**
Seokhyeon Jeong, Inhee Lee, David Blaauw, Dennis Sylvester: University of Michigan

This work presents an ultra-low power oscillator designed for wake-up timers in compact wireless sensors. A constant charge subtraction scheme removes continuous comparator delay from the oscillation period, which is the source of temperature dependence in conventional RC relaxation oscillators. This relaxes comparator design constraints, enabling low power operation. In 0.18µm CMOS, the oscillator consumes 5.8nW at room temperature with temperature stability of 45ppm/°C (-10°C to 90°C) and 1%V line sensitivity.

Session 17 – Advanced Simulation Techniques pg. 651

Wednesday, 9/17, 9:00 am
Fir Ballroom
Session Chair: Chenie Gu, Intel
Session Co-chair: Laurence Nagel, Omega Enterprises Consulting

9:00 am **Introduction**

This session contains three papers that present new and exciting techniques for the simulation of integrated circuits including an invited paper on stochastic testing simulation

17-1 9:05 am **Stochastic Testing Simulator for Integrated Circuits and MEMS: Hierarchical and Sparse Techniques (Invited) pg. 652**
Z. Zhang, X. Yang, G. Marucci**, P. Maffezzoni**, I. M. Elfadel***, G. Karniadakis*, L. Daniel, Massachusetts Institute of Technology, *Brown University, **Politecnico di Milano, ***Masdar Institute of Science and Technology*

We present two algorithms for fast statistical simulation of MEMS and IC. Based on our stochastic testing simulator, we first present a stochastic hierarchical approach to simulate a complex system consisting of several blocks. Second, we present an algorithm based on anchored ANOVA for simulating circuits with many process variations.

17-2 9:55 am **PPV-Based Modeling and Event-Driven Simulation of Injection-Locked Oscillators in SystemVerilog pg. 660**
J. Kim, S. Yang, J.-E. Jang, Seoul National University

Injection-locked oscillators (ILO) have widespread use in wireline and wireless systems as fast-locking clock generators, phase noise filters, and frequency multipliers/ dividers, but their modeling and simulation typically resort to SPICE due to their nonlinear, time-varying characteristics. This paper presents a way to simulate ILOs in an event-driven logic simulator such as SystemVerilog, based on a perturbation projection vector (PPV) model. By expressing the continuous-time signals in analytical forms of which coefficients are updated as events, the nonlinear phase response of the ILO can be simulated in an algebraic fashion without numerical integration.

17-3 **Efficient Per-Element Distortion Contribution Analysis via Harmonic Balance pg. 664**

10:20 am **Adjoints**
B. Wu, J, Roychowdhury, University of California, Berkeley

We propose a new metric for quantifying per-element distortion that is simple, intuitive and well-defined for both small- and large- signal excitations. Traditional distortion concepts, based on polynomial expansions and Volterra series, can be viewed as an approximation of our new metric. Although computing this metric exactly is quadratic in circuit size, we devise a novel approximation that (unlike polynomial/Volterra) also makes sense for large distortions and can be computed efficiently using adjoint Harmonic Balance. We validate our new approximate metric on a differential pair and the 741 op-amp, comparing it against the full metric and demonstrating order-of-magnitude speedups. Unlike polynomial/Volterra based methods, our proposed per-element distortion computation technique is easy to implement in any modern simulator that features Harmonic Balance or similar steady-state/RF analyses.

10:45 am **BREAK**

Session 18 – High Performance Wireless Receiver Techniques and 4G Cellular Transceivers

Wednesday, 9/17, 9:00 am
Pine Ballroom
Session Chair: Julian Tham, Broadcom
Session Co-chair: Yanjie (Jay) Wang, Intel

9:00 am **Introduction**

High performance wireless receiver techniques for blocker and harmonic rejection and LO suppression together with 4G cellular transceiver specifications and a carrier aggregation receiver are presented.

18-1
9:05 am **The Role of Translational Circuits in RF Receiver Design (Invited) pg. 668**
Behzad Razavi

This paper provides an overview of translational or commutated circuits and their role in RF receivers. Insights are offered into the frequency translation of impedances, their modeling, and their application in input matching, blocker rejection, and channel selection. A new front end is also described that rejects blockers at the third harmonic of the local oscillator frequency.

18-2
9:55 am **A 16-band Channelizer Employing Harmonic Rejection Mixers with Enhanced Image Rejection pg. 676**
Vineet Singh, Travis Forbes, Wei-Gi Ho, Jaegan Ko, Ranjit Gharpurey, University of Texas at Austin

A channelizing broadband receiver for a spectrum analysis application that employs a bank of two-stage harmonic rejection mixers (HRMs) is described. Each HRM internally synthesizes a distinct downconversion LO. In addition to minimizing LO harmonic response, the HRMs also include a quadrature phase matching technique for enhancing image rejection. The technique reduces the two-dimensional calibration for enhancing image performance, that requires amplitude and phase correction, into a one-dimensional problem, thereby significantly reducing calibration complexity. The prototype receiver downconverts an I/Q input of

bandwidth 250 MHz to baseband and channelizes the signal concurrently into 16 sub-bands of bandwidth 15.625 MHz each. The design is implemented in 65nm CMOS. It achieves an image rejection of 56 dB with amplitude calibration alone, and a harmonic rejection of 56.5 dB without any calibration for a 1 MHz baseband output.

18-3 10:20 am **A Baseband Technique for Automated LO Leakage Suppression Achieving <-80dBm in Wideband Passive Mixer-First Receivers pg. 680**
S. Jayasuriya, D. Yang, A. Molnar, Cornell University

A baseband technique is presented to detect and suppress LO leakage in passive mixer-first receivers. Modulating the RF port's impedance, the leakage is down-converted and detected from baseband outputs where current DACs cancel this leakage. Suppression <-80dBm is shown with a fully automated algorithm without RF spectrum monitoring.

10:45 am **BREAK**

18-4 11:05 am **Multi-mode Cellular Transceivers for LTE and LTE-Advanced (Invited) pg. 684**
P. Rakers, M. Alam, D. Newman, K. Hausmann, D. Schwartz, M. Rahman, M. Kirschenmann, Intel Mobile Communications

This paper presents some of the challenges unique to a multi-mode transceiver supporting LTE and LTE-Advanced. Specific technical solutions are provided for duplex offset IIP2 and counter intermodulation.

18-5 11:55 am **Reconfigurable Blocker-Resilient Receiver with Concurrent Dual-band Carrier Aggregation pg. 692**
Run Chen, Hossein Hashemi, University of Southern California

A reconfigurable SDR receiver supporting dual-band carrier aggregation is demonstrated. The front-end filter can be configured either as a bandpass or a notch filter. Carrier aggregation is achieved by combing N-path filter with complex signal processing. The notch filter improves the blocker tolerance by 15dB compared to the bandpass mode.

Session 19 – Energy-efficient Bio-Sensing System pg. 696

Wednesday, 9/17, 11:00 am
Fir Ballroom
Session Chair: Pedram Mohseni, Case Western Reserve University
Session Co-chair: Patrick Chiang, Oregon State University

11:00 am **Introduction**

The invited papers in this session will first discuss compressive sensing as a novel approach to achieve energy scaling in highly complex sensing systems, and will then review the design tradeoffs in low-power biosignal recording interfaces.

19-1 11:05 am **Energy Scaling in Multi-tiered Sensing Systems Through Compressive Sensing (Invited) pg. 697**
M. Shoaib, J. Liu, M. Phillipose, Microsoft

High functional complexity is leading us towards new architectures for sensing systems. Multi-tiered design is one among the many emerging alternatives. Such architectures bring

new opportunities for effective system-level power management. For instance, varying one/more tier-level parameters can provide substantial end-to-end energy scaling. In this paper, we review an existing approach that shows how one such parameter, namely data compression, can help us scale energy at the cost of algorithmic accuracy. The methodology is driven by a case study of inferring the onset of seizure events directly from compressively-sensed electroencephalograms. Results from an integrated circuit implementation have shown tier-level computational energy scaling in the range 1.2-214 μJ depending on the amount of compression (2-24×) and inference accuracy (sensitivity, latency, and specificity of 91-96%, 4.7-5.3 sec., and 0.17-0.30 false-alarms/hr., respectively). The projections we make in this paper show that for similar systems, compressive sensing, through this approach, has the potential to prolong battery lives of all tiers by up to 5×.

19-2
11:55 am

Robust, Reconfigurable, and Power-Efficient Biosignal Recording Systems (Invited) pg. 705
Vaibhav Karkare, Hariprasad Chandrakumar, Dejan Rozgić, Dejan Marković, University of California, Los Angeles, USA

A VCO-based biosignal recording front-end can meet the often sidelined dynamic-range specification for biosignal recordings, without a significant power/area increase over prior work. The compute-communicate tradeoff is crucial for system power optimization, especially for neural action-potential recording. Development of micro thermoelectric generators is a promising precursor to self-powered sensors.

Educational Sessions

Educational Session 5 pgs. 713-741

Wednesday, September 17, 9:00 am, Cedar Room
An Introduction to Design Considerations of DRAM Memory Controllers
Speaker: David Wang, Inphi Corporation

The session on design considerations of DRAM memory controller is presented as five inter-related sub-sessions. Session one presents the overview of the role of the memory controller in specific applications as the bridging device between one or more logical processing elements and one or more DRAM memory devices. Session two examines the processor-to-memory-controller interface. Session three examines the memory-controller-to-DRAM interface. Session four examines the internal structures of the memory controller interface. Then session five summarizes the presentation and discusses specific examples.

Educational Session 6 pgs. 742-803

Wednesday, September 17, 11:00 am, Cedar Room
Advanced Modeling and Simulation of State-of-the-Art High-Speed I/O Interfaces
Speaker: Jaeha Kim, Seoul National University

This tutorial will highlight advanced modeling and simulation methods to estimate various performance metrics such as bit-error rate (BER), eye-opening, and jitter tolernce (JTOL) of state-of-the-art high-speed I/O interfaces. Specifically, the talk will address how to model interferences and noises present in I/O systems and estimate BERs using efficient statistical simulation techniques. Topics of interest include: modeling the nonlinear distortion, finite aperature, and noise in analog front-end circuits such as equalizers and clocked comparators; assessing the effects of power-supply noise and feedback latency in digitally-controlled timing circuits such as PLLs and CDRs; simulating the transient and steady-state behaviors of various calibration loops such as equalizer adaptation loops and offset

calibration loops; and evaluating design trade-offs in ADC-based links.

Session 20 – Modeling of Advanced Devices pg. 804

Wednesday, 9/17, 1:30 pm
Fir Ballroom
Session Chair: Colin McAndrew, Freescale Semiconductor, Inc.
Session Co-chair: Hidetoshi Onodera, Kyoto University

1:30 pm **Introduction**

This session introduces the NEEDS project, for compact modeling of emerging and future technologies, followed by recent developments in models for today's advanced devices and circuits.

20-1 **NEES: Moving Nanoscience to Nanotechnology (Invited) pg. 805**
1:35 pm *Mark Lundstrom, Purdue University*

NEEDS was established to provide physics-based, SPICE-compatible models for emerging nano-devices, and it is also developing a compact model development toolset, complemented with educational and training resources. This paper discusses the rationale for establishing NEEDS, its status and plans, and how those not in the formal program can participate.

20-2 **Optimization and Modeling of Resonant Clocking Inductors for the POWER8**
2:00 pm **Microprocessor pg. 809**
Robert Groves, Phillip Restle, Alan Drake, David Shan, Michael Thompson, IBM

A parameterized model for resonant clocking inductors embedded in a dense power grid was developed using electromagnetic simulations. The model was used to support resonant clock designs for the POWER8 microprocessor. Simulations using the model showed excellent agreement with measurement for inductance, Q and global clock power.

20-3 **Virtual De-embedding Study for the Accurate Extraction of Fin FET Gate Resistance pg. 813**
2:25 pm *S. Warnock*, R. Groves, H. Li, R. Wachnik, P. Kotecha, S. Lee**, N. Lu**, P. Solomon***, K. Jenkins***, IBM Semiconductor Research and Development Center at Hopewell Junction NY, *Massachusetts Institute of Technology, **IBM Semiconductor Research and Development Center at Essex Junction VT, ***IBM Research at Yorktown Heights NY*

This work presents a "Virtual De-Embedding" approach to the optimization of gate resistance measurement structures and de-embedding methodologies. We examine the effects of BEOL stack choice, groundplane design, FET size, and de-embedding technique on gate resistance measurement accuracy.

20-4 **Modeling of Resistance in FinFET Local Interconnect pg. 817**
2:50 pm *N. Lu, P. M. Kotecha, R. A. Wachnik, IBM*

We present an innovative and comprehensive approach to model the resistance of local interconnect used in finFET technologies. Our resistance formulas cover both merged and unmerged fin processes. They have been verified with field solver simulation results, and are found to be accurate over a wide range of parameter values.

3:15 pm **BREAK**

20-5 3:30 pm **Compact Modeling of LDMOS Working in the Third Quadrant pg. 821**
Kejun Xia, Maxim Integrated, Harihara Indana, Usha Gogineni, Maxim Integrated Circuit Design Pvt. Ltd, India

This paper presents a method to model the drain current of LDMOS working in the 3rd quadrant (Vds<0), which is important for power management IC design. A drain current expression for the sub-threshold region is developed and added to the device model through a SPICE component bsource. The modeling accuracy is significantly improved.

Session 21 – Advanced Memory Topics pg. 825

Wednesday, 9/17, 1:30 pm
Pine Ballroom
Session Chair: Toshiaki Kirihata, IBM
Session Co-chair: Dinesh Somasekhar, Intel

1:30 pm **Introduction**

This session covers advanced memory topics on high performance SRAMs, LPDDR4, DRAM, ECC, BTI, and PCM.

21-1 1:35 pm **Directions in Future of SRAM with QDR-WideIO for High Performance Networking Applications and Beyond (Invited) pg. 826**
Ali Keshavarzi, Dinesh Maheshwari, Derwin Mattos, Ravi Kapre, Sandeep Kirshnegowda, Morgan Whately, Sudhir Gopalswamy, Cypress Semiconductor

In this paper we describe the high performance synchronous QDR-WideIO SRAM KGD from Cypress that is architected with fast and wide interface with optimized memory sub-system for future high performance networking and computing applications. Systems for next generation networking switches rely on high rate router line cards of 200 to 400 Gbps. QDR-WideIO fabricated on 28nm HKMG technology builds upon High Bandwidth Memory (HBM) interface standard while using 2.5D/3D stacking to form a System in Package (SiP) networking system solutions. We explain that both SRAM and DRAM are necessary and can co-exist in these systems and why it does not make sense to integrate the SRAM inside the logic ASIC. We also describe the memory design and partitioning that allows for delivering requisite Random Transaction Rate (RTR) representing random accesses to the memory per second of approaching 24000 MT/s (>10X improvement over our previous generation of QDR-IV synchronous SRAM) and total bandwidth of greater than 1.5 Tbps in a power efficient way. QDR-WideIO achieves latency of 13 cycles for read and 8 cycles for write with density of 288Mb with core operating at 1500 MHz. Finally we describe a path forward toward future of in-package integrated products.

21-2 2:25 pm **A 16 kB Tile-able SRAM Macro Prototype of an Operating Window of 4.8GHz at 1.12V VDD to 10 MHz at 0.5V in a 28-nm HKMG CMOS pg. 832**
Ming-Zhang Kuo, Henry Hsieh, Sang Dhong, Ping-Lin Yang, Cheng-Chung Lin, Ryan Tseng, Kevin Huang, Min-Jer Wang, Wei Hwang, Taiwan Semiconductor Manufacturing Company, *National Chiao-Tung University*

The paper is focused on the low-voltage design and optimization needed for DVFS. Cross-coupled PMOS keepers with a higher P-to-N ratio NAND2 as the local readout circuit, optimizing the global bit-line keeper size, and a new concept of ICPW have showed enhanced noise immunity and faster read-write speed.

21-3 2:50 pm **HTOL SRAM Vmin shift considerations in scaled HKMG technologies pg. 836**
S. Balasubramanian, V. Joshi, T. Klick, R. Mann, J. Versaggi, A. Gautam, C. Weintraub, G. Kurz, G. Krause, A. Kerber, B. Parameshwaran, T. Nigam, GLOBALFOUNDRIES

This paper examines the role of NBTI and PBTI on SRAM Vmin shifts during HTOL stressing and quantifies their impact on reliability lifetime projections in scaled high-k metal gate (HKMG) technologies. Correlation between measured HTOL SRAM Vmin shifts and transistor level parametrics is summarized on both 28nm poly-SiON and HKMG technologies. The paper concludes that the commonly used HTOL acceleration voltage of 1.4xVnom may be excessive in scaled HKMG technologies due to the larger role of PBTI in SRAMs

3:15 pm **BREAK**

21-4 3:30 pm **A 1.1V 2y-nm 4.35Gb/s/pin 8Gb LPDDR4 Mobile Device with Bandwidth Improvement techniques pg. 840**
Keunsoo Song, Sangkwon Lee, Dongkyun Kim, Youngbo Shim, Sangil Park, Bokrim Ko, Duckhwa Hong, Yongsuk Joo, Wooyoung Lee, Yongdeok Cho, Wooyeol Shin, Jaewoong Yun, Hyengouk Lee, Jeonghun Lee, Eunryeong Lee, Jaemo Yang, Haekang Jung, Namkyu Jang, Joohwan Cho, Hyeongon Kim, Jinkook Kim, SK hynix

The demands on higher bandwidth with reduced power consumption in mobile market are driving mobile DRAM to have advanced design techniques. Proposed LPDDR4 in this paper achieves over 30% improved power efficiency and over 4.3Gbps data rate with 1.1V supply voltage. These are challenging target comparing with that of LPDDR3. This works includes various techniques including multi-channel per die, various trainings, low swing interface, DQS and clock frequency dividing, internal reference voltage for data and command-address signals and so on. This chip was fabricated in a 3-metal 2y-nm DRAM CMOS process.

21-5 3:55 pm **Exploiting Error-Correcting Codes for Cache Minimum Supply Voltage Reduction while Maintaining Coverage for Radiation-Induced Soft Errors pg. 844**
Alex Park, Venkat Narayanan, Keith Bowman, Francois Atallah, Alain Artieri, Sei Seung Yoon, Kendrick Yuen, David Hansquine, Qualcomm Incorporated

Model projections and silicon measurements from a 7Mb cache in a 20nm technology reveal insight into the trade-off between the minimum supply voltage (VMIN) reduction and soft-error protection when applying single-error correction, double-error detection (SECDED). Silicon measurements demonstrate a 19% lower VMIN while maintaining 99.88% coverage for radiation-induced soft errors.

21-6 4:20 pm **A Two-step 5b Logarithmic ADC with Minimum Step-size of 0.1% Full-scale for MLC Phase-Change Memory Readout pg. 848**
J. Kwon, D. Jin, H. Kim, S. Hwang, M. Shin, J. Kang*, S. Ryu, Korea Advanced Institute of Science and Technology, *SK Hynix*

A compact two-step 5b logarithmic ADC is designed for the readout application of multi-level cell phase-change memory. The chip was fabricated using a 65 nm CMOS and the width of a single channel ADC is 15 um. Single-channel ADC consumes 108 uW at 10 MS/s conversion rate under a 1.2 V supply.

Educational Sessions

Educational Session 7 pgs. 852-904

Wednesday, September 17, 1:30 pm, Cedar Room
Reconfigurable SDR Front-end Techniques
Speaker: Bram Nauta, University of Twente

Due to the increase of wireless standards using different RF frequencies there is a need to have receivers that can handle a wide range of RF frequencies. Also future cognitive radio will use an even more wide range of frequencies. The challenge in these modern receivers is that the amount of filtering at RF using classical bulky and expensive fixed-frequency filters should be minimized to save cost and volume. However these RF filters did serve an important purpose: to protect the transceiver from strong out of band interferers. Moreover in these classical narrow band systems one could use resonant circuits, which offered passive amplification of voltages while adding little noise. By abandoning this narrowband approach, new receiver architectures are explored, which can work without these fixed-frequency filters at RF. Challenges are: wide-band circuits with low noise and high linearity and where possible removal of interferers outside the radio band/channel in use. In this presentation several innovative techniques will be described, such as noise cancelling, distortion cancelling, frequency translated filtering, N-path filtering and beamforming.

Educational Session 8 pgs. 905-944

Wednesday, September 17, 3:30 pm, Cedar Room
Recent Developments in RF Receivers
Speaker: Behzad Razavi, UCLA

RF designers cannot rest. The demand for low-power, multi-mode, multi-band radios continues to exact more efficient and compact receiver designs. This presentation describes state-of-the-art developments in high-performance RF receivers, focusing on the new paradigms that elegantly deal with power and complexity issues. Concepts such as noise-cancelling receivers, blocker-tolerant systems, and carrier aggregation are introduced and low-power techniques at the circuit and architecture levels are presented. A number of case studies are used to illustrate these efforts.