

2014 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems

(DFT 2014)

**Amsterdam, Netherlands
1-3 October 2014**



**IEEE Catalog Number: CFP14078-POD
ISBN: 978-1-4799-6156-6**

Proceedings of the

**2014 IEEE International Symposium on
Defect and Fault Tolerance in VLSI
and Nanotechnology Systems (DFT)**

1 – 3 October 2014
Amsterdam

Sponsors by



Foreword

On behalf of the steering committee, organizing committee and the program committee, we welcome you to twenty-seventh edition of the IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2014) being held in Amsterdam, October 1 – 3, 2014.

DFT 2014 is sponsored by the IEEE Computer Society, IEEE Fault-Tolerant Computing Technical Committee and IEEE Test Technology Technical Council.

Over the last 27 years, DFT has served as an international forum for research in the field of defect and fault tolerance in VLSI systems inclusive of emerging technologies. DFT serves as a forum for both academic and industrial research enabling collaboration and mutual progress. The topic of interests spans manufacturing sources of defects and their impact on design, manufacturing, test, system reliability and availability including design and manufacturing methods to mitigate the impact of defects.

This year the symposium features 30 paper and 20 poster presentations with authors hailing from 22 different countries and two keynote presentations. The opening keynote speaker is Prof. Josep Torrellas of the University of Illinois, Urbana-Champaign. His talk is titled Tackling Parameter Variation from an Architectural Perspective. Prof. Neeraj Suri of the Technical University of Darmstadt will deliver the keynote on the second day of the conference. His talk is titled Quo Vadis Diagnosis: A Systems View.

This year the conference is co-located with two workshops Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN) and Trustworthy Manufacturing and Utilization of Secure Devices (TRUDEVICE) based on European Union sponsored projects. These workshops will be open to all participants. The events will be capped with a full-day of social program.

Joint Open Forum: Two of the European Cooperation in Science and Technology (COST) projects MEDIAN and TRUDEVICE focus on aspects related to reliability of future digital systems and hardware security to combat semiconductor device counterfeiting, theft of service and tampering—the topics that are also of interest to the DFT community. This year, a joint Open Forum will be held on Sep. 30, 2014 to provide an environment for young researchers to discuss problems, common practices, and recent findings.

Full Day Social Event: The third day will be completely devoted to a social event, a very good opportunity of building social interaction between the attendees. The event will consist in a visit to Volendam a popular tourist attraction in the Netherlands, well known for its old fishing boats and the traditional clothing still worn by some residents.

An event of this nature and dimension is only possible due to contributions of many individuals and institutions. These include technical contribution of the authors, the constructive feedback from the reviewers and session chairs who moderate the discussions and keep the schedule on track. We thank them all for their contributions. The program will not be possible without the tireless service of the local organizers and chairs for finance, publication and publicity. We express our gratitude to all of them. Finally, we thank the public and private sponsors of this event.

We hope that you will find DFT 2014 rewarding and exciting. We wish you all a productive and enjoyable stay in Amsterdam and hope that you will continue to make DFT a success through technical participation, assisting in its organization, and providing feedback to make it even better.

Welcome to Amsterdam!

General Co-Chairs

Marco Ottavi

University of Rome “Tor Vergata”, Italy

Said Hamdioui

TU Delft, Netherlands

Program Co-Chairs

Sandip Kundu

*University of Massachusetts Amherst,
USA*

Salvatore Pontarelli

CNIT, Italy

Committees

General Co-Chairs

Said Hamdioui, *Delft University of Technology, Netherlands*

Marco Ottavi, *University of Rome “Tor Vergata”, Italy*

Program Co-Chairs

Sandip Kundu, *University of Massachusetts, Amherst, USA*

Salvatore Pontarelli, *CNIT, Italy*

Industrial Liasons

Prashant Joshi, *Intel, U.S.A.*

Publicity Chair

Antonio Miele, *Politecnico di Milano, Italy*

Publication Chair

Qiaoyan Yu, *University of New Hampshire, U.S.A.*

Technical Program Committee

P. Ampadu, *University of Rochester*

L. Anghel, *TIMA*

C. Bolchini, *Politecnico di Milano*

G. Chapman, *Simon Fraser University*

L. Chen, *University of Saskatchewan*

Y. Choi, *Hongik University*

R. Cideciyan, *IBM*

A. Cristal, *BSC*

A. Daniel, *Intel*

S. Das, *ARM*

L. Dilillo, *LIRMM*

B. Eklow, *CISCO*

O. Ergin, *TOBB*

A. Evans, *IROC*

M. Fukushi, *Yamaguchi University*

D. Gizopoulos, *University of Athens*

J. Han, *University of Alberta*

C. Huang, *Nat’l Tsing Hua University*

N. Jha, *Princeton*

W. Jone, *University of Cincinnati*

N. Karimi, *NY Poly*

R. Karri, *NY Poly*

Y. Kim, *Northeastern University*

I. Koren, *UMASS Amherst*

L. Lastras, *IBM*

R. Leveugle, *TIMA*

X. Li, *Chinese Academy of Science*

H. Li, *Chinese Academy of Science*

F. Lombardi, *Northeastern University*

C. Metra, *University of Bologna*

M. Michael, *University of Cyprus*

A. Miele, *Politecnico di Milano*

M. Mozaffari Kermani, *Rochester Inst. Tech.*

K. Namba, *Chiba University*

N. Nicolici, *McMaster University*

N. Park, *Oklahoma State University*

A. Paschalis, *University of Athens*

Z. Peng, *Linkoping University*

W. Pleskacz, *Warsaw U. T.*

I. Pomeranz, *Purdue University*

S. Reddy, *University of Iowa*

P. Reviriego, *University of Nebraska*

D. Rossi, *University of Bologna*

F. Salice, *Politecnico di Milano*

D. Sciuto, *Politecnico di Milano*

O. Sinanoglu, *N. Y. U. Abu Dhabi*

V. Sridharan, *AMD*

M. Tehranipoor, *U. Connecticut*

J. Teixeira, *Técnica de Lisboa*

C. Thibeault, *Ecole de Tech.*

N. Toubia, *Univ. Texas at Austin*

S. Tragoudas, *S. Illinois U. Carbondale*

M. Violante, *Politecnico di Torino*

L. Wang, *University of Connecticut*

X. Wen, *Kyushu Inst. Tech.*

D. Xiang, *Tsinghua University*

Q. Yu, *University of New Hampshire*

Keynote Talks

Title	Tackling Parameter Variation from an Architectural Perspective
Speaker Name	Josep Torrellas

Abstract

Dealing with parameter variation in a cost-effective manner is one of the main challenges faced by design and test teams • especially when supply voltages are reduced for extreme energy efficiency. This challenge is best addressed at multiple levels. This talk presents some of the approaches that are useful at the architecture level. I will also describe the implications on other layers of the computing stack, and promising future directions of this field.

Biography

Josep Torrellas is a Professor of Computer Science and Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign. He is a Fellow of IEEE and ACM. He is the Director of the Center for Programmable Extreme-Scale Computing, a center funded by DARPA, DOE, and NSF that focuses on architectures for extreme energy and power efficiency. He also directs the Intel-Illinois Parallelism Center (I2PC), a center created by Intel to advance parallel computing in clients. He has made contributions to parallel computer architecture in the areas of shared memory multiprocessor organizations, cache hierarchies and coherence protocols, thread-level speculation, and hardware and software reliability. He has a Ph.D. from Stanford University. Other professional details appear at <http://iacoma.cs.uiuc.edu/~torrellas>

Title	Quo Vadis Diagnosis: A Systems View
Speaker Name	Neeraj Suri

Abstract

Progressing from processor level diagnosis to systems level diagnosis entails a perspective change on specification of the faults to diagnose as well as on the underlying diagnostic approaches. The talk focuses on fault diagnosis in distributed systems discussing the range of diagnosis mechanisms including the tuning of parameters to result in effective diagnosis.

Biography

Suri is the TUD Chair Professor of "Dependable Systems and Software" at TU Darmstadt, Germany and also affiliated with the Univ. of Texas at Austin. Following his PhD at the Univ. of Massachusetts at Amherst, he has held both industry and academic positions at Allied-Signal/Honeywell Research, Boston Univ., Saab Endowed Chair Professor, and also receiving trans-national funding from the EC, German DFG/BMBF/DAAD, SSF/VINNOVA, US-NSF/DARPA/ONR/AFOSR, NASA, Microsoft, IBM, Hitachi, Saab, Volvo, Daimler, GM and others. He is a recipient of the NSF CAREER award, as well as Microsoft and IBM Faculty Awards. Suri's professional services span associate Editor-in-Chief for the IEEE Trans. on Dependable and Secure Computing, editorial boards for IEEE Trans. on SW Engg., IEEE TPDS, ACM Computing Surveys, IEEE Security & Privacy and many others. He has been the PC-chair of the full spectrum of dependability conferences: DSN, ICDCS, SRDS, HASE, ISAS, DATE, WORDS, RAF and SmartComputing among others. He serves on advisory boards for Microsoft (Trustworthy Computing Academic Advisory Board, Strategy Advisor for MSR-ATL's) and multiple other US/EU/Asia industry and university advisory boards. Suri chaired the IEEE Technical Committee on Dependability and Fault Tolerance, and it's Steering Committee. Other professional details appear at <http://www.deeds.informatik.tu-darmstadt.de/suri>

Technical Papers

Session 1	Memories
Date/Time	Wednesday, October 1, 2014 / 10:20 AM – 11:20 AM
Chair	Cecilia Metra , <i>Università di Bologna</i>

- **Triggering Trojans in SRAM Circuits with X-Propagation** **pg. 1**
Senwen Kan and Jennifer Dworak
- **Characterization of Data Retention Faults in DRAM Devices** **pg. 9**
Angelo Bacchini, Marco Rovatti, Gianluca Furano and Marco Ottavi
- **Characterizing Soft Error Vulnerability of Cache Coherence Protocols for Chip-Multiprocessors** **pg. 15**
Chuanlei Zheng and Shuai Wang

Session 2	Self Testing
Date/Time	Wednesday, October 1, 2014 / 11:30 AM – 12:30 PM
Chair	Maria Michael , <i>University of Cyprus</i>

- **Power Droop Reduction During Logic BIST of Sequential ICs with Launch-On-Shift Scan** **pg. 21**
Martin Omaña, Daniele Rossi, Edda Beniamino, Cecilia Metra, Chandra Tirumurti and Rajesh Galivanche
- **Diagnostic Self-Test for Dynamically Scheduled Superscalar Processors Based on Reconfiguration Techniques for Handling Permanent Faults** **pg. 27**
Mario Schölzel, Tobias Koal and Heinrich T. Vierhaus
- **Exploration of System Availability During Software-Based Self-Testing in Many-Core Systems under Test Latency Constraints** **pg. 33**
Michael Skitsas, Chrysostomos Nicopoulos and Maria Michael

Session 3	Security and Fault Tolerance
Date/Time	Wednesday, October 1, 2014 / 02:00 PM – 03:20 PM
Chair	Prashant Joshi

- **Protecting Cryptographic Hardware Against Malicious Attacks by Nonlinear Robust codes** **pg. 40**
Victor Tomashevich, Yaara Neumeier, Raghavan Kumar, Osnat Keren and Ilia Polian
- **CSST: Preventing Distribution of Unlicensed and Rejected ICs by Untrusted Foundry and Assembly** **pg. 46**
Md. Tauhidur Rahman, Domenic Forte, Qihang Shi, Gustavo Contreras and Mohammad Tehranipoor
- **Reusing the IEEE 1500 Design for Test Infrastructure for Security Monitoring of Systems-on-Chip** **pg. 52**
Jerry Backer, David Hély and Ramesh Karri
- **Security Methods in Fault Tolerant Modified Line Graph based Networks** **pg. 57**
Prashant Joshi and Said Hamdioui

Session 4	Emerging technologies
Date/Time	Wednesday, October 1, 2014 / 03:50 PM – 05:30 PM
Chair	Glenn Chapman , <i>Simon Fraser University</i>

- 🔊 **A System-level Scheme for Resistance Drift Tolerance of a Multilevel Phase Change Memory** **pg. 63**
Pilin Junsangsri, Jie Han and Fabrizio Lombardi
- 🔊 **Designs and Analysis of Non-Volatile Memory Cells for Single Event Upset (SEU) Tolerance** **pg. 69**
Fabrizio Lombardi, Wei Wei and Kazuteru Namba
- 🔊 **Reliability Estimation at Block-Level Granularity of Spin-Transfer-Torque MRAMs** **pg. 75**
Marco Indaco, Elena Vatajelu, Stefano Di Carlo, Paolo Prinetto, Rosa Rodriguez-Montanes and Joan Figueras
- 🔊 **Oxide based Resistive RAM: ON/OFF Resistance Analysis versus Circuit Variability** **pg. 81**
Hassen Aziza, Haithem Ayari, Santhosh Onkaraiah, Mathieu Moreau, Jean-Michel Portal and Marc Bocquet
- 🔊 **Using Memristor State Change Behavior to Identify Faults in Photovoltaic Arrays** **pg. 86**
Jimson Mathew, Yuanfan Yang, Marco Ottavi and Prof. Dhiraj K Pradhan

Session 5	Network on Chip
Date/Time	Thursday, October 2, 2014 / 10:20 AM – 11:20 AM
Chair	Cristiana Bolchini , <i>Politecnico di Milano</i>

- 🔊 **TSV-to-TSV Inductive Coupling-Aware Coding Scheme for 3D Network-on-Chip** **pg. 92**
Ashkan Eghbal, Pooria Yaghini, Siavash S. Yazdi and Nader Bagherzadeh
- 🔊 **Rescuing Healthy Cores Against Disabled Routers** **pg. 98**
Masoumeh Ebrahimi, Wang Junshi, Letian Huang, Masoud Daneshtalab and Axel Jantsch
- 🔊 **Fault Tolerant and Highly Adaptive Routing for 2D NoCs** **pg. 104**
Manoj Kumar, Vijay Laxmi, Manoj Gaur, Masoud Daneshtalab, Masoumeh Ebrahimi and Mark Zwolinski

Session 6	Sensors
Date/Time	Thursday, October 2, 2014 / 11:30 AM – 12:30 PM
Chair	Fabrizio Lombardi , <i>Northeastern University</i>

- 🔊 **Performance Sensor for Tolerance and Predictive Detection of Delay-Faults** **pg. 110**
Jorge Semião, André Romão, David Saraiva, Carlos Leong, Marcelino Santos, Isabel Teixeira and Paulo Teixeira
- 🔊 **Improved Correction for Hot Pixels in Digital Imagers** **pg. 116**
Glenn Chapman, Rohit Thomas, Rahul Thomas, Israel Koren and Zahava Koren
- 🔊 **Diagnosis of Segment Delay Defects with Current Sensing** **pg. 122**
Wisam Aljoubouri, Ahish Somashekar, Themistoklis Haniotakis and Spyros Tragoudas

Session 7	Analysis and Synthesis of Resilient Systems
Date/Time	Thursday, October 2, 2014 / 02:00 PM – 03:20 PM
Chair	Spyros Tragoudas , <i>Southern Illinois University</i>








- **A Scheduling Algorithm in Datapath Synthesis for Long Duration Transient Fault Tolerance** **pg. 128**
Tsuyoshi Iwagaki, Tatsuya Nakaso, Ryoko Ohkubo, Hideyuki Ichihara and Tomoo Inoue
- **Artificial Intelligence Based Task Mapping and Pipelined Scheduling for Checkpointing on Real Time Systems with Imperfect Fault Detection** **pg. 134**
Anup Das, Akash Kumar and Bharadwaj Veeravalli
- **A Probabilistic Analysis of Resilient Reconfigurable Designs** **pg. 141**
Alirad Malek, Stavros Tzilis, Danish Anis Khan, Ioannis Sourdis, Georgios Smaragdos and Christos Strydis
- **Domino Effect Protection on Dataflow Error Detection and Recovery** **pg. 147**
Tiago A. O. Alves, Leandro A. J. Marzulo, Sandip Kundu and Felipe M. G. França

Session 8	Fault Tolerance in FPGA devices
Date/Time	Thursday, October 2, 2014 / 03:50 PM – 05:30 PM
Chair	Bill Eklow , <i>Cisco Systems</i>

- **Decreasing FIT with Diverse Triple Modular Redundancy in SRAM-based FPGAs** **pg. 153**
Lucas Antunes Tambara, Fernanda Kastensmidt, Paolo Rech and Christopher Frost
- **A Fault Injection Methodology and Infrastructure for Fast Single Event Upsets Emulation on Xilinx SRAM-based FPGAs** **pg. 159**
Stefano Di Carlo, Paolo Prinetto, Daniele Rolfo and Pascal Trotta
- **Design and implementation of a Self-Healing Processor on SRAM-based FPGAs** **pg. 165**
Alexandros Vavousis, Mihalis Psarakis, Cristiana Bolchini and Antonio Miele
- **Aging Analysis for Recycled FPGA Detection** **pg. 171**
Halit Dogan, Domenic Forte and Mark Tehranipoor
- **Analytic Reliability Evaluation for Fault-Tolerant Circuit Structures on FPGAs** **pg. 177**
Jahanzeb Anwer and Marco Platzner

Poster Session I

- **Estimating the Effect of Single-Event Upsets on Microprocessors** **pg. 185**
Cristian Constantinescu, Srini Krishnamoorthy and Tuyen Nguyen
- **Unifying Scan Compression** **pg. 191**
Swapnil Bahl, Shray Khullar, Shreyans Rungta, Rohit Kapur, Anshuman Chandra, Salvatore Talluto, Pramod Notiyath and Ajay Rajagopalan
- **Exploiting Intel TSX for Fault-Tolerant Execution in Safety-Critical Systems** **pg. 197**
Florian Haas, Sebastian Weis, Theo Ungerer and Stefan Metzloff

- 
Exploiting Dynamic Partial Reconfiguration for On-Line On-Demand Testing of Permanent Faults in Reconfigurable Systems **pg. 203**
Domenico Sorrenti, Dario Cozzi, Sebastian Korf, Luca Cassano, Jens Hagemeyer, Mario Porrman and Cinzia Bernardeschi
- 
GPGPUs ECC Efficiency and Efficacy **pg. 209**
Daniel Alfonso Gonçalves De Oliveira, Paolo Rech, Laércio L. Pilla, Philippe Navaux and Luigi Carro
- 
A Runtime Manager for Gracefully Degrading SoCs **pg. 216**
Stavros Tzilis and Ioannis Sourdis
- 
A Built-In Calibration System with A Reduced FFT Engine for Linearity Optimization of Low Power LNA **pg. 222**
Yongsuk Choi, Chun-Hsiang Chang, In-Seok Jung, Marvin Onabajo and Yong-Bin Kim
- 
A Data Recomputation Approach for Reliability Improvement of Scratchpad Memory in Embedded Systems **pg. 228**
Hossein Sayadi, Hamed Farbeh, Amir Mahdi Hosseini Monazzah and Seyed Ghassem Miremadi
- 
Shortest Path Reduction in a Class of Uniform Fault Tolerant Networks **pg. 234**
Prashant Joshi and Said Hamdioui
- 
SAM: A Comprehensive Mechanism for Accessing Embedded Sensors in Modern SoCs **pg. 240**
Miao He and Mohammad Tehranipoor

Poster Session II

- 
Machine Learning-based Techniques for Board-level Incremental Functional Diagnosis: a Comparative Analysis **pg. 246**
Cristiana Bolchini and Luca Cassano
- 
A Heuristic Path Selection Method for Small Delay Defects Test **pg. 252**
Paniz Foroutan, Mehdi Kamal and Zainalabedin Navabi
- 
Towards an Adaptable bit-width NMR Voter for Multiple Error Masking **pg. 258**
Thiago Berticelli Lo, Fernanda Lima Kastensmidt and Antonio Carlos Beck
- 
Automated Formal Approach for Debugging Dividers Using Dynamic Specification **pg. 264**
Mohammad-Hashem Haghbayan, Bijan Alizadeh, Amir-Mohammad Rahmani, Pasi Liljeberg and Hannu Tenhunen
- 
Energy-Efficient Concurrent Testing Approach for Many-Core Systems in the Dark Silicon Age **pg. 270**
Mohammad-Hashem Haghbayan, Amir-Mohammad Rahmani, Pasi Liljeberg, Juha Plosila and Hannu Tenhunen
- 
A 12-bit 32MS/s SAR ADC Using Built-in Self Calibration Technique To Minimize Capacitor Mismatch **pg. 276**
In-Seok Jung and Yong-Bin Kim
- 
Fault Injection in the Process Descriptor of a Unix-based Operating System **pg. 281**
Alejandro Velasco, Bartolomeo Montrucchio and Maurizio Rebaudengo
- 
An Instance-based SER Analysis in the Presence of PVT Variations **pg. 287**
Bahar Farahani and Saeed Safari

- **Preemptive Multi-Bit JTAG Testing with Reconfigurable Infrastructure** **pg. 293**
Shahrzad Keshavarz, Amirreza Nekooei and Zainalabedin Navabi
- **On the in-Field Functional Testing of Decode Units in Pipelined Embedded Processors** **pg. 299**
Paolo Bernardi, Riccardo Cantoro, Lyl Ciganda, Ernesto Sanchez, Matteo Sonza Reorda, Sergio De Luca, Renato Meregalli and Alessandro Sansonetti