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DCAS 2014 – Detailed Conference Program (Technical Paper Presentation Tracks)

Track-1: Analog and Mixed Signal

2:00-5:00, Sunday, Oct. 12, TI Auditorium (ECSS-2.102) Session Chair: Sidharth Balasubramanian

1.1	2:00	A Loop-breaking method for the simulation of feedback circuits using a VCVS- Terminated Subnetwork Model 1 Howard Russell, Ronald Carter, Alan Davis (University of Texas Arlington)
1.2	2:04	28 nm Charge Sensitive Preamplifier Using 1 G Ohm Dual PMOS Feedback Resistor Operating in the Weak Inversion Region 5 Mahmoud Hassan, Hazem W. Marar (Princess Sumaya University for Technology, Jordan)
1.3	2:08	A 14-b, 0.1ps Resolution Coarse-Fine Time-to-Digital Converter in 45 nm CMOS 8 Huihua Huang, Carl Sechen (University of Texas at Dallas)
1.4	2:12	A Dual Positive Feedback Three-Stage Low Noise Amplifier 12 Majid Jalalifar, Gyung-Su Byun (Southern Methodist University)
1.5	2:16	A Low-Voltage, Process and Temperature Compensated Ring VCO Design 16 Wu, Guoying, Ping Gui, Kexu Sun, Shita Guo, Tao Zhang, Tianzuo Xi (SMU)
	2:30 - 3:00	Break / Poster Session
		CMCC investor based welfage and summer references in short showed
1.6	3:00	CMOS inverter-based voltage and current references in short channel technologies 20 Raghunandan K.R., Viswanathan T.R. (University of Texas at Austin)
1.6 1.7	3:00 3:20	technologies20Raghunandan K.R., Viswanathan T.R. (University of Texas at Austin)Predicting ADC: A New Approach for Low Power ADC Design24
		technologies 20 Raghunandan K.R., Viswanathan T.R. (University of Texas at Austin)
1.7	3:20	 technologies 20 Raghunandan K.R., Viswanathan T.R. (University of Texas at Austin) Predicting ADC: A New Approach for Low Power ADC Design 24 Nicholas Wood (UT Dallas), Nan Sun (UT Austin) Variation Resilient High Performance and Low Voltage Single Ended Sense Amplifier 28

Track-2: High Performance and Energy-efficient Digital

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		Andreas Emeretlis, Vassileios Kelefouras, George Theodoridis (University of Patras), George - Othon Glentis (University of Peloponnese, Greece)	
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		Girish Ramanand Deshpande, Dinesh Bhatia (University of Texas at Dallas)	
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2.6 2.7		Radix-2 ^h Online Floating Point Multipliers 60 Georgina Binoy Joseph (KCG College of Technology, India), Devanathan R.	
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Track-5: Process and Technology

2:00-5:00, Sunday, Oct. 12, ECSS-2.415 Session Chair: Andrew Marshall

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Yiyan Li, Hongzhong Li, and R. Jacob Baker (University of Nevada, Las Vegas)