

2014 IEEE/ACM International Conference on Computer-Aided Design

(ICCAD 2014)

**San Jose, California, USA
2-6 November 2014**



**IEEE Catalog Number: CFP14CAD-POD
ISBN: 978-1-4799-6279-2**

TABLE OF CONTENTS

Session 1-A Enhancing Correctness of Advanced Design

Moderator(s): Vijay Sundararajan – Broadcom Corporation

Jie-Hong (Roland) Jiang – National Taiwan University

- 1-A.1 Automated Detection and Verification of Parity-Protected Memory Elements** 1
Eli Arbel, IBM Corporation; Shlomit Koyfman, IBM Corporation; Prabhakar Kudva, IBM T.J. Watson Research Center; Shiri Moran, IBM Corporation
- 1-A.2 Validating Direct Memory Access Interfaces with Conformance Checking** 9
Li Lei, Portland State University; Kai Cong, Portland State University; Zhenkun Yang, Portland State University; Fei Xie, Portland State University
- 1-A.3 Data-Parallel Simulation for Fast and Accurate Timing Validation of CMOS Circuits** 17
Eric Schneider, University of Stuttgart; Stefan Holst, Kyushu Institute of Technology; Xiaqing Wen, Kyushu Institute of Technology; Hans-Joachim Wunderlich, University of Stuttgart

Session 1-B CAD for Next-Generation Vehicles

Moderator(s): Wenchao Li – SRI International

Armin Wasicek – University of California, Berkeley

- 1-B.1 Security-Aware Mapping for TDMA-Based Real-Time Distributed Systems** 24
Chung-Wei Lin, University of California, Berkeley; Qi Zhu, University of California, Riverside; Alberto Sangiovanni-Vincentelli, University of California, Berkeley
- 1-B.2 Reinforcement Learning based Power Management for Hybrid Electric Vehicles** 32
Xue Lin, University of Southern California; Yanzhi Wang, University of Southern California; Paul Bogdan, University of Southern California; Naehyuck Chang, Korea Advanced Institute of Science and Technology; Massoud Pedram, University of Southern California
- 1-B.3 Functional Modeling Compiler for System-Level Design of Automotive Cyber-Physical Systems** 39
Arquimedes Canedo, Siemens Corporation; Jiang Wan, University of California, Irvine; Mohammad Abdullah Al Faruque, University of California, Irvine

Session 1-C Emerging Reconfigurable Array Technologies

Moderator(s): Dimin Niu – Samsung Research America

- 1-C.1 BDD-Based Synthesis of Reconfigurable Single-Electron Transistor Arrays** 47
Zheng Zhao, Shanghai Jiao Tong University; Chian-Wei Liu, National Tsing Hua University; Chun-Yao Wang, National Tsing Hua University; Weikang Qian, Shanghai Jiao Tong University
- 1-C.2 Architecting 3D Vertical Resistive Memory for Next-Generation Storage Systems** 55
Cong Xu, Pennsylvania State University; Pai-Yu Chen, Arizona State University; Dimin Niu, Pennsylvania State University; Yang Zheng, Pennsylvania State University; Shimeng Yu, Arizona State University; Yuan Xie, Pennsylvania State University

1-C.3	Reduction and IR-drop Compensations Techniques for Reliable Neuromorphic Computing Systems	63
	<i>Beiyue Liu, University of Pittsburgh; Hai Li, University of Pittsburgh; Yiran Chen, University of Pittsburgh; Xin Li, Carnegie Mellon University; Tingwen Huang, Texas A&M University; Qing Wu, Air Force Research Lab; Mark Barnell, Air Force Research Lab</i>	
 Session 1-D Challenges and Techniques for High Level Design		
Moderator(s): Umit Ogras – Arizona State University		
Organizer(s): Frank Liu – IBM Corporation		
1-D.1	Application Driven High Level Design in the Era of Heterogeneous Computing	71
	<i>Ruchir Puri, IBM T.J. Watson Research Center</i>	
1-D.2	High Level Design for Wearables and IoT	72
	<i>Yatin Hoskote, Intel Corporation; Ilya Klotchkov, Intel Corporation</i>	
1-D.3	Towards a Standard Flow for System Level Power Modeling	73
	<i>Nagu Dhanwada, IBM Corporation; Rhett Davis, North Carolina State University; Jerry Frenkil, Silicon Integration Initiative, Inc.</i>	
 Session 2-A Adaptive Designs in Computing, Power Management and Communication for Low-Power Circuits and Systems with Ultra-Wide Dynamic Ranges		
Moderator(s): Arijit Raychowdhury – Georgia Institute of Technology		
Shreyas Sen – Intel Corporation		
2-A.1	The Role of Adaptation and Resiliency in Computation and Power Management	74
	<i>Arijit Raychowdhury, Georgia Institute of Technology; Saad Bin Nasir, Georgia Institute of Technology; Samantak Gangopadhyay, Georgia Institute of Technology</i>	
2-A.2	Channel-Adaptive Zero-Margin & Process-Adaptive Self-Healing Communication Circuits/Systems	80
	<i>Shreyas Sen, Intel Corporation</i>	
 Session 2-B Design, Modeling and Tools for Video Analytics using Emerging Devices		
Moderator(s): Vijaykrishnan Narayanan – Pennsylvania State University		
2-B.3	Modeling Oscillator Arrays for Video Analytic Applications	86
	<i>Yan Fang, University of Pittsburgh; Victor V. Yashin, University of Pittsburgh; Andrew J. Seel, University of Pittsburgh; Brandon Jennings, University of Pittsburgh; Reggie Barnett, University of Pittsburgh; Donald M. Chiarulli, University of Pittsburgh; Steven P. Levitan, University of Pittsburgh</i>	
2-B.4	Cellular Neural Networks for Image Analysis using Steep Slope Devices	92
	<i>Indranil Palit, University of Notre Dame; Qiuwen Lou, University of Notre Dame; Michael Niemier, University of Notre Dame; Behnam Sedighi, University of Notre Dame; Joseph Nahas, University of Notre Dame; X. Sharon Hu, University of Notre Dame</i>	
2-B.5	A Hardware Accelerated Multilevel Visual Classifier for Embedded Visual-Assist Systems	96
	<i>Matthew Cotter, Pennsylvania State University; Siddarth Advani, Pennsylvania State University; Jack Sampson, Pennsylvania State University; Kevin Irick, SiliconScapes LLC; Vijaykrishnan Narayanan, Pennsylvania State University</i>	

Session 2-C Patterns and Placement

Moderator(s): Rani Ghaida – GLOBALFOUNDRIES

- 2-C.1 DRC-Based Hotspot Detection Considering Edge Tolerance and Incomplete Specification**..... 101
Yen-Ting Yu, National Chiao Tung University; Iris Hui-Ru Jiang, National Chiao Tung University; Yumin Zhang, Synopsys, Inc.; Charles Chang, Synopsys, Inc.
- 2-C.2 Triple Patterning Lithography Aware Optimization for Standard Cell based Design** 108
Jian Kuang, Chinese University of Hong Kong; Wing-Kai Chow, Chinese University of Hong Kong; Evangeline F.Y. Young, Chinese University of Hong Kong
- 2-C.3 Triple Patterning Aware Detailed Placement with Constrained Pattern Assignment** 116
Haitong Tian, University of Illinois at Urbana-Champaign; Yuelin Du, University of Illinois at Urbana-Champaign; Hongbo Zhang, Synopsys, Inc.; Zigang Xiao, University of Illinois at Urbana-Champaign; Martin D.F. Wong, University of Illinois at Urbana-Champaign
- 2-C.4 Sub-20 nm Design Technology Co-Optimization for Standard Cell Logic**..... 124
Kaushik Vaidyanathan, Carnegie Mellon University; Lars Liebmann, IBM Corporation; Andrzej Strojwas, Carnegie Mellon University; Larry Pileggi, Carnegie Mellon University

Session 2-D Energy, Performance and Security for Embedded Systems.

Moderator(s): Yang Ge – Broadcom Corporation

- 2-D.1 Energy-Efficient Architecture for Advanced Video Memory**..... 132
Felipe Sampaio, University Federal do Rio Grande do Sul; Muhammad Shafique, Karlsruhe Institute of Technology; Bruno Zatt, University Federal de Pelotas; Sergio Bampi, University Federal do Rio Grande do Sul; Jörg Henkel, Karlsruhe Institute of Technology
- 2-D.2 Compaction-Free Compressed Cache for High Performance Multi-Core System**..... 140
Po-Yang Hsu, National Tsing Hua University; Pei-Lan Lin, National Tsing Hua University; TingTing Hwang, National Tsing Hua University
- 2-D.3 A Non-Volatile Memory based Physically Unclonable Function without Helper Data**..... 148
Wenjie Che, University of New Mexico; Jim Plusquellic, University of New Mexico; Swarup Bhunia, Case Western Reserve University
- 2-D.4 Cryptoraptor: High Throughput Reconfigurable Cryptographic Processor**..... 154
Gokhan Sayilar, University of Texas at Austin; Derek Chiou, Microsoft Research, University of Texas at Austin

Session 3-A Can One SHIELD Integrated Circuits and Systems from Supply Chain Attacks?

Moderator(s): Ramesh Karri – New York University

**Organizer(s): Ramesh Karri – New York University
Farinaz Koushanfar – Rice University**

- 3-A.2 BIST-PUF: Online, Hardware-based Evaluation of Physically Unclonable Circuit Identifiers**..... 162
Siam U. Hussain, Rice University; Sudha Yellapantula, Rice University; Mehrdad Majzoobi, Mesh Motion Inc.; Farinaz Koushanfar, Rice University

3-A.4	Shielding and Securing Integrated Circuits with Sensors	170
	<i>Davood Shahrjerdi, New York University; Jeyavijayan Rajendran, New York University; Siddharth Garg, New York University; Farinaz Koushanfar, Rice University; Ramesh Karri, New York University</i>	
 Session 3-B Smart Energy System: Electric Vehicle, Home, HVAC, Hybrid System and Cybersecurity		
Moderator(s): Tsung-Yi Ho – National Chiao Tung University		
Organizer(s): Shiyun Hu – Michigan Technological University		
3-B.1	Power Consumption Characterization, Modeling and Estimation of Electric Vehicles	175
	<i>Naehyuck Chang, Korea Advanced Institute of Science and Technology; Donkyu Baek, Korea Advanced Institute of Science and Technology; Jeongmin Hong, Korea Advanced Institute of Science and Technology</i>	
3-B.2	Vulnerability Assessment and Defense Technology for Smart Home Cybersecurity Considering Pricing Cyberattacks	183
	<i>Yang Liu, Michigan Technological University; Shiyun Hu, Michigan Technological University; Tsung-Yi Ho, National Chiao Tung University</i>	
3-B.3	Co-Scheduling of HVAC Control, EV Charging and Battery Usage for Building Energy Efficiency	191
	<i>Tianshu Wei, University of California, Riverside; Qi Zhu, University of California, Riverside; Mehdi Maasoumy, C3 Energy</i>	
3-B.4	Real Time Anomaly Detection in Wide Area Monitoring of Smart Grids	197
	<i>Jie Wu, Missouri University of Science and Technology; Jinjun Xiong, IBM Corporation; Prasenjit Shil, Ameren Corporation; Yiyu Shi, Missouri University of Science and Technology</i>	
 Session 3-C Analysis and Optimization of Timing, Noise, and Power		
Moderator(s): Igor Keller – Cadence Design Systems, Inc.		
Mondira Pant – Intel Corporation		
3-C.1	Variation Aware Optimal Threshold Voltage Computation for On-Chip Noise Sensors	205
	<i>Tao Wang, Missouri University of Science and Technology; Chun Zhang, Missouri University of Science and Technology; Jinjun Xiong, IBM T.J. Watson Research Center; Pei-Wen Luo, Industrial Technology Research Institute; Liang-Chia Cheng, Industrial Technology Research Institute; Yiyu Shi, Missouri University of Science and Technology</i>	
3-C.2	More Effective Power-Gated Circuit Optimization with Multi-Bit Retention Registers	213
	<i>Shu-Hung Lin, National Chung Cheng University; Mark Po-Hung Lin, National Chung Cheng University</i>	
3-C.3	An Efficient Spectral Graph Sparsification Approach to Scalable Reduction of Large Flip-Chip Power Grids	218
	<i>Xueqian Zhao, Michigan Technological University; Zhuo Feng, Michigan Technological University; Cheng Zhuo, Intel Corporation</i>	
3-C.4	Reinforcement Learning based Self-adaptive Voltage-swing Adjustment of 2.5D I/Os for Many-core Microprocessor and Memory Communication	224
	<i>Huang Hantao, Nanyang Technological University; Sai Manoj P.D., Nanyang Technological University; Dongjun Xu, Nanyang Technological University, Xi'an University of Technology; Hao Yu, Nanyang Technological University; Zhigang Hao, MediaTek, Singapore Pte. Ltd.</i>	

Session 3-D What is Behind the Mask?

Moderator(s): *Luigi Capodiceci – GLOBALFOUNDRIES*

Ibrahim (Abe) Elfadel – Masdar Institute of Science and Technology

- 3-D.1 Fast Lithographic Mask Optimization Considering Process Variation**..... 230
Yu-Hsuan Su, National Taiwan University; Yu-Chen Huang, National Taiwan University; Liang-Chun Tsai, National Taiwan University; Yao-Wen Chang, National Taiwan University; Shayak Banerjee, Samsung Accelerator
- 3-D.2 A Fast Process Variation and Pattern Fidelity Aware Mask Optimization Algorithm**..... 238
Ahmed Awad, Tokyo Institute of Technology; Atsushi Takahashi, Tokyo Institute of Technology; Satoshi Tanaka, Toshiba Corporation; Chikaaki Kodama, Toshiba Corporation
- 3-D.3 Benchmarking of Mask Fracturing Heuristics** 246
Tuck Boon Chan, University of California at San Diego; Puneet Gupta, University of California, Los Angeles; Kwangsoo Han, University of California at San Diego; Abde Ali Kagalwalla, University of California, Los Angeles; Andrew B. Kahng, University of California at San Diego; Emile Sahouria, Mentor Graphics Inc.
- 3-D.4 Overlapping-aware Throughput-driven Stencil Planning for E-Beam Lithography** 254
Jian Kuang, Chinese University of Hong Kong; Evangeline F.Y. Young, Chinese University of Hong Kong

Session 4-A Detection & Prevention of IC Security Threats

Moderator(s): *Celia Merzbacher – Semiconductor Research Corporation*

Sandeep Goel – Taiwan Semiconductor Manufacturing Co., Ltd.

- 4-A.1 Protecting Integrated Circuits from Piracy with Test-Aware Logic Locking**..... 262
Stephen M. Plaza, Howard Hughes Medical Institute; Igor L. Markov, University of Michigan
- 4-A.2 Hardware Obfuscation using PUF-Based Logic** 270
James B. Wendt, University of California, Los Angeles; Miodrag Potkonjak, University of California, Los Angeles
- 4-A.3 On Trojan Side Channel Design and Identification** 278
Jie Zhang, Chinese University of Hong Kong; Guantong Su, Tsinghua University; Yannan Liu, Chinese University of Hong Kong; Lingxiao Wei, Chinese University of Hong Kong; Feng Yuan, Chinese University of Hong Kong; Guoqiang Bai, Tsinghua University; Qiang Xu, Chinese University of Hong Kong

Session 4-B Design Automation for Biochemistry Synthesis on a Digital Microfluidic Lab-on-a-Chip

Moderator(s): *Krishnendu Chakrabarty – Duke University*

Organizer(s): *Krishnendu Chakrabarty – Duke University*

Bhargab B. Bhattacharya – Indian Statistical Institute

Ansuman Banerjee – Indian Statistical Institute

- 4-B.1 Design Automation for Biochemistry Synthesis on a Digital Microfluidic Lab-on-a-Chip** 286
Krishnendu Chakrabarty, Duke University; Bhargab B. Bhattacharya, Indian Statistical Institute; Ansuman Banerjee, Indian Statistical Institute

Session 4-C Runtime Optimizations for Emerging Memory and On-Chip Systems

Moderator(s): *Unit Ogras – Arizona State University*

Timothy Kam – Intel Corporation

- 4-C.1 High-Radix On-Chip Networks with Low-Radix Routers**..... 289
Animesh Jain, University of Michigan; Ritesh Parikh, University of Michigan; Valeria Bertacco, University of Michigan
- 4-C.2 Data-Aware DRAM Refresh to Squeeze the Margin of Retention Time in Hybrid Memory Cube** 295
Yinhe Han, Chinese Academy of Sciences; Ying Wang, Chinese Academy of Sciences; Huawei Li, Chinese Academy of Sciences; Xiaowei Li, Chinese Academy of Sciences
- 4-C.3 Using Multi-Level Cell STT-RAM for Fast and Energy-Efficient Local Checkpointing**..... 301
Ping Chi, Pennsylvania State University; Cong Xu, Pennsylvania State University; Tao Zhang, NVIDIA Corporation; Xiangyu Dong, Qualcomm Technologies, Inc.; Yuan Xie, Pennsylvania State University

Session 4-D Noise and Variability

Moderator(s): *Eric Keiter – Sandia National Laboratories*

Chirayu Amin – Intel Corporation

- 4-D.1 Modeling and Analysis of Nonstationary Low-Frequency Noise in Circuit Simulators: Enabling non Monte Carlo Techniques** 309
A. Gokcen Mahmutoglu, Koc University; Alper Demir, Koc University
- 4-D.2 MPME-DP: Multi-Population Moment Estimation via Dirichlet Process for Efficient Validation of Analog/Mixed-Signal Circuits** 316
Manzil Zaheer, Carnegie Mellon University; Xin Li, Carnegie Mellon University; Chenjie Gu, Intel Corporation
- 4-D.3 Fast Statistical Analysis of Rare Circuit Failure Events via Subset Simulation in High-Dimensional Variation Space**..... 324
Shupeng Sun, Carnegie Mellon University; Xin Li, Carnegie Mellon University

Session 5-A Advanced Verification and Diagnosis Techniques

Moderator(s): *Miroslav Velez – Aries Design Automation, LLC*

Rolf Drechsler – University of Bremen

- 5-A.1 Removing Concurrency for Rapid Functional Verification**..... 332
Stephen Longfield, Jr., Cornell University; Rajit Manohar, Cornell University
- 5-A.2 Towards Formal Evaluation and Verification of Probabilistic Design**..... 340
Nian-Ze Lee, National Taiwan University; Jie-Hong R. Jiang, National Taiwan University
- 5-A.3 Silicon Fault Diagnosis using Sequence Interpolation with Backbones** 348
Charlie Shucheng Zhu, Princeton University; Georg Weissenbacher, Vienna University of Technology; Sharad Malik, Princeton University

Session 5-B 2014 CAD Contest

*Moderator(s): Iris Hui-Ru Jiang – National Chiao Tung University
Natarajan Viswanathan – IBM Corporation*

*Organizer(s): Tai-Chen Chen – National Central University
Jin-Fu Li – National Central University*

- 5-B.1 The Overview of 2014 CAD Contest at ICCAD** 356
*Iris Hui-Ru Jiang, National Chiao Tung University; Natarajan Viswanathan, IBM Corporation;
Tai-Chen Chen, National Central University; Jin-Fu Li, National Central University*
- 5-B.2 ICCAD-2014 CAD Contest in Simultaneous CNF Encoder Optimization with SAT Solver
Setting Selection and Benchmark Suite** 357
*Chih-Jen Hsu, Cadence Design Systems, Inc.; Wei-Hsun Lin, Cadence Design Systems, Inc.; Chi-
An Wu, Cadence Design Systems, Inc.; Kei-Yong Khoo, Cadence Design Systems, Inc.*
- 5-B.3 ICCAD-2014 CAD Contest in Incremental Timing-Driven Placement and Benchmark Suite** 361
*Myung-Chul Kim, IBM Corporation; Jin Hu, IBM Corporation; Natarajan Viswanathan, IBM
Corporation*
- 5-B.4 ICCAD-2014 CAD Contest in Design for Manufacturability Flow for Advanced
Semiconductor Nodes and Benchmark Suite** 367
Rasit O. Topaloglu, IBM Corporation

Session 5-C Emerging Applications of Networked Cyberphysical Systems

Moderator(s): Arquimedes Canedo – Siemens Corporation

Shiyan Hu – Michigan Technological University

- 5-C.1 Optimal Offloading Control for a Mobile Device based on a Realistic Battery Model and
Semi-Markov Decision Process** 369
*Shuang Chen, University of Southern California; Yanzhi Wang, University of Southern
California; Massoud Pedram, University of Southern California*
- 5-C.2 A Learning-on-Cloud Power Management Policy for Smart Devices** 376
*Gung-Yu Pan, National Chiao Tung University; Bo-Cheng Charles Lai, National Chiao Tung
University; Sheng-Yen Chen, National Chiao Tung University; Jing-Yang Jou, National Central
University and National Chiao Tung University*
- 5-C.3 Smart Grid Load Balancing Techniques via Simultaneous Switch/Tie-line/Wire
Configurations** 382
*Iris Hui-Ru Jiang, National Chiao Tung University; Gi-Joon Nam, IBM Corporation; Hua-
Yu Chang, National Taiwan University; Sani R. Nassif, Radyalis LLP; Jerry Hayes, IBM
Corporation*

Session 5-D Routing in EDA and Beyond

Moderator(s): Li Li – Synopsys, Inc.

Yih-Lang Li – National Chiao Tung University

- 5-D.1 A Resource-level Parallel Approach for Global-routing-based Routing Congestion
Estimation and a Method to Quantify Estimation Accuracy** 389
*Wen-Hao Liu, Cadence Design Systems, Inc.; Zhen-Yu Peng, National Tsing Hua University;
Ting-Chi Wang, National Tsing Hua University*

5-D.2	MCFRoute: A Detailed Router based on Multi-Commodity Flow Method	397
	<i>Xiaotao Jia, Tsinghua University; Yici Cai, Tsinghua University; Qiang Zhou, Tsinghua University; Gang Chen, Nimbus Automation Technologies; Zhuoyuan Li, Nimbus Automation Technologies; Zuowei Li, Nimbus Automation Technologies</i>	
5-D.3	Exact Routing for Digital Microfluidic Biochips with Temporary Blockages	405
	<i>Oliver Keszocze, University of Bremen; Robert Wille, University of Bremen; Rolf Drechsler, University of Bremen</i>	
Session 6-A	CAD for the Internet of Things	
	<i>Moderator(s): Farinaz Koushanfar – Rice University</i>	
	<i>Organizer(s): Miodrag Potkonjak – University of California, Los Angeles</i>	
6-A.1	Design THINGS for the Internet of Things – An EDA Perspective	411
	<i>Gang Qu, University of Maryland; Lin Yuan, Atoptech, Inc.</i>	
6-A.2	Security of IoT systems: Design Challenges and Opportunities	417
	<i>Teng Xu, University of California, Los Angeles; James B. Wendt, University of California, Los Angeles; Miodrag Potkonjak, University of California, Los Angeles</i>	
6-A.3	Towards a Rich Sensing Stack for IoT Devices	424
	<i>Chenguang Shen, University of California, Los Angeles; Haksoo Choi, University of California, Los Angeles; Supriyo Chakraborty, University of California, Los Angeles; Mani Srivastava, University of California, Los Angeles</i>	
Session 6-B	Full-Chip Electromigration Assessment and System-Level EM Reliability Management	
	<i>Moderator(s): Valeriy Sukharev – Mentor Graphics Corporation</i>	
	<i>Organizer(s): Sheldon Tan – University of California, Riverside</i>	
6-B.1	IR-Drop based Electromigration Assessment: Parametric Failure Chip-Scale Analysis	428
	<i>Valeriy Sukharev, Mentor Graphics Corporation; Xin Huang, University of California, Riverside; Hai-Bao Chen, University of California, Riverside; Sheldon X.-D. Tan, University of California, Riverside</i>	
6-B.2	Lifetime Optimization for Real-Time Embedded Systems Considering Electromigration Effects	434
	<i>Taeyoung Kim, University of California, Riverside; Bowen Zheng, University of California, Riverside; Hai-Bao Chen, University of California, Riverside; Qi Zhu, University of California, Riverside; Valeriy Sukharev, Mentor Graphics Corporation; Sheldon X.-D. Tan, University of California, Riverside</i>	
6-B.3	Accurate Full-Chip Estimation of Power Map, Current Densities and Temperature for EM Assessment	440
	<i>Marko Chew, Mentor Graphics Corporation; Ara Aslyan, Mentor Graphics Corporation; Jun-ho Choy, Mentor Graphics Corporation; Xin Huang, University of California, Riverside</i>	
Session 6-C	Advances in Logic Synthesis	
	<i>Moderator(s): Sergio Bampi – University Federal do Rio Grande do Sul</i>	
	<i>Li-C Wang – University of California, Berkeley</i>	
6-C.1	TonyChopper: A Desynchronization Package	446
	<i>Zhao Wang, University of Texas at Dallas; Xiao He, University of Texas at Dallas; Carl M. Sechen, University of Texas at Dallas</i>	

6-C.2	SuperPUF: Integrating Heterogeneous Physically Unclonable Functions	454
	<i>Michael Wang, University of Michigan; Andrew Yates, University of Michigan; Igor L. Markov, University of Michigan</i>	
6-C.3	Constrained Interpolation for Guided Logic Synthesis	462
	<i>Ana Petkovska, Ecole Polytechnique Fédérale de Lausanne; David Novo, Ecole Polytechnique Fédérale de Lausanne; Alan Mishchenko, University of California, Berkeley; Paolo Ienne, Ecole Polytechnique Fédérale de Lausanne</i>	
6-C.4	Logic Synthesis and a Generalized Notation for Memristor-Realized Material Implication Gates	470
	<i>Anika Raghuvanshi, Portland State University; Marek Perkowski, Portland State University</i>	
 Session 6-D How to Keep Chip Aging at Bay		
Moderator(s): Zhiru Zhang – Cornell University		
Eli Chiprout – Intel Corporation		
6-D.1	Towards Interdependencies of Aging Mechanisms	478
	<i>Hussam Amrouch, Karlsruhe Institute of Technology; Victor M. van Santen, Karlsruhe Institute of Technology; Thomas Ebi, Karlsruhe Institute of Technology; Volker Wenzel, Karlsruhe Institute of Technology; Jörg Henkel, Karlsruhe Institute of Technology</i>	
6-D.2	A Systematic Approach for Analyzing and Optimizing Cell-Internal Signal Electromigration	486
	<i>Gracieli Posser, University Federal do Rio Grande do Sul; Vivek Mishra, University of Minnesota; Palkesh Jain, Texas Instruments, Inc.; Ricardo Reis, University Federal do Rio Grande do Sul; Sachin S. Sapatnekar, University of Minnesota</i>	
6-D.3	ReSCALE: Recalibrating Sensor Circuits for Aging and Lifetime Estimation under BTI	492
	<i>Deepashree Sengupta, University of Minnesota; Sachin S. Sapatnekar, University of Minnesota</i>	
6-D.4	Sensorless Estimation of Global Device-Parameters based on Fmax Testing	498
	<i>Michihiro Shintani, Kyoto University; Takashi Sato, Kyoto University</i>	
 Session 7-A Approximate and Stochastic Circuits		
Moderator(s): Iris Hui-Ru Jiang – National Chiao Tung University		
Sergio Bampi – University Federal do Rio Grande do Sul		
7-A.1	Multi-Level Approximate Logic Synthesis under General Error Constraints	504
	<i>Jin Miao, University of Texas at Austin; Andreas Gerstlauer, University of Texas at Austin; Michael Orshansky, University of Texas at Austin</i>	
7-A.2	On Error Modeling and Analysis of Approximate Adders	511
	<i>Li Li, Synopsys, Inc.; Hai Zhou, Northwestern University</i>	
7-A.3	Generating Multiple Correlated Probabilities for MUX-Based Stochastic Computing Architecture	519
	<i>Yili Ding, Shanghai Jiao Tong University; Yi Wu, Shanghai Jiao Tong University; Weikang Qian, Shanghai Jiao Tong University</i>	

Session 7-B Cool Technologies for Cool Chips

Moderator(s): *Muhammad Shafique – Karlsruhe Institute of Technology*
Ravishankar Rao – Synopsys

- 7-B.1 PowerCool: Simulation of Integrated Microfluidic Power Generation in Bright Silicon MPSoCs**..... 527
Arvind Sridhar, Ecole Polytechnique Fédérale de Lausanne and IBM Corporation; Mohamed M. Sabry, Ecole Polytechnique Fédérale de Lausanne; Patrick Ruch, IBM Corporation; David Aienza, Ecole Polytechnique Fédérale de Lausanne; Bruno Michel, IBM Corporation
- 7-B.2 Workload Dependent Evaluation of Thin-Film Thermoelectric Devices for On-Chip Cooling and Energy Harvesting**..... 535
Sri Harsha Choday, Purdue University; Kon-Woo Kwon, Purdue University; Kaushik Roy, Purdue University
- 7-B.3 Fast and Accurate Emissivity and Absolute Temperature Maps Measurement for Integrated Circuits**..... 542
Hsueh-Ling Yu, Industrial Technology Research Institute; Yih-Lang Li, National Chiao Tung University; Tzu-Yi Liao, Industrial Technology Research Institute; Tianchen Wang, Missouri University of Science and Technology; Yiyu Shi, Missouri University of Science and Technology; Shu-Fei Tsai, Industrial Technology Research Institute

Session 7-C Design and CAD to Enable 3D Integration

Moderator(s): *Siddharth Garg – University of Waterloo*
Hai Li – University of Pittsburgh

- 7-C.1 Efficient Layout Generation and Evaluation of Vertical Channel Devices**..... 550
Wei-Che Wang, University of California, Los Angeles; Puneet Gupta, University of California, Los Angeles
- 7-C.2 Thermal-Aware Synthesis of Integrated Photonic Ring Resonators**..... 557
Christopher Condrat, Calypto Design Systems, Inc.; Priyank Kalla, University of Utah; Steve Blair, University of Utah
- 7-C.3 Full Chip Impact Study of Power Delivery Network Designs in Monolithic 3D ICs**..... 565
Sandeep Kumar Samal, Georgia Institute of Technology; Kambiz Samadi, Qualcomm Technologies, Inc.; Pratyush Kamal, Qualcomm Technologies, Inc.; Yang Du, Qualcomm Technologies, Inc.; Sung Kyu Lim, Georgia Institute of Technology

Session 7-D DFM for Extreme Technology Nodes

Moderator(s): *David Pan – University of Texas at Austin*
Organizer(s): *Frank Liu – IBM Corporation - Austin*

- 7-D.1 Evolving Physical Design Paradigms in the Transition from 20/14 to 10nm Process Technology Nodes**..... 573
Luigi Capodieci, GLOBALFOUNDRIES
- 7-D.2 Design and Manufacturing Process Co-optimization in Nano-Technology**..... 574
Meng-Kai Hsu, Taiwan Semiconductor Manufacturing Co., Ltd.; Nitesh Katta, Taiwan Semiconductor Manufacturing Co., Ltd.; Homer Yen-Hung Lin, Taiwan Semiconductor Manufacturing Co., Ltd.; Keny Tzu-Hen Lin, Taiwan Semiconductor Manufacturing Co., Ltd.; King Ho Tam, Taiwan Semiconductor Manufacturing Co., Ltd.; Chung-Hsing Wang, Taiwan Semiconductor Manufacturing Co., Ltd.

7-D.3	Design and Technology Co-Optimization Near Single-Digit Nodes	582
	<i>Lars W. Liebmann, IBM Corporation; Rasit O. Topaloglu, IBM Corporation</i>	
 Session 8-A Automated and Quality-Driven Requirement Engineering		
Moderator(s): Robert Wille – University of Bremen		
Organizer(s): Robert Wille – University of Bremen		
8-A.1	Automated and Quality-Driven Requirement Engineering	586
	<i>Rolf Drechsler, University of Bremen; Mathias Soeken, University of Bremen; Robert Wille, University of Bremen</i>	
 Session 8-B Pessimism Removal During Timing Analysis		
Moderator(s): Jin Hu – IBM Corporation		
Organizer(s): Jin Hu – IBM Corporation		
<i>Debjit Sinha – IBM Corporation</i>		
<i>Igor Keller – Cadence Design Systems, Inc.</i>		
<i>Chirayu Amin – Intel Corporation</i>		
8-B.1	TAU 2014 Contest on Removing Common Path Pessimism during Timing Analysis	591
	<i>Jin Hu, IBM Corporation; Debjit Sinha, IBM Corporation; Igor Keller, Cadence Design Systems, Inc.</i>	
8-B.2	Common Path Pessimism Removal: An Industry Perspective	592
	<i>Vibhor Garg, Cadence Design Systems, Inc.</i>	
8-B.3	Fast Path-Based Timing Analysis for CPPR	596
	<i>Tsung-Wei Huang, University of Illinois at Urbana-Champaign; Pei-Ci Wu, University of Illinois at Urbana-Champaign; Martin D.F. Wong, University of Illinois at Urbana-Champaign</i>	
8-B.4	iTimerC: Common Path Pessimism Removal using Effective Reduction Methods	600
	<i>Yu-Ming Yang, National Chiao Tung University; Yu-Wei Chang, National Chiao Tung University; Iris Hui-Ru Jiang, National Chiao Tung University</i>	
8-B.5	TKtimer: Fast & Accurate Clock Network Pessimism Removal	606
	<i>Christos Kalonakis, University of Thessaly; Charalampos Antoniadis, University of Thessaly; Panagiotis Giannakou, University of Thessaly; Dimos Dioudis, University of Thessaly; Georgios Pinitas, Delft University of Technology; Georgios Stamoulis, University of Thessaly</i>	
 Session 8-C Emulation, Modeling and Simulation of Analog Systems		
Moderator(s): Jaijeet Roychowdhury – University of California, Berkeley		
Ting Mei – Sandia National Labs		
8-C.1	A Novel Linear Algebra Method for the Determination of Periodic Steady States of Nonlinear Oscillators	611
	<i>Haotian Liu, University of Hong Kong; Kim Batselier, University of Hong Kong; Ngai Wong, University of Hong Kong</i>	
8-C.2	A Unifying and Robust Method for Efficient Envelope-Following Simulation of PWM/PFM DC-DC Converters	618
	<i>Ya Wang, Texas A&M University; Peng Li, Texas A&M University; Suming Lai, Texas A&M University</i>	

8-C.3	Large-Signal MOSFET Modeling using Frequency-Domain Nonlinear System Identification	626
	<i>Moning Zhang, Tsinghua University; Yang Tang, Tsinghua University; Zuo-chang Ye, Tsinghua University</i>	
8-C.4	Pragma-Based Floating-to-Fixed Point Conversion for the Emulation of Analog Behavioral Models	633
	<i>Frank Austin Nothaft, Broadcom Corporation; Luis Fernandez, Broadcom Corporation; Stephen Cefali, Broadcom Corporation; Nishant Shah, Broadcom Corporation; Jacob Rael, Broadcom Corporation; Luke Darnell, Broadcom Corporation</i>	
Session 8-D Advanced Placement		
Moderator(s): Martin D.F. Wong – University of Illinois at Urbana-Champaign		
Ismail Bustany – Mentor Graphics Corporation		
8-D.1	Asynchronous Circuit Placement by Lagrangian Relaxation	641
	<i>Gang Wu, Iowa State University; Tao Lin, Iowa State University; Hsin-Ho Huang, University of Southern California; Chris Chu, Iowa State University; Peter A. Beerel, University of Southern California</i>	
8-D.2	Efficient and Effective Packing and Analytical Placement for Large-Scale Heterogeneous FPGAs	647
	<i>Yu-Chen Chen, National Taiwan University; Sheng-Yen Chen, National Taiwan University; Yao-Wen Chang, National Taiwan University</i>	
8-D.3	A Hierarchical Approach for Generating Regular Floorplans	655
	<i>Javier De San Pedro, University Politècnica de Catalunya; Jordi Cortadella, University Politècnica de Catalunya; Antoni Roca, University Politècnica de Catalunya</i>	
8-D.4	Planning and Placing Power Clamps for Effective CDM Protection	663
	<i>Hsin-Chun Lin, National Chiao Tung University and Global Unichip Corporation; Sean S.-Y. Liu, National Chiao Tung University; Hung-Ming Chen, National Chiao Tung University</i>	
Session 9-A Advances in Debug and Formal Verification		
Moderator(s): Yirng-An Chen – Marvell Semiconductor, Inc.		
Organizer(s): Miroslav Velev – Aries Design Automation, LLC		
9-A.1	On Application of Data Mining in Functional Debug	670
	<i>Kuo-Kai Hsieh, University of California, Santa Barbara; Wen Chen, University of California, Santa Barbara; Li-C. Wang, University of California, Santa Barbara; Jayanta Bhadra, Freescale Semiconductor, Inc.</i>	
9-A.2	Improving the Efficiency of Automated Debugging of Pipelined Microprocessors by Symmetry Breaking in Modular Schemes for Boolean Encoding of Cardinality	676
	<i>Miroslav N. Velev, Aries Design Automation, LLC; Ping Gao, Aries Design Automation, LLC</i>	
9-A.3	Multiple Clock Domain Synchronization in a QBF-Based Verification Environment	684
	<i>Djordje Maksimovic, University of Toronto; Bao Le, University of Toronto; Andreas Veneris, University of Toronto</i>	
9-A.4	Probabilistic Model Checking for Comparative Analysis of Automated Air Traffic Control Systems	690
	<i>Yang Zhao, Microsoft Corporation; Kristin Y. Rozier, NASA Ames Research Center</i>	

Session 9-B Mathematical Methods for Interconnect Modeling and Low Power Design

Moderator(s): *Wenjian Yu – Tsinghua University*

Eli Chiprout – Intel Corporation

- 9-B.1 A Zonotoped Macromodeling for Reachability Verification of Eye-Diagram in High-Speed I/O Links with Jitter** 696
Sai Manoj P.D., Nanyang Technological University; Hao Yu, Nanyang Technological University; Chenji Gu, Intel Corporation; Cheng Zhuo, Intel Corporation
- 9-B.2 Random Walk based Capacitance Extraction for 3D ICs with Cylindrical Inter-Tier-Vias**..... 702
Wenjian Yu, Tsinghua University; Chao Zhang, Tsinghua University; Qing Wang, Tsinghua University; Yiyu Shi, Missouri University of Science and Technology
- 9-B.3 Self-Learning MIMO-RF Receiver Systems: Process Resilient Real-Time Adaptation to Channel Conditions for Low Power Operation** 710
Debashis Banerjee, Georgia Institute of Technology; Barry Muldrey, Georgia Institute of Technology; Shreyas Sen, Intel Corporation; Xian Wang, Georgia Institute of Technology; Abhijit Chatterjee, Georgia Institute of Technology

Session 9-C Software for Management of Parallelism and Data Integrity in Embedded Systems

Moderator(s): *Jose Ayala – Complutense University of Madrid*

- 9-C.1 Multithreaded Pipeline Synthesis for Data-Parallel Kernels**..... 718
Mingxing Tan, Cornell University; Bin Liu, Facebook, Inc.; Steve Dai, Cornell University; Zhiru Zhang, Cornell University
- 9-C.2 Toward Scalable Source Level Accuracy Analysis for Floating-Point to Fixed-Point Conversion**..... 726
Gaël Deest, University of Rennes 1; Tomofumi Yuki, INRIA; Olivier Sentieys, INRIA, University of Rennes 1; Steven Derrien, University of Rennes 1
- 9-C.3 Warranty-Aware Page Management for PCM-Based Embedded Systems** 734
Sheng-Wei Cheng, National Taiwan University; Yu-Fen Chang, National Tsing Hua University; Yuan-Hao Chang, Academia Sinica; Hsin-Wen Wei, Tamkang University; Wei-Kuan Shih, National Tsing Hua University

Session 9-D Clock Network Design and Timing

Moderator(s): *Tao Huang – Synopsys, Inc.*

Rajendra Panda – Oracle

- 9-D.1 Frequency-Centric Resonant Rotary Clock Distribution Network Design**..... 742
Ying Teng, Drexel University; Baris Taskin, Drexel University
- 9-D.2 Opportunistic Through-Silicon-Via Inductor Utilization in LC Resonant Clocks: Concept and Algorithms**..... 750
Umamaheswara Rao Tida, Missouri University of Science and Technology; Varun Mittapalli, Missouri University of Science and Technology; Cheng Zhuo, Intel Corporation; Yiyu Shi, Missouri University of Science and Technology
- 9-D.3 UI-Timer: An Ultra-Fast Clock Network Pessimism Removal Algorithm**..... 758
Tsung-Wei Huang, University of Illinois at Urbana-Champaign; Pei-Ci Wu, University of Illinois at Urbana-Champaign; Martin D.F. Wong, University of Illinois at Urbana-Champaign