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B7P-D-12	Design and Simulation of a Wideband Channelized Transceiver for DRFM Applications Ajinkya Kale, Vijaya Sankara Rao Pasupureddi (International Institute of Information Technology, Hyderabad, India), J Chattopadhyay (Defence Research and Development Organization, India)	(pp. 635–638)

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B7P-D-14 Privacy Preserving Face Recognition in Encrypted Domain

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B7P-D-15 A Note on the Energy-Aware Mapping for NoCs

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B7P-D-16 FPGA Implementation of Type Identifier for Colorectal Endoscopic Images with NBI (pp. 651–654) **Magnification**

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Special Session (C1L-B): Technologies for Innovative Multi-Core **NoC**

C1L-B-01 A Systematic Network-on-Chip Traffic Modeling and Generation Methodology (pp. 675–678)

Zhe Wang (Hong Kong University of Science and Technology, Hong Kong), Weichen Liu (Chongqing University, China), Jiang Xu, Xiaowen Wu, Zhehui Wang (Hong Kong University of Science and Technology, Hong Kong), Bin Li, Ravi Iyer, Ramesh Illikkal (Intel Labs, United States)

C1L-B-02 An NoC-Based Evaluation Platform for Safety-Critical Automotive Applications

(pp. 679-682)

Tomohiro Yoneda (National Institute of Informatics, Japan), Masashi Imai (Hirosaki University, Japan), Hiroshi Saito (University of Aizu, Japan), Takahiro Hanyu (Tohoku University, Japan), Kenji Kise (Tokyo Institute of Technology, Japan), Yuichi Nakamura (NEC Corporation, Japan)

C1L-B-03 Highly Reliable Single-Ended Current-Mode Circuit for an Inter-Chip Asynchronous (pp. 683–686) **Communication Link**

Akira Mochizuki, Hirokatsu Shirahama, Naoya Onizawa, Takahiro Hanyu (Tohoku University, Japan)

C1L-B-04 Energy-and-Performance Efficient Differential Domino Logic Cell Libraries for (pp. 687–690) **QDI-Model-Based Asynchronous Circuits**

Masashi Imai (Hirosaki University, Japan), Tomohiro Yoneda (National Institute of Informatics, Japan)

C1L-B-05 An Extended Framework for Worst-Case Throughput Analysis with Router Constraint

(pp. 691-694)

Vineeth Mohan (Hong Kong University of Science and Technology, Hong Kong), Wenjing Hsu (Nanyang Technological University, Singapore), Wei Zhang, Xiaowen Wu (Hong Kong University of Science and Technology, Hong Kong)

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C1L-C-01 A Low-Power Subthreshold-to-Superthreshold Level-Shifter for Sub-0.5V Embedded (pp. 695–698) Resistive RAM (ReRAM) Macro in Ultra Low-Voltage Chips

Meng-Fan Chang, Che-Wei Wu, Jui-Yu Hung, Ya-Chin King, Chorng-Jung Lin (National Tsing Hua University, Taiwan), Mon-Shu Ho (National Chung Hsing University, Taiwan), Chia-Cheng Kuo, Shyh-Shyuan Sheu (ITRI, Taiwan)

C1L-C-02 Comparative Study of Power-Gating Architectures for Nonvolatile SRAM Cells Based on (pp. 699–702) Spintronics Technology

Yusuke Shuto, Shuu'ichirou Yamamoto, Satoshi Sugahara (Tokyo Institute of Technology, Japan)

C1L-C-03 A Novel Design of a Memristor-Based Look-Up Table (LUT) for FPGA

(pp. 703-706)

Thulasiraman Nandha Kumar, Haider Abbas F. Almurib (University of Nottingham, Malaysia), Fabrizio Lombardi (Northeastern University, United States)

C1L-C-04 Numerical Free-Disposal-Hull Data-Envelopment Analysis of Potential CMOS-Successor (pp. 707–710) Technologies

Matthias Korb (Broadcom Corporation, United States), Andreas Kleine (FernUniversität Hagen, Germany)

C1L-C-05 A Randomized Algorithm for the Fixed-Length Routing Problem

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