

2015 Workshop on Exploiting Silicon Photonics for Energy-Efficient High Performance Computing

(SiPhotonics 2015)

**Amsterdam, Netherlands
19-21 January 2015**



**IEEE Catalog Number: CFP15B26-POD
ISBN: 978-1-4799-8094-9**

2015 Workshop on Exploiting Silicon Photonics for Energy-Efficient High Performance Computing

SiPhotonics 2015

Table of Contents

Message from General Chairs	vi
Message from Program Chairs	vii
Conference Organization	ix
Program Committee	x
Invited Talks	xi

From Photonic Network to Architectural Issues

High-Speed Optical Cache Memory as Single-Level Shared Cache in Chip-Multiprocessor Architectures	1
<i>Pavlos Maniotis, Savvas Gitzenis, Leandros Tassioulas, and Nikos Pleros</i>	
On the Design of a Path-Setup Architecture for Exploiting Hybrid Photonic-Electronic NoCs	9
<i>Edoardo Fusella, José Flich, Alessandro Cilardo, and Antonino Mazzeo</i>	

From Photonics Technology to Network Issues

Partitioning Strategies of Wavelength-Routed Optical Networks-on-Chip for Laser Power Minimization	17
<i>Marta Ortin, Luca Ramini, Marco Balboni, Lorenzo Zuolo, Nonato Maddalena, Victor Viñals, and Davide Bertozzi</i>	
Optimal Power Efficient Photonic SWMR Buses	25
<i>Eldhose Peter and Smruti R. Sarangi</i>	
Channel Allocation Protocol for Reconfigurable Optical Network-on-Chip	33
<i>Jiating Luo, Cédric Killian, Sébastien Le Beux, Daniel Chillet, Hui Li, Ian O'Connor, and Olivier Sentieys</i>	
Author Index	40