

# **2014 International Conference on Field-Programmable Technology**

## **(FPT 2014)**

**Shanghai, China  
10-12 December 2014**



**IEEE Catalog Number: CFP14528-POD  
ISBN: 978-1-4799-6246-4**

# CONTENTS

## Table of Contents

### Cover Page

### Message from the General Chair and Program Co-Chairs

*Lingli Wang, Hayden Kwok-Hay So and Yuchun Ma*

### Organization

### Keynote Lectures

|   |   |
|---|---|
| Logic Emulation in the MegaLUT Era- Moore's Law beats Rent's Rule ..... | 1 |
| <i>Mike Butts</i>   |   |
| Automating Customized Computing .....                                   | 2 |
| <i>Jason Cong</i>   |   |
| Doing FPGA in a Former Software Company.....                            | 3 |
| <i>Feng-hsiung Hsu</i>  |   |

### 1.1 Tools & Design Productivity

|  |    |
|--|----|
| Design Re-Use for Compile Time Reduction in FPGA High-Level Synthesis Flows .....                    | 4  |
| <i>Marcel Gort and Jason Anderson</i>  |    |
| Is High Level Synthesis Ready for Business? A Computational Finance Case Study .....                 | 12 |
| <i>Gordon Inggs, Shane Fleming, David Thomas and Wayne Luk</i>                                       |    |
| Comparing Performance, Productivity and Scalability of the TILT Overlay Processor to OpenCL HLS..... | 20 |
| <i>Rafat Rashid, J. Gregory Steffan and Vaughn Betz</i>  |    |
| Size Aware Placement for Island Style FPGAs .....  | 28 |
| <i>Junying Huang, Colin Yu Lin, Yang Liu, Zhihua Li and Haigang Yang</i>                             |    |
| Analyzing the Impact of Heterogeneous Blocks on FPGA Placement Quality .....                         | 36 |
| <i>Chang Xu, Wentai Zhang and Guojie Luo</i>   |    |

### 1.2 Financial Applications

|  |    |
|--|----|
| Low-latency Option Pricing using Systolic Binomial Trees ..... | 44 |
| <i>Aryan Tavakkoli and David B. Thomas</i>                     |    |

|  |    |
|--|----|
| Collaborative Processing of Least-Square Monte Carlo for American Options.....               | 52 |
| <i>Jinzhe Yang, Ce Guo, Wayne Luk and Terence Nahar</i>                                      |    |
| Accelerating Transfer Entropy Computation.....   | 60 |
| <i>Shengjia Shao, Ce Guo, Wayne Luk and Stephen Weston</i>                                   |    |
| FPGA-Accelerated Monte-Carlo Integration using Stratified Sampling and Brownian Bridges..... | 68 |
| <i>Mark de Jong, Vlad-Mihai Sima, Koen Bertels and David Thomas</i>                          |    |

## **1.3 Architecture & Runtime Systems**

|   |    |
|---|----|
| Time Sharing of Runtime Coarse-Grain Reconfigurable Architectures Processing Elements in<br>Multi-Process Systems ..... | 76 |
| <i>Benjamin Carrion Schafer</i>   |    |
| Architectural Synthesis of Computational Pipelines with Decoupled Memory Access .....                                   | 83 |
| <i>Shaoyi Cheng and John Wawrzynek</i>  |    |
| Improve Memory Access for Achieving both Performance and Energy Efficiencies on<br>Heterogeneous Systems .....          | 91 |
| <i>Hongyuan Ding and Miaoqing Huang</i>   |    |
| Approaching Overhead-Free Execution on FPGA Soft-Processors .....   | 99 |
| <i>Charles Eric LaForest, Jason Anderson and J. Gregory Steffan</i>   |    |

## **2.1 Mathematical Circuits**

|   |     |
|---|-----|
| Low-Latency Double-Precision Floating-Point Division for FPGAs.....   | 107 |
| <i>Björn Liebig and Andreas Koch</i>  |     |
| Efficient FPGA Implementation of Digit Parallel Online Arithmetic Operators .....   | 115 |
| <i>Kan Shi, David Boland and George A. Constantinides</i>   |     |
| An Efficient FPGA Implementation of QR Decomposition using a Novel Systolic Array Architecture based on<br>Enhanced Vectoring CORDIC..... | 123 |
| <i>Jianfeng Zhang, Paul Chow and Hengzhu Liu</i>  |     |

|  |     |
|--|-----|
| Area Efficient Floating Point Adder and Multiplier with IEEE-754 Compatible Semantics..... | 131 |
| <i>Andreas Ehliar</i>  |     |
| A Universal FPGA-based Floating-Point Matrix Processor for Mobile Systems .....            | 139 |
| <i>Wenqiang Wang, Kaiyuan Guo, Mengyuan Gu, Yuchun Ma and Yu Wang</i>                      |     |

## **2.2 Special Session: Hardware Security**

|  |     |
|--|-----|
| A Survey on Security and Trust of FPGA-based Systems ..... | 147 |
|--|-----|

*Jiliang Zhang and Gang Qu*

Hardware Trojan Detection Acceleration Based on Word-Level Statistics Properties Management ..... 153

*He Li and Qiang Liu*

Power Supply Noise Aware Evaluation Framework for Side Channel Attacks and Countermeasures ..... 161

*Jianlei Yang, Chenguang Wang, Yici Cai and Qiang Zhou*

Memory Security in Reconfigurable Computers: Combining Formal Verification with Monitoring ..... 167

*Tobias Wiersema, Stephanie Drzevitzky and Marco Platzner*

An FPGA-based Spectral Anomaly Detection System ..... 175

*Duncan J.M Moss, Zhe Zhang, Nicholas J. Fraser and Philip H.W. Leong*

### **3.1 Applications & Devices**

ROTOROUTER: Router Support for Endpoint-Authorized Decentralized Traffic Filtering to Prevent DoS Attacks ..... 183

*Albert Kwon, Kaiyu Zhang, Perk Lun Lim, YuChen Pan, Jonathan M. Smith and André DeHon*

Parallel Resampling for Particle Filters on FPGAs ..... 191

*Shuanglong Liu, Grigoris Mingas and Christos-Savvas Bouganis*

Evaluation of SNMP-like Protocol to Manage a NoC Emulation Platform ..... 199

*Otávio Alcântara de Lima Junior, Virginie Fresse and Frédéric Rousseau*

A High-Performance Low-Power Near-Vt RRAM-based FPGA ..... 207

*Xifan Tang, Pierre-Emmanuel Gaillardon and Giovanni De Micheli*

A Pure-CMOS Nonvolatile Multi-Context Configuration Memory for Dynamically Reconfigurable FPGAs ..... 215

*Kosuke Tatsumura, Masato Oda and Shinichi Yasuda*

### **Poster Session I: Application**

A Flexible Interface Architecture for Reconfigurable Coprocessors in Embedded Multicore Systems using PCIe Single-Root I/O Virtualization ..... 223

*Oliver Sander, Steffen Baehr, Enno Luebbers, Timo Sandmann, Viet Vu Duy and Juergen Becker*

Gigabyte-Scale Alignment Acceleration of Biological Sequences via Ethernet Streaming ..... 227

*Theepan Moorthy and Sathish Gopalakrishnan*

Power Modelling and Capping for Heterogeneous ARM/FPGA SoCs ..... 231

*Yun Wu, Jose Nunez-Yanez, Roger Woods and Dimitrios S. Nikolopoulos*

Analysis and Optimization of a Deeply Pipelined FPGA Soft Processor ..... 235

*Hui Yan Cheah, Suhaib A. Fahmy and Nachiket Kapre*

|   |     |
|---|-----|
| A Circuit to Synchronize High Speed Serial Communication Channel .....  | 239 |
| <i>Mrinal J Sarmah</i>  |     |
| Novel Reconfigurable Hardware Implementation of Polynomial Matrix/Vector Multiplications .....                          | 243 |
| <i>Server Kasap and Soydan Redif</i>  |     |
| A Complementary Architecture for High-Speed True Random Number Generator .....  | 248 |
| <i>Xian Yang and Ray C.C. Cheung</i>  |     |
| Fanout Decomposition Dataflow Optimizations for FPGA-based Sparse LU Factorization .....                                | 252 |
| <i>Siddhartha and Nachiket Kapre</i>  |     |
| Zero Latency Encryption with FPGAs for Secure Time-Triggered Automotive Networks.....                                   | 256 |
| <i>Shanker Shreejith and Suhaib A. Fahmy</i>  |     |
| Using C to Implement High-efficient Computation of Dense Optical Flow on FPGA-accelerated Heterogeneous Platforms ..... | 260 |
| <i>Zhilei Chai, Haojie Zhou, Zhibin Wang and Dong Wu</i>  |     |
| Hardware Architecture of Bi-Cubic Convolution Interpolation for Real-time Image Scaling.....                            | 264 |
| <i>Gopinath Mahale, Hamsika Mahale, Rajesh Babu Parimi, S.K. Nandy and Sukumar Bhattacharya</i>                         |     |
| FPGA-based High Throughput XTS-AES Encryption/Decryption for Storage Area Network .....                                 | 268 |
| <i>Yi Wang, Akash Kumar and Yajun Ha</i>  |     |
| Zyndroid: An Android Platform for Software/Hardware Coprocessing.....   | 272 |
| <i>Susumu Mashimo, Motoki Amagasaki, Masahiro Iida, Morihiro Kuga and Toshinori Sueyoshi</i>                            |     |
| A Dataflow System for Anomaly Detection and Analysis .....  | 276 |
| <i>Andrei Bara, Xinyu Niu and Wayne Luk</i>   |     |

## Poster Session II: PhD Forum

|   |     |
|---|-----|
| Design Space Exploration for FPGA-based Hybrid Multicore Architecture .....   | 280 |
| <i>Jian Yan, Junqi Yuan, Ying Wang, Philip Leong and Lingli Wang</i>  |     |
| Reducing the Overhead of Dynamic Partial Reconfiguration for Multi-mode Circuits .....                                | 282 |
| <i>Brahim Al Farisi, Karel Heyse and Dirk Stroobandt</i>  |     |
| HW Acceleration of Multiple Applications on a Single FPGA .....   | 284 |
| <i>Yidi Liu and Benjamin Carrion Schafer</i>  |     |
| Towards Automatic Partial Reconfiguration in FPGAs .....  | 286 |
| <i>Fubing Mao, Wei Zhang and Bingsheng He</i>   |     |
| Achieving Higher Performance of Memcached by Caching at Network Interface .....                                       | 288 |
| <i>Eric S. Fukuda, Hiroaki Inoue, Takashi Takenaka, Dahoo Kim, Tsunaki Sadahisa, Tetsuya Asai and Masato Motomura</i> |     |

|   |     |
|---|-----|
| No Zero Padded Sparse Matrix-Vector Multiplication on FPGAs ..... | 290 |
|---|-----|

*Jiasen Huang, Junyan Ren, Wenbo Yin and Lingli Wang*

## Poster Session III: Architecture & Tools

|  |     |
|--|-----|
| AMMC: Advance Multi-core Memory Controller ..... | 292 |
|--|-----|

*Tassadaq Hussain, Oscar Palomar, Osman Unsal, Adrian Cristal, Eduard Ayguade, Mateo Valero and S. A. Gursal*

|  |     |
|--|-----|
| Assessing Scrubbing Techniques for Xilinx SRAM-based FPGAs in Space Applications ..... | 296 |
|--|-----|

*Fredrik Brosser, Emil Milh, Vilhelm Geijer and Per Larsson-Edefors*

|  |     |
|--|-----|
| A Fast, Energy Efficient, Field Programmable Threshold-Logic Array ..... | 300 |
|--|-----|

*Niranjan Kulkarni, Jinghua Yang and Sarma Vrudhula*

|  |     |
|--|-----|
| A Novel Three-dimensional FPGA Architecture with High-speed Serial Communication Links ..... | 306 |
|--|-----|

*Takuya Kajiwara, Qian Zhao, Motoki Amagasaki, Masahiro Iida, Morihiro Kuga and Toshinori Sueyoshi*

|  |     |
|--|-----|
| Scalable Radio Processor Architecture for Modern Wireless Communications ..... | 310 |
|--|-----|

*Young-Hwan Park, Keshava Prasad, Yeonbok Lee, Kitaek Bae and Ho Yang*

|  |     |
|--|-----|
| Integrating FPGA-based Processing Elements into a Runtime for Parallel Heterogeneous Computing ..... | 314 |
|--|-----|

*David de la Chevallerie, Jens Korinth and Andreas Koch*

|  |     |
|--|-----|
| Deep and Narrow Binary Content-Addressable Memories using FPGA-based BRAMs ..... | 318 |
|--|-----|

*Ameer M.S. Abdelhadi and Guy G.F. Lemieux*

|  |     |
|--|-----|
| Development Productivity in Implementing a Complex Heterogeneous Computing Application ..... | 322 |
|--|-----|

*Anthony Milton, David Kearney, Sebastien Wong and Simon Lemmo*

|  |     |
|--|-----|
| Real-time 3D Reconstruction for FPGAs: A Case Study for Evaluating the Performance, Area, and Programmability Trade-offs of the Altera OpenCL SDK..... | 326 |
|--|-----|

*Quentin Gautier, Alexandria Shearer, Janarbek Matai, Dustin Richmond, Pingfan Meng and Ryan Kastner*

|   |     |
|---|-----|
| Online Scheduling for FPGA Computation in the Cloud ..... | 330 |
|---|-----|

*Guohao Dai, Yi Shan, Fei Chen, Yu Wang, Kun Wang and Huazhong Yang*

|   |     |
|---|-----|
| High Performance Relevance Vector Machine on HMPSoC ..... | 334 |
|---|-----|

*Yongfu He, Shaojun Wang, Yu Peng, Yeyong Pang, Ning Ma and Jingyue Pang*

|  |     |
|--|-----|
| Improving the Reliability of RO PUF using Frequency Offset ..... | 338 |
|--|-----|

*Bin Tang, Yaping Lin and Jiliang Zhang*

## Demo Session

|   |     |
|---|-----|
| Network Recorder and Player:FPGA-based Network Traffic Capture and Replay ..... | 342 |
|---|-----|

*Siyi Qiao, Chen Xu, Lei Xie, Ji Yang, Chengchen Hu, Xiaohong Guan and Jianhua Zhou*

|  |     |
|--|-----|
| Implementation of LS-SVM with HLS on Zynq .....  | 346 |
| <i>Ma Ning, Wang Shaojun, Pang Yeyong and Peng Yu</i>  |     |
| A High-performance and High-programmability Reconfigurable Wireless Development Platform .....                                 | 350 |
| <i>Jiahua Chen, Tao Wang, Haoyang Wu, Jian Gong, Xiaoguang Li, Yang Hu, Gaohan Zhang, Zhiwei Li, Junrui Yang and Songwu Lu</i> |     |
| Image Processing by a 0.3V 2MW Coarse-Grained Reconfigurable Accelerator CMA-SOTB with a Solar Battery .....                   | 354 |
| <i>Yu Fujita, Koichiro Masuyama and Hideharu Amano</i>   |     |

## **Design Competition**

|   |     |
|---|-----|
| Hardware/Software co-design Architecture for Blokus Duo Solver .....  | 358 |
| <i>Naru Sugimoto and Hideharu Amano</i>   |     |
| Optimize MinMax Algorithm to solve Blokus Duo Game by HDL .....   | 362 |
| <i>Hossein Borhanifar and Seyed Peyman Zolnouri</i>   |     |
| An improved FPGA-based specific processor for Blokus Duo .....  | 366 |
| <i>Javier Olivito, Alberto Delmás and Javier Resano</i>   |     |
| Highly Scalable, SharedMemory, Monte-Carlo Tree Search based Blokus Duo Solver on FPGA .....                                | 370 |
| <i>Ehsan Qasemi, Amir Samadi, Mohammad Hadi Shadmehr, Bardia Azizian, Sajjad Mozaffari, Amir Shirian and Bijan Alizadeh</i> |     |
| Blokus Duo Engine on a Zynq .....   | 374 |
| <i>Susumu Mashimo, Kansuke Fukuda, Motoki Amagasaki, Masahiro Iida, Morihiro Kuga and Toshinori Sueyoshi</i>                |     |
| FPGA Implementation of Blokus Duo Player using Hardware/Software Co-Design .....  | 378 |
| <i>Akira Kojima</i>   |     |

## **MOOC Panel**

## **Industrial Session**

## **Author Index**