2015 16th Latin-American Test Symposium

(LATS 2015)

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LATS2015

16th Latin-American Test Symposium

March 25 - 27, 2015 Puerto Vallarta, Mexico

TECHNICAL PROGRAM

Wednesday - March 25, 2015

08:00 – 08:50 Registration

08:50 – 09:20 Opening Session

General Chairs: *Victor Champac – National Institute for Astrophysics,Optics and Electronics (INAOE), Mexico, Yervant Zorian – Synopsys, USA*

Program Chairs: *Vishwani Agrawal – Auburn University, USA, Leticia Bolzani Poehls – Pontifical Catholic University of Rio Grande do Sul (PUCRS), Brazil*

09:20 – 10:10 Keynote Talk

Moderator: **Vishwani Agrawal (Auburn University, USA)**

Title: Top 10 Semiconductor Trends
... that are changing how we Design, Manufacture, Test & Deliver High-Quality ICs. N/A

Phil Nigh (IBM)

10:10 – 11:00 TTEP Tutorial

Moderator: **Fabian Luis Vargas (PUCRS, Brazil)**

Title: Test & Yield Challenges in Today's Technology Nodes N/A

Yervant Zorian (Synopsys, USA)

11:00 – 11:30 Coffee Break

11:30 – 12:30 Session 1: Fault Modelling and Simulation

Moderator: **Adit Singh (Auburn University, USA)**

- **Efficient Fault Injection in QEMU 1**
  Davide Ferraretto, Graziano Pravadelli (University of Verona)

- **Ringing Error Prevention Techniques in Lucy-Richardson Deconvolution Process for SRAM Space-Time Margin Variation Effect Screening Designs 7**
  Hiroyuki Yamauchi, Worawit Somha (Fukuoka Institute of Technology)

- **Complex Delay Fault Reasoning With Sequential 7-Valued Algebra 13**
  Jaak Kõusaar, Raimund Ubar (Tallinn University of Technology)

12:30 – 14:00 Lunch

14:00 – 14:40 Invited Talk

Moderator: **Victor Champac (INAOE, Mexico)**

Title: Sub-10nm Technology Nodes: Design and Test Challenges N/A
Kaushik Roy (Purdue University)

14:40 – 15:40 Session 2: Automatic Test Generation

Moderator: **Francisco Russi (Synopsys, USA)**

- **Test Set Generation Almost For Free Using Run-Time FPGA Reconfiguration Technique 19**
  Alexandra Kourfali and Dirk Stroobandt (Ghent University)

- **Rejuvenation of Nanoscale Logic at NBTI-Critical Paths Using Evolutionary TPG 25**
  N. Palermo (Politecnico di Torino), V.Tihhomirov (Tallinn University of Technology), T.S.Copetti (Pontifical Catholic University of Rio Grande do Sul – PUCRS), M.Jenihhin, J.Raik, S.Kostin (Tallinn University of Technology), M.Gaudesi, G.Squillero, M.Sonza Reorda (Politecnico di Torino), F.Vargas, L.Bolzani Poehls (Pontifical Catholic University of Rio Grande do Sul – PUCRS).

- **An Evolutionary Approach for Test Program Compaction 31**
  R. Cantoro, M. Gaudesi, E. Sanchez, P. Schiavone, G. Squillero, (Politecnico di Torino)

15:40 – 16:00 Coffee Break

16:00 – 17:00 Session 3: Analog Mixed Signal Test

Moderator: **John Hayes (University of Michigan, USA)**

- **A Digital Technique for the Evaluation of SSB Phase Noise of Analog/RF Signals 37**
  F. Azais, S. David-Grignot, L. Latorre (LIRMM, CNRS/Univ), F. Lefevre (NXP Semiconductors Caen)

- **Single Event Effects in an Analog SOI Transconductor: A Case Study 43**
  Carlos Viale, Pablo Petrashin, Luis Toledo, Walter Lancioni, Carlos Vazquez (Universidad Católica de Córdoba)

- **CMOS Amplifier With Self-Correction Offset For SERDES Application 47**
  Rigoberto Bracamontes- Salazar, Esdras Juárez- Hernández and Federico Lobato López (Freescale Semiconductor), Esteban Martínez-Guerrero (ITESO, Jesuit University at Guadalajara)

17:00 – 18:00 Session 4: Design for Testability

Moderator: **Matteo Sonza Reorda (Politecnico di Torino, Italy**)

- **Improving Logic Obfuscation via Logic Cone Analysis 51**
  Yu-Wei Lee and Nur A. Touba (University of Texas)

- **Virtual Reconfigurable Scan-Chains on FPGAs for Optimized Board Test 57**
  Igor Aleksejev (Tallinn Univ. of Technology), Sergei Devadze, Artur Jutman (Testonica Lab OÜ), Konstantin Shibin (Tallinn University of Technology)

- **A Controllable Setup and Propagation Delay Flip-Flop Design 63**
  Alexandro Giron-Allende, and Victor Avendaño, (Freescale Semiconductor), Esteban Martinez-Guerrero (ITESO-The Jesuit University of Guadalajara)

19:00 – 21:00 Welcome Cocktail

Thursday - March 26, 2015

09:00 – 09:40 Invited Talk

Moderator: Yervant Zorian (Synopsys, USA)

Title: Scan Based Two-Pattern Tests: Should They Target Opens Instead of TDFs? 251
Adit Singh (Auburn University, USA)

09:40 – 10:20 Session 5: Memory: Testing and Fault Injection

Moderator: **Maksim Jenihhin (Tallinn Univ. of Technology, Estonia)**

- **SW-Based Transparent In-Field Memory Testing 68**
  Paolo Bernardi, Lyl Ciganda, Matteo Sonza Reorda (Politecnico di Torino), Said Hamdioui (Delft University of Technology)

- **Multiple Fault Injection Platform for SRAM-Based FPGA Based on Ground-Level Radiation Experiments 74**
  Jimmy Tarrillo, (Universidad de Ingenieria y Tecnologia – UTEC), Jorge Tonfat, Lucas Tambara, Fernanda Lima Kastensmidt and Ricardo Reis (Universidade Federal do Rio Grande do Sul - UFRGS)

10:20 – 10:50 Coffee Break

10:50– 11:50 Session 6: System-on-Chip Test

Moderator: **Carlos Silva Cardenas (PUCP, Peru)**

- **Generation and Performance Evaluation of Reconfigurable Random Routing Algorithm for 2D Mesh NoCs 80**
  Sandeep Kumar Singh, Abir J Mondal, Alak Majumder (NIT Arunachal Pradesh)

- **Effective Selection of Favorable Gates in BTI-Critical Paths to Enhance Circuit Reliability 86**
  Andres Gomez, Victor Champac (National Institute for Astrophysics, Optics and Electronics - INAOE)

- **Adopting Multi-Valued Logic For Reduced Pin-Count Testing 92**
  Baohu Li, Bei Zhang and Vishwani D. Agrawal (Auburn University)

11:50 – 12:10 Invited Talk

Moderator: **Florence Azais (LIRMM, CNRS/University, France)**

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David Atienza (Ecole Polytechnique Federale de Lausanne - EPFL)

12:10 – 13:40 Lunch

13:40 – 14:10 Poster Session

Moderator: **Ernesto Sanchez (Politecnico di Torino, Italy)**

- **Design Dependent SRAM PUF Robustness Analysis 98**
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- **A Virtual Instrumentation Design for Low-Cost Charge-Pumping Characterization in Integrated MOSFETs 104**
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- **FPGA Redundancy Recovery Based on Partial Bitstreams for Multiple Partitions 108**
  Victor M. Gonçalves Martins (Federal University of Santa Catarina)(INESC-ID), Joao Gabriel Reis (Federal University of Santa Catarina), Horacio C. C. Neto (INESC-ID), Eduardo Augusto Bezerra (Federal University of Santa Catarina).

- **Low Cost Built-in-Tuning of On-Chip Passive Filters for Low-If Double Quadrature RF Receiver 112**
  W. Rahajandraibe, F. Haddad, H. Aziza, K. Castellani-Coulié, J-M. Portal (Aix Marseille University, CNRS, Université de Toulon)

- **NBTI-Induced Circuit Aging Optimization By Protectability-Aware Gate Replacement Technique 116**
  Guimao Zhang, Maoxiang Yi, Yong Miao, Dawen Xu, Huaguo Liang (Hefi University of Technolgy)

14:10 – 15:50 Special Session: Issues in Electronic Design Automation: Tolerance Analysis and Design Verification

Moderator: **Esteban Tlelo Cuautle (INAOE, Mexico)**
Luis Gerardo de la Fraga (CINVESTAV, Mexico)

- **Optimizing Operational Amplifiers by Metaheuristics and Considering Tolerance Analysis 120**
  Luis Gerardo de la Fraga (Cinvestav), Esteban Tlelo-Cuautle (INAOE)

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  I. Guerra-Gomez (SEMTECH/Snowbush Mexico Design Center), Trent McConaghy (Solido Design Automation), E. Tlelo-Cuautle (INAOE)

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  Jesus López-Arredondo, Esteban Tlelo-Cuautle (INAOE), Rodolfo Trejo-Guerra (SEMTECH-Snowbush)

- **Fault Conditions of a Simple Chaotic Circuit Under Capacitor Nonlinear Effects 140**
  J.L. Bueno-Ruiz, C.A. Arriaga-Arriaga, R. Huerta-Barrera, G.V. Cruz-Domínguez, C.H. Pimentel-Romero, J.M. Muñoz-Pacheco, L.C. Gómez-Pavón, O. Félix-Beltrán, A. Luis-Ramos (Benemérita Universidad Autónoma de Puebla)

15:50 – 16:10 Coffee Break

16:10 – 16:50 Session 7: Software-Based Fault Tolerance

Moderator: **Graziano Pravadelli (Univ. Degli Studi di Verona, Italy)**

- **A Multi-Layer Software-Based Fault-Tolerance Approach for Heterogenous Multi-Core Systems 145**
  S. Müller, T. Koal, S. Scharoba, H.T. Vierhaus, (Brandenburg University of Technology), M. Schölzel, (IHP and University of Potsdam)

- **Considerations on Applications of Selective Hardening Based on Software Fault Tolerance Techniques 151**
  Felipe Restrepo-Calle, (Universidad Nacional de Colombia), Sergio Cuenca-Asensi, Antonio Martínez-Álvarez (University of Alicante), Fernanda Lima Kastensmidt, (Universidade Federal do Rio Grande do Sul - UFRGS)

Social Event
Gala Dinner

Friday – March 27, 2015

09:00 – 09:40 Invited Talk

Moderator: Fernanda Kastensmidt (UFRGS, Brazil)

Title: System on a Chip Security Fundamentals N/A
Ismael Rangel (Intel, USA)

09:40 – 10:40 Session 8: Built-In Self-Test

Moderator: Marcelino Santos (INESC-Lisboa, Portugal)

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  Ondřej Novák, Jiří Jeníček, Martin Rozkovec (Technical University in Liberec)

- "**Safe" Built-In Test and Tuning of BOOST Converters Using Feedback Loop Perturbations 163**
  X. Wang1 (Georgia Institute of Technology), K. Blanchard, S. Estella (Texas Instruments), A. Chatterjee (Georgia Institute of Technology)

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  Takanori Moriyasu, Satoshi Ohtake (Oita University)

10:40 – 11:10 Coffee Break

11:10 – 12:30 Session 9: Issues in EMC, EMI and Radiation

Moderator: **Fabian Luis Vargas (PUCRS, Brazil)**

- **Improvement of a Detection Chain Based on a VCO Concept for Microelectronic Reliability Under Natural Radiative Environment 175**
  K. Coulié-Castellani, W. Rahajandraibe , H. Aziza, JM. Portal (Aix Marseille Université, CNRS, Université de Toulon), G. Micolau (Université d'Avignon).

- **Impedance Matching Analysis of a Low-Cost PCB Differential Interconnect 180**
  J. Rafael del-Rey (Freescale Semiconductor & ITESO – Jesuit University of Guadalajara), Zabdiel Brito-Brito and José E. Rayas-Sánchez (Jesuit University of Guadalajara)

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João Guilherme Mourão Melo, Frank Sill Torres (University of Minas Gerais)

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12:30 – 14:00 Lunch

14:00 – 14:40 Invited Talk

Moderator: Said Hamdioui (Delft University of Technology, The Netherlands)

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Matteo Sonza Reorda (Politecnico di Torino, Italy)

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Moderator: Letícia Maria Bozani Poehls (PUCRS, Brazil)

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  Antonio Zenteno Ramírez, (Intel Tecnología de México)

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  Raul Acosta Hernandez, (Integrated Systems Technological Laboratory), Marius Strum, Wang Jiang Chau (University of Sao Paulo)

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  André B. M. Gomes, Fredy A. M. Alves, Ricardo S. Ferreira, José Augusto M. Nacif (UFV)

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16:00 – 16:30 Coffee Break

16:30 – 18:00 Session 11: Fault Tolerance Architectures

Moderator: **Antonio Zenteno (Intel, Mexico)**

- **Using Only Redundant Modules with Approximate Logic to Reduce Drastically Area Overhead in TMR 227**
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  T. Copetti, G. Cardoso Medeiros, L. Bolzani Poehls, F. Vargas (Pontifical Catholic University of Rio Grande do Sul – PUCRS)

18:00 – 18:30 Closing Remarks