

2014 Conference on Design and Architectures for Signal and Image Processing

(DASIP 2014)

**Madrid, Spain
8-10 October 2014**



**IEEE Catalog Number: CFP14DAS-POD
ISBN: 978-1-4799-5310-3**

Table of Contents



Welcome

General Co-Chairs

Keynote Speakers

Program Co-Chairs

Steering Committee

Program Committee

Conference Papers

Session 1: Wearable Computing, Compressed Sensing, and Communication 1

Rakeness-based Compressed Sensing on Ultra-Low Power Multi-Core Biomedical Processors 3
Daniele Bortolotti, Mauro Mangia, Andrea Bartolini, Riccardo Rovatti, Gianluca Setti and Luca Benini

A Wearable Human Activity Recognition System on a Chip 11
Koldo Basterretxea, Javier Echanobe and Inés Del Campo

Flexible Real-Time Transmitter at 10Gbit/s for SCFDMA PONs Focusing on Low-Cost ONUs 19
Lukas Meder, Philipp Schindler, Amos Agmon, Maxim Meltsin, Rene Bonk, Michael Dreschmann, Joachim Meyer, Alex Tolmachev, Rolf Hilgendorf, Moshe Nazarathy, Shalva Ben-Ezra, Thomas Pfeiffer, Wolfgang Freude, Jürg Leuthold, Christian Koos and Jürgen Becker

Session 2: Hardware, FPGAs, and Reconfigurable Hardware 27

FPGA Implementation of a Flexible Synchronizer for Cognitive Radio Applications 29
Farid Shamani, Roberto Airoidi, Tapani Ahonen and Jari Nurmi

Hardware Realization of an FPGA Processor -- Operating System Call Offload and Experiences 37
Andreas Hindborg, Nicklas Bo Jensen, Pascal Schleuniger and Sven Karlsson

Automatic Generation of Dataflow-Based Reconfigurable Coprocessing Units 45
Carlo Sau and Francesca Palumbo

Closed-loop Adaptive and Stochastic Prefetch Mechanism for Data Array 53
Lionel Vincent and Stéphane Mancini

Session 3 (SS): Arithmetic for Image and Signal Processing 61

A Fast Method for Overflow Effect Analysis in Fixed-point Systems 63
Riham Nehmeh, Daniel Menard, Andrei Banciu, Thierry Michel and Romuald Rocher

Toward the Synthesis of Fixed-Point Code for Matrix Inversion Based on Cholesky Decomposition 69
Matthieu Martel, Amine Najahi and Guillaume Revy

Table of Contents



Session 4 (SS): Visual Scene Analysis on Hybrid Multicore 77

Self Adaptive Harris Corner Detection on Heterogeneous Many-core Processor **79**
Johny Paul, Walter Stechele, Éricles Rodrigues Sousa, Vahid Lari, Frank Hannig, Jürgen Teich, Manfred Kröhnert and Tamim Asfour

Optimizing Memory Bandwidth in OpenVX Graph Execution on Embedded Many-Core Accelerators **87**
Giuseppe Tagliavini, Luca Benini and Germain Haugou

Hardware-Software Implementation of Vehicle Detection and Counting Using Virtual Detection Lines **95**
Tomasz Kryjak, Mateusz Komorkiewicz and Marek Gorgoń

A Scalable Hardware Architecture for Retinal Blood Vessel Detection in High Resolution Fundus Images **103**
Hamza Bendaoudi, Farida Cheriet, Housseem Ben Tahar and J.M.Pierre Langlois

Session 5: Frameworks and Model Transformations 109

A Framework for Rapid Prototyping of Embedded Vision Applications **111**
Michael Mefenza, Franck Ulrich Yonga Yonga, Luca B. Saldanha and Christophe Bobda

MARTE to π SDF Transformation for Data-Intensive Applications Analysis **119**
Manel Ammar, Mouna Baklouti, Maxime Pelcat, Karol Desnos and Mohamed Abid

Execution Trace Graph Analysis of Dataflow Programs: Bounded Buffer Scheduling and Deadlock Recovery Using Model Predictive Control **127**
Simone Casale Brunet, Endri Bezati, Marco Mattavelli, Massimo Canale and Jorn W. Janneck

Energy Efficiency and Performance Management of Parallel Dataflow Applications **133**
Simon Holmbacka, Erwan Nogues, Maxime Pelcat, Sébastien Lafond and Johan Lilius

Session 6: Heterogeneous Platforms 141

Accelerating Local Feature Extraction using OpenCL on Heterogeneous Platforms **143**
Konrad Moren, Diana Göhringer and Thomas Perschke

PHAT: A Technology for Prototyping Parallel Heterogeneous Architectures **151**
Thorsten Wink and Andreas Koch

Low-Cost Guaranteed-Throughput Dual-Ring Communication Infrastructure for Heterogeneous MPSoCs **159**
Berend Dekens, Philip Wilmanns, Marco Bekooij and Gerard Smit

Communication-model based Embedded Mapping of Dataflow Actors on Heterogeneous MPSoC **167**
Dinh-Thanh Ngo, Jean-Philippe Diguët, Kevin Martin and Daniel Sepulveda

Table of Contents



Poster Session 1 175

Model-Driven Design Flow for Distributed Control in Reconfigurable FPGA Systems 177
Chiraz Trabelsi, Samy Meftali, Rabie Ben Atitallah and Jean-Luc Dekeyser

Energy-Aware Decoders: a Case Study Based on an RVC-CAL Specification 183
Rong Ren, Eduardo Juarez, Cesar Sanz, Mickael Raulet and Fernando Pescador

HLS-based FPGA Implementation of a Predictive Block-based Motion Estimation Algorithm - A Field Report 189
Gregor Schewior, Christian Zahl, Holger Blume, Stefan Wonneberger and Jan Effertz

Synthilation: JIT-Compilation of Microinstruction Sequences in AMIDAR Processors 197
Christian Hochberger, Lukas Johannes Jung, Andreas Engel and Andreas Koch

Poster Session 2 (SS) 203

Arithmetic for Image and Signal Processing

Optimized Fixed-Point Implementation of a Local Stereo Matching Algorithm onto C66x DSP 205
Judicaël Menant, Muriel Pressigout, Luce Morin and Jean-François Nezan

Visual Scene Analysis on Hybrid Multicore

CUVLE: Variable-Length Encoding on CUDA 211
Antonio Fuentes-Alventosa, Juan Gómez-Luna, José María González-Linares and Nicolás Guil

Foreground Detection in Video Streams in an FPGA without External Memory 217
Martin Danek, Roman Bartosinski and Christian Hochberger

Video++, a Modern Image and Video Processing C++ Framework 223
Matthieu Garrigues and Antoine Manzanera

Poster Session 3 229

A Review of World's Fastest Connected Component Labeling Algorithms: Speed and Energy Estimation 231
Laurent Cabaret, Lionel Lacassagne and Louiza Oudni

Hardware Implementation of a Biometric Recognition Algorithm Based on In-Air Signature 237
Rosario Arjona, Iluminada Baturone and Rocío Romero-Moreno

Hardware Architecture Design and Implementation for FMCW Radar Signal Processing Algorithm 243
Eugin Hyun and Jonghun Lee

0, 1, 2, Many - A Classroom Occupancy Monitoring System for Smart Public Buildings 249
Francesco Paci, Davide Brunelli and Luca Benini

Energy Consumption Modeling of Smart Nodes with a Function Approach 255
Andriamampianina Aina Randrianarisaina, Olivier Pasquier and Pascal Chargé

Table of Contents



dasip

Demo Night 261

Demonstrating a Dataflow-based RTOS for Heterogeneous MPSoC on a Stereo Matching Applications **263**

Julien Heulot, Judicaël Menant, Maxime Pelcat, Jean Francois Nezan, Luce Morin, Muriel Pressigout and Slaheddine Aridhi.

Orc's Compa-Backend Demonstration **265**

Yaset Oliva, Emmanuel Casseau, Kevin Martin, Pierre Bomel, Jean-Philippe Diguët, Hervé Yviquel, Mickaël Raulet, Erwan Raffin and Laurent Morin

Robust Unclonable Identifiers and True Random Numbers from off-the-Shelf SRAMs **267**

Miguel Ángel Prada Delgado, Susana Eiroa and Iluminada Baturone

TURNUS: an Open-Source Design Space Exploration Framework for Dynamic Stream Programs **269**

Simone Casale Brunet, Malgorzata Maria Wiszniewska, Endri Bezati, Marco Mattavelli, Jorn Janneck and Massimo Canale