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(HOST 2015)

**Washington, DC, USA
5-7 May 2015**



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Session 1	Keynote I
Date/Time	Tuesday, 5 May 2015 / 09:00 – 10:00
Chair	Mark Tehranipoor, <i>U. of Connecticut</i>

- 🔊 **Keynote Talk: IOT Security: Challenges and Solutions**¹ IC
Dr. RAMESH SEPEHRRAD
Vice President, National Governance, Risk and Compliance Comcast

Session 2	Invited Industrial Session
Date/Time	Tuesday, 5 May 2015 / 10:20 – 11:35
Chair	Mark Tehranipoor, <i>U. of Connecticut</i>

- 🔊 **Mentor Graphics' view of Security**² IC
Serge Leef, *Mentor Graphics*
- 🔊 **Comcast's view of Security**³ IC
Jim Fahrny, *Senior Fellow, Comcast*
- 🔊 **Honeywell's view of Security**⁴ IC
Ken Heffner, *Fellow, Honeywell*

Session 3	Efficient Implementation of Secure Systems
Date/Time	Tuesday, 5 May 2015 / 01:00 – 02:15
Chair	Qiaoyan Yu, <i>University of New Hampshire</i>

- 🔊 **Silent SIMON: A Threshold Implementation under 100 Slices**⁵
Aria Shahverdi, *Mostafa Taha and Thomas Eisenbarth*
- 🔊 **Robust True Random Number Generator Using Hot-Carrier Injection Balanced Metastable Sense Amplifiers**⁶
Mudit Bhargava, *Kaship Sheikh and Ken Mai*
- 🔊 **Efficient and Secure Split Manufacturing via Obfuscated Built-In Self-Authentication**⁷
Kan Xiao, *Domenic Forte and Mark (Mohammed) Tehranipoor*

Session 4	PUF
Date/Time	Tuesday, 5 May 2015 / 02:35 – 03:50
Chair	Ioannis Savidis, <i>Drexel University</i>

- 🔊 **Security Analysis of Index-Based Syndrome Coding for PUF-Based KeGeneration**⁸
Georg T. Becker, *Alexander Wild and Tim Güneysu*
- 🔊 **Exploiting Resistive Cross-point Array for Compact Design of Physical Unclonable Function**⁹
Pai-Yu Chen, *Runchen Fang, Rui Liu, Chaitali Chakrabarti, Yu Cao and Shimeng Yu*
- 🔊 **A Family of Schmitt-Trigger-based Arbiter-PUFs and Selective Challenge-Pruning for Robustness and Quality**¹⁰
Cheng Wei Lin and *Swaroop Ghosh*

Session 5	Poster Session
Date/Time	Tuesday, 5 May 2015 / 04:00 – 05:50
Chair	Garrett S. Rose, <i>University of Tennessee</i>

- Maximum-Likelihood Decoding of Device-Specific Multi-Bit Symbols for Reliable Key Generation**⁵:
Meng-Day (Mandel) Yu, Matthias Hiller and Srinivas Devadas
- A Practical DPA on Grain v1 using LS-SVM**⁶⁶
Abhishek Chakraborty, Bodhisatwa Mazumdar and Debdeep Mukhopadhyay
- FPGA SoC Architecture and Runtime to Prevent Hardware Trojans from Leaking Secrets**⁶: "
Gedare Bloom, Bhagirath Narahari, Rahul Simha, Ali Namazi and Renato Levy
- A Security-aware Design Scheme for Better Hardware Trojan Detection Sensitivity**⁷⁴
Chongxi Bao, Yang Xie and Ankur Srivastava
- Automatic Obfuscated Cell Layout for Trusted Split-Foundry Design**⁷⁸
Carlos Tadeo Ortega Otero, Jonathan Tse, Robert Karmazin, Benjamin Hill and Rajit Manohar
- High Precision Fault Injections on the Instruction Cache of ARMv7-M Architectures**⁸⁴
Lionel Rivièrè, Zakaria Najm, Pablo Rauzy, Jean-Luc Danger, Julien Bringer and Laurent Sauvage
- Power Analysis of the t-Private Logic Style for FPGAs**⁸:
Zachary N. Goddard, Nicholas LaJeunesse and Thomas Eisenbarth
- TVVF: Estimating the Vulnerability of Hardware Cryptosystems against Timing Violation Attacks**⁹⁴
Bilgiday Yuce, Nahid Farhady Ghalaty and Patrick Schaumont
- Validation of RTL Laser Fault Injection Model with respect to Layout Information**⁹:
Athanasios Papadimitriou, Marios Tampas, David Hély, Vincent Berouille, Paolo Maistri and Regis Leveugle
- Linear Complementary Dual Code Improvement to Strengthen Encoded Circuit Against Hardware Trojan Horses**⁴: 4
Xuan Thuy Ngo, Shivam Bhasin, Jean-Luc Danger, Sylvain Guilley and Zakaria Najm
- Preventing Fault Attack on Stream Cipher using Randomization**[!]: :
Shamit Ghosh and Dipanwita Roy Chowdhury
- Post-Layout Estimation of Side-Channel Power Supply Signatures**⁴: 4
Sushmita Kadiyala Rao, Deepak Krishnankutty, Ryan Robucci, Nilanjan Banerjee and Chintan Patel
- Template Attack on Masking AES Based on Fault Sensitivity Analysis**⁸: 8
Qian Wang, An Wang, Liji Wu, Gang Qu and Guoshuang Zhang

Session 6	Keynote II
Date/Time	Wednesday, 6 May 2015 / 09:00 – 10:00
Chair	Saverio Fazzari, <i>Booz Allen Hamilton</i>

- Keynote Talk: Is it safe?**^{P IC}
Mr. W. ERIC HERR
Director, Technology Integration Office (TIO)
Office of the Under Secretary of Defense (AT&L)

Session 7	Panel
Date/Time	Wednesday, 6 May 2015 / 10:15 – 11:45
Moderators	Saverio Fazzari, <i>Booz Allen Hamilton</i> and Mark Tehranipoor, <i>U. of Connecticut</i>

- 🔊 **Kerry Bernstein**, *DARPA*
- 🔊 **Serge Leef**, *Mentor Graphics*
- 🔊 **TBA**, *Northrup Grumman*
- 🔊 **Nina Amla**, *NSF*
- 🔊 **Celia Merzbacher**, *SRC*

Session 8	Invited Government Session
Date/Time	Wednesday, 6 May 2015 / 01:00 – 02:15
Chair	Saverio Fazzari, <i>Booz Allen Hamilton</i>

- 🔊 **DARPA SHIELD Program** P IC
Arnett Brown, *Booz Allen Hamilton*
- 🔊 **AFRL Trusted Initiative** P IC
Matt Casto, *AFRL, Dayton OH*
- 🔊 **OSD Harward Assurance Initiative** P IC
Brett Hamilton, *NAVSEA-CRANE*


Session 9	Side Channel and Fault Attacks Analysis I
Date/Time	Wednesday, 6 May 2015 / 02:30 – 03:45
Chair	Yier Jin, <i>U. of Central Florida</i>

- 🔊 **Diagonal Fault Analysis of Grøstl in Dedicated MAC Mode** 322
Dhiman Saha and Dipanwita Roy Chowdhury
- 🔊 **Neural Network Based Attack on a Masked Implementation of AES** 328
Richard Gilmore, Neil Hanley and Maire O'Neill
- 🔊 **A DPA-Resistant Self-Timed Three-Phase Dual-Rail Pre-Charge Logic Family** 334
Nail Etkin Can Akkaya, Burak Erbagci, Raymond Carley and Ken Mai




Session 10	Side Channel and Fault Attacks Analysis II
Date/Time	Wednesday, 6 May 2015 / 04:00 – 05:15
Chair	Domenic Forte, <i>U. of Connecticut</i>

- 🔊 **Efficient 2nd-order Power Analysis on Masked Devices Utilizing Multiple Leakage** 33:
Liwei Zhang, A. Adam Ding, Yunsi Fei and Pei Luo
- 🔊 **Simulation and Analysis of Negative-Bias Temperature Instability Aging on Power Analysis Attacks** 346
Xiaofei Guo, Naghme Karimi, Francesco Regazzoni, Chenglu Jin and Ramesh Karri
- 🔊 **Achieving Side-Channel Protection with Dynamic Logic Reconfiguration on Modern FPGAs** 352
Pascal Sasdrich, Amir Moradi, Oliver Mischkey and Tim Güüneysu



Session 11	Keynote III
Date/Time	Thursday, 7 May 2015 / 09:00 – 10:00
Chair	James Plusquellic, <i>University of New Mexico</i>

-  **Keynote Talk: SoC Security Objectives: What Does Your Market Say?''''P IC**
Dr. DHINESH MANOHARAN
Director, Product Security Research, Security Center of Excellence
Intel

Session 12	Hardware Trojan Horses, Security Analysis, Evaluations, and Metrics
Date/Time	Thursday, 7 May 2015 / 10:20 – 11:35
Chair	Houman Homayoun, <i>George Mason University</i>

-  **Evaluating the Security of Logic Encryption Algorithms''''359**
Pramod Subramanyan, Sayak Ray and Sharad Malik
-  **GDS-II Trojan Detection using Multiple Supply Pad V_{DD} and GND I_{DDQ} s in ASIC Functional Units''''366**
I. Wilcox, F. Saqib and J. Plusquellic
-  **Resilient Hardware Trojans Detection based on Path Delay Measurements ''''373**
Ingrid Exurville, Loic Zussay, Jean-Baptiste Rigaudz and Bruno Robisson

Session 13	Secure and Trusted Synthesis and Design
Date/Time	Thursday, 7 May 2015 / 11:35 – 12:25
Chair	Gregory L. Creech, <i>ElectroScience Laboratory, Ohio State University</i>

-  **Physically Secure and Fully Reconfigurable Data Dstorage Using Optical Scattering''''379**
Roarke Horstmeyer, Sid Assaworranit, Ulrich Rührmair and Changhui Yang
-  **Toward Automatic Proof Generation for Information Flow Policies in Third-Party Hardware IP''''385**
Mohammad-Mahdi Bidmeshki and Yiorgos Makris