

2015 21st IEEE International Symposium on Asynchronous Circuits and Systems

(ASYNC 2015)

**Mountain View, California, USA
4 – 6 May 2015**



**IEEE Catalog Number: CFP15012-POD
ISBN: 978-1-4799-8717-7**

2015 21st IEEE International Symposium on Asynchronous Circuits and Systems

ASYNC 2015

Table of Contents

Message from the Chairs	viii
Technical Program Committee	x
Steering Committee	xii
Keynotes	xiii

Session 1: Crossing Clock Boundaries

A Pausible Bisynchronous FIFO for GALS Systems	1
<i>Ben Keller, Matthew Fojtik, and Brucek Khailany</i>	
How to Synchronize a Pausible Clock to a Reference	9
<i>Robert Najvirt and Andreas Steininger</i>	
A Low-Latency, Energy-Efficient L1 Cache Based on a Self-Timed Pipeline	17
<i>L.C. Trudeau, G. Gagnon, F. Gagnon, C. Thibeault, T. Awad, and D. Morrissey</i>	
Synchronizers and Data Flip-Flops are Different	19
<i>Jerome Cox, George Engel, David Zar, and Ian W. Jones</i>	

Session 2: Circuit Design and Case Studies

Blade—A Timing Violation Resilient Asynchronous Template	21
<i>Dylan Hand, Matheus Trevisan Moreira, Hsin-Ho Huang, Danlei Chen, Frederico Butzke, Zhichao Li, Matheus Gibiluka, Melvin Breuer, Ney Laert Vilar Calazans, and Peter A. Beerel</i>	
Design and Verification of Speed-Independent Multiphase Buck Controller	29
<i>Danil Sokolov, Victor Khomenko, Andrey Mokhov, Alex Yakovlev, and David Lloyd</i>	
DD1: A QDI, Radiation-Hard-by-Design, Near-Threshold 18uW/MIPS Microcontroller in 40nm Bulk CMOS	37
<i>Sean Keller, Alain J. Martin, and Chris Moore</i>	

Session 3: Demos

Session 4: Physical Design and Optimization

Timing Driven Placement for Quasi Delay-Insensitive Circuits	45
<i>Robert Karmazin, Stephen Longfield, Carlos Tadeo Ortega Otero, and Rajit Manohar</i>	
Gate Sizing and Vth Assignment for Asynchronous Circuits Using Lagrangian Relaxation	53
<i>Gang Wu, Ankur Sharma, and Chris Chu</i>	
Performance Optimization and Analysis of Blade Designs under Delay Variability	61
<i>Dylan Hand, Hsin-Ho Huang, Benmao Cheng, Yang Zhang, Matheus Trevisan Moreira, Melvin Breuer, Ney Laert Vilar Calazans, and Peter A. Beerel</i>	

Session 5: New Perspectives

Analyzing Isochronic Forks with Potential Causality	69
<i>Rajit Manohar and Yoram Moses</i>	
Naturalized Communication and Testing	77
<i>Marly Roncken, Swetha Mettala Gilla, Hoon Park, Navaneeth Jamadagni, Chris Cowan, and Ivan Sutherland</i>	

Session 6: Cryptoprocessors and NOCs

AES Hardware-Software Co-design in WSN	85
<i>Carlos Tadeo Ortega Otero, Jonathan Tse, and Rajit Manohar</i>	
Low Power Monolithic 3D IC Design of Asynchronous AES Core	93
<i>Neela Lohith Penmetsa, Christos Sotiriou, and Sung Kyu Lim</i>	
Deadlock Recovery in Asynchronous Networks on Chip in the Presence of Transient Faults	100
<i>Guangda Zhang, Jim Garside, Wei Song, Javier Navaridas, and Zhiying Wang</i>	

Session 7: Fresh Ideas

Session 8: Merge, Mutual Exclusion, and Arbitration

Increasing Impartiality and Robustness in High-Performance N-Way Asynchronous Arbiters	108
<i>Gabriele Miorandi, Davide Bertozzi, and Steven M. Nowick</i>	
Opportunistic Merge Element	116
<i>Andrey Mokhov, Victor Khomenko, Danil Sokolov, and Alex Yakovlev</i>	
Design and Analysis of Testable Mutual Exclusion Elements	124
<i>Yang Zhang, Leandro S. Heck, Matheus T. Moreira, David Zar, Melvin Breuer, Ney L.V. Calazans, and Peter A. Beerel</i>	

Session 9: Emerging Technologies

Asynchronous Charge Sharing Power Consistent Montgomery Multiplier	132
<i>Jiaoyan Chen, Arnaud Tisserand, Emanuel Popovici, and Sorin Cotofana</i>	
Non-volatility for Ultra-Low Power Asynchronous Circuits in Hybrid CMOS/Magnetic Technology	139
<i>E. Zianbetov, E. Beigne, and G. Di Pendina</i>	
Author Index	147