

2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems

(DDECS 2015)

**Belgrade, Serbia
22 – 24 April 2015**



**IEEE Catalog Number: CFP15DDE-POD
ISBN: 978-1-4799-6781-0**

2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems

DDECS 2015

Table of Contents

Foreword to the 18th IEEE DDECS	
Symposium.....	xi
Symposium Committees.....	xii
DDECS 2015 Sponsors.....	xiii
Keynotes.....	xiv
Embedded Tutorials.....	xvii

Session 1A: ATPG & Test Compression

TPG for Crosstalk Faults between On-Chip Aggressor and Victim Using Genetic Algorithms	3
<i>Kishore Duganapalli, Ajoy K. Palit, and Walter Anheier</i>	
LFSR Reseeding Based Test Compression Respecting Different Controllability of Decompressor Outputs	9
<i>Ondrej Novák, Jirí Jeníček, and Martin Rozkovec</i>	

Session 1B: Design Architectures & Synthesis

Compiler-Centred Microprocessor Design (CoMet) - From C-Code to a VHDL Model of an ASIP	17
<i>Roberto Urban, Mario Schölzel, Heinrich T. Vierhaus, Enrico Altmann, and Horst Seelig</i>	
Low-Area and High-Speed Approximate Matrix-Vector Multiplier	23
<i>I-Che Chen and John P. Hayes</i>	

Session 2A: Digital Design

A Design for the 178-MHz WXGA 30-fps Optical Flow Processor Based on the HOE Algorithm	31
<i>Tetsuya Matsumura, Aoi Kurokawa, Kousuke Imamura, and Yoshio Matsuda</i>	

A Design of Ring Oscillator Based PUF on FPGA	37
<i>Filip Kodýtek and Róbert Lórencz</i>	

Design-for-Diagnosis Architecture for Power Switches	43
<i>M. Valka, A. Bosio, L. Dilillo, P. Girard, A. Virazel, P. Debaud, and S. Guilhot</i>	

Session 2B: Analog Circuits

A Novel Compact Dual-Band Bandpass Waveguide Filter	51
<i>Snežana Stefanovski, Milka Potrebic, Dejan Tošic, and Zoran Stamenković</i>	

Fully Differential Difference Amplifier for Low-Noise Applications	57
<i>Daniel Arbet, Gabriel Nagy, Martin Kovác, and Viera Stopjaková</i>	

A Low Ripple Current Mode Voltage Doubler	63
<i>Andrzej Grodzicki and Witold Pleskacz</i>	

Poster Session I

SystemC-Based Loose Models for Simulation Speed-Up by Abstraction of RTL IP Cores	71
<i>Syed Saif Abrar, Maksim Jenihhin, and Jaan Raik</i>	

NoCDepend: A Flexible and Scalable Dependability Technique for 3D Networks-on-Chip	75
<i>Thomas Hollstein, Siavoosh Payandeh Azad, Thilo Kogge, Haoyuan Ying, and Klaus Hofmann</i>	

A Synchronous Mirror Delay with Duty-Cycle Tunable Technology	79
<i>Yo-Hao Tu, Kuo-Hsing Cheng, Yian-An Lin, and Hong-Yi Huang</i>	

Design of In AlN/GaN Heterostructure-Based Logic Cells	83
<i>Lukáš Nagy, Viera Stopjaková, and Alexander Šatka</i>	

Triangular Modulation Using Switched-Capacitor Scheme for Spread-Spectrum Clocking	87
<i>Hong-Yi Huang, Gene Fe Palencia, Da-Kai Chen, and Wei-Hsuan Huang</i>	

Application of Evolutionary Algorithms for Regression Suites Optimization	91
<i>Michaela Belešová, Zdenek Kotásek, Marcela Šimková, and Tomáš Hruška</i>	

Boolean Difference Technique for Detecting All Missing Gate Faults in Reversible Circuits	95
<i>Joyati Mondal, Bappaditya Mondal, Dipak Kole, Hafizur Rahaman, and Debesh K. Das</i>	

Combining Correction of Delay Faults and Transient Faults	99
<i>Tobias Koal, Stefan Scharoba, and Heinrich T. Vierhaus</i>	

Fast Simulation of SystemC Synthesizable Subset	103
<i>Mikhail Glukhikh and Mikhail Moiseev</i>	

Design of Wireless Sensor Network for Real-Time Structural Health Monitoring	107
<i>Marco Giammarini, Daniela Isidori, Enrico Concettoni, Cristina Cristalli, Matteo Fioravanti, and Marco Peralisi</i>	

The Advanced Circuitry of the Precision Super Capacitances Based on the Classical and Differential Difference Operational Amplifiers	111
<i>Nikolay N. Prokopenko, Nikolay V. Butyrlagin, Sergei G. Krutchinsky, Evgeniy A. Zhebrun, and Alexey E. Titov</i>	
Direct Test Methodology for HDL Verification	115
<i>Rados Dabic, Sasa Jednak, Ilija Adzic, Dusko Stanic, Aleksandar Mijatovic, and Stanislav Vuckovic</i>	
Modeling CMOS Gates Using Equivalent Inverters	119
<i>Spyridon Nikolaidis</i>	
UVM-Based Verification of Bluetooth Low Energy Controller	123
<i>Maciej Moskala, Patryk Kloczko, Marek Cieplucha, and Witold Pleskacz</i>	
PVT Insensitive High-Resolution Time to Digital Converter for Intraocular Pressure Sensing	125
<i>Hong-Yi Huang, Jen-Chieh Liu, Pei-Ying Lee, Kun-Yuan Chen, Jin-Sheng Chen, Kuo-Hsing Cheng, Tzuen-Hsi Huang, Ching-Hsing Luo, and Jin-Chern Chiou</i>	

Session 3A: Modeling and Simulation

An Asynchronous Projection and Summation Circuit for In-Pixel Processing in Single Photon Avalanche Diode Sensors	131
<i>Xiao Yang, Hongbo Zhu, Toru Nakura, Tetsuya Iizuka, and Kunihiko Asada</i>	
BSIM4 to PSP Model Conversion for Passive Mixer IM3 Simulation	137
<i>Dušan N. Grujic, Mihajlo Božovic, and Milan Savic</i>	

Session 3B: Student Session

FPGA Prototyping and Accelerated Verification of ASIPs	145
<i>Jakub Podivinsky, Marcela Šimková, Ondrej Cekan, and Zdenek Kotásek</i>	
Performance Enhancement of Serial Based FPGA Probabilistic Fault Emulation Techniques	149
<i>Ioana Mot, Oana Boncalo, and Alexandru Amarica</i>	
Parameterized Critical Path Selection for Delay Fault Testing	153
<i>Miroslav Siebert and Elena Gramatova</i>	
Mapping Trained Neural Networks to FPNs	157
<i>Martin Krcma, Jan Kastil, and Zdenek Kotásek</i>	
Synthesis and Optimization of Switching Nanoarrays	161
<i>Muhammed Ceylan Morgul and Mustafa Altun</i>	
Modeling the Coupling through Substrate for Frequencies up to 100GHz	165
<i>Vasileios Gerakis, Fontounasios Christos, and Alkis Hatzopoulos</i>	

Session 4A: Formal Verification

Contradiction Analysis for Inconsistent Formal Models	171
<i>Nils Przigoda, Robert Wille, and Rolf Drechsler</i>	
Equivalence Checking on System Level Using a Priori Knowledge	177
<i>Niels Thole, Heinz Riener, and Görschwin Fey</i>	
Requirement Phrasing Assistance Using Automatic Quality Assessment	183
<i>Arman Allahyari-Abhari, Mathias Soeken, and Rolf Drechsler</i>	

Session 4B: Design Enhancement

A Design Preconditioning Flow for Low-Noise Circuits	191
<i>Steffen Zeidler, Xin Fan, Oliver Schrape, and Miloš Krstić</i>	
Containment of Metastable Voltages in FPGAs	197
<i>Robert Najvirt, Thomas Polzer, Florian Beck, and Andreas Steininger</i>	
Design Flow for Radhard TMR Flip-Flops	203
<i>Vladimir Petrović and Miloš Krstić</i>	

Session 5A: Wear-Out & Intermittent Faults

Intermittent Resistive Faults in Digital CMOS Circuits	211
<i>Hans G. Kerckhoff and H. Ebrahimi</i>	
A Coarse Model for Estimation of Switching Noise Coupling in Lightly Doped Substrates	217
<i>Milan Babic and Miloš Krstić</i>	
SPICE-Inspired Fast Gate-Level Computation of NBTI-induced Delays in Nanoscale Logic	223
<i>Sergei Kostin, Jaan Raik, Raimund Ubar, Maksim Jenihhin, Thiago Copetti, Fabian Vargas, and Leticia Bolzani Poehls</i>	

Session 5B: Measurement & Analysis

Activity Profiling and Power Estimation for Embedded Wireless Sensor Node Design	231
<i>Goran Panic and Zoran Stamenković</i>	
Embedded Test Instrument for On-Chip Phase Noise Evaluation of Analog/IF Signals	237
<i>F. Azais, S. David-Grignot, L. Latorre, and F. Lefevre</i>	
A Delay Measurement Mechanism for Asynchronous Circuits of Bundled-Data Model	243
<i>Shuichi Sato and Satoshi Ohtake</i>	

Poster Session II

New Fault Models and Self-Test Generation for Microprocessors Using High-Level Decision Diagrams	251
<i>Artjom Jasnetski, Jaan Raik, Anton Tsertov, and Raimund Ubar</i>	
Simulation-Based Analysis of the Single Event Transient Response of a Single Event Latchup Protection Switch	255
<i>Marko Andjelkovic, Vladimir Petrović, Zoran Stamenković, Goran Ristic, and Goran Jovanovic</i>	
Power-Management Specification in SystemC	259
<i>Dominik Macko, Katarína Jelemenská, and Pavel Cicák</i>	
Design and Implementation of an Adaptive Algorithm for Hybrid Automatic Repeat Request	263
<i>Lukasz Lopacinski, Joerg Nolte, Steffen Buechner, Marcin Brzozowski, and Rolf Kraemer</i>	
Increasing Manufacturing Yield Using Partially Programmable Circuits with CLB Implementation of Incompletely Specified Boolean Function of the Corresponding Sub-Circuit	267
<i>A. Matrosova, S. Ostanin, and I. Kirienko</i>	
Implementation of the ADELITE Microcontroller for Biomedical Applications	271
<i>Krzysztof Marcinek, Maciej Plasota, Andrzej Wielgus, and Witold Pleskacz</i>	
High Precision Digital Based 3.8GHz Phase Shifter	275
<i>Francesco Cannone, Gianfranco Avitabile, Giuseppe Coviello, and Giovanni Piccini</i>	
Generic Self Repair Architecture with On-Line Fault Diagnosis	279
<i>Stefan Kristofik, Marcel Balaz, and Maria Fischerova</i>	
Microwave Selective Amplifiers with High Asymptotic Attenuation in the Range of Subresonance Frequencies	283
<i>Nikolay N. Prokopenko, Nikolay V. Butyrlagin, Sergei G. Krutchinsky, Evgeniy A. Zhebrun, and Alexey E. Titov</i>	
Analog Circuitry for BLDC Motor Magnetic Saturation Diagnostic	287
<i>Nebojsa Pjevalica, Milos Nikolic, and Ivan Kastelan</i>	
High Throughput Floating-Point Dividers Implemented in FPGA	291
<i>Peter Malik</i>	
Formal Verification of Software for the Contiki Operating System Considering Interrupts	295
<i>Thilo Vörtler, Benny Höckner, Petra Hofstedt, and Thomas Klotz</i>	
Wireless Heart Rate Monitor in Personal Emergency Response System	299
<i>David L. Larkai and Ruiheng Wu</i>	
Hardware Implementation of a RSS Localization Algorithm for Wireless Capsule Endoscopy	301
<i>M. Cicic, J.G. Teran, and Zoran Stamenković</i>	

Author Index	305
---------------------------	-----