

# **2015 Symposium on VLSI Technology**

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M. Khare, IBM Research

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G. Yeap, Qualcomm Inc.

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R. Arghavani, LAM Research

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(Invited)

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Chairpersons: S. Takagi, The Univ. of Tokyo  
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Tuesday, June 16, 20:00-22:00

Organizers: Technology  
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G. Jurczak, imec

Circuits  
M. Yamaoka, Hitachi, Ltd.  
A. Molnar, Cornell Univ.

Moderators: J. Tham, Broadcom Corp.  
T. Piliszczuk, Soitec

Panelists: O. Nalamasu, Applied Materials  
J. Hausner, Intel Mobile Communications GmbH  
S. Tanaka, Murata  
T. Yamauchi, Renesas Electronics Corp.  
S. Sivaram, SanDisk  
C. Diaz, TSMC  
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Tuesday, June 16, 20:00-22:00

Organizers: N. Sugii, Hitachi, Ltd.  
G. Jurczak, imec

Moderators: A. Nishiyama, Toshiba Corp.  
F. Boeuf, STMicroelectronics

Panelists: M. Vinet, CEA-LETI  
E. Shiu, Google  
A. Kumar, IBM  
A. Thean, imec  
J. Ohta, Nara Institute of Science & Technology  
T. Mogami, PETRA  
S. Mitra, Stanford Univ.

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### [Shunju I, II, III]

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Chairpersons: M. Motomura, Hokkaido Univ.  
G. Lehmann, Infineon Technologies AG

#### 1-1 - 8:30

##### Welcome and Opening Remarks

H. Kabuo, Socionext Inc.  
J. Gealow, Analog Devices, Inc.

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(Invited)

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(Invited)

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Chairpersons: M. Tada, NEC Corp.  
G. Yeric, ARM Ltd.

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(Invited)

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(Invited)

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K. Attenborough, NXP Central R&D

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C.-P. Chang, Applied Materials

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**8-3 - 14:45**

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**8-5 - 15:35**

**Improved Electromigration-Resistance of Cu Interconnects by Graphene-Based Capping Layer**, S. J. Yoon\*, A. Yoon\*\*, W. S. Hwang\*\*\*, S.-Y. Choi\* and B. J. Cho\*, \*KAIST, Korea, \*\*Lam Research Corp., USA and \*\*\*Korea Aerospace Univ., Korea

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G. Jurczak, imec

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**9-3 - 17:05**

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**A Novel CBRAM Integration Using Subtractive Dry-Etching Process of Cu Enabling High-Performance Memory Scaling Down to 10nm Node**, A. Redolfi\*, L. Goux\*, N. Jossart\*, F. Yamashita\*\*, E. Nishimura\*\*, D. Urayama\*\*, K. Fujimoto\*\*, T. Witters\*, F. Lazzarino\* and M. Jurczak\*, imec, Belgium and \*\*Tokyo Electron Ltd., Japan

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S. Salahuddin, Univ. of California, Berkeley

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**MoS<sub>2</sub> FET Fabrication and Modeling for Large-Scale Flexible Electronics**, L. Yu, D. El-Damak, S. Ha, S. Rakheja, X. Ling, J. Kong, D. Antoniadis, A. Chandrakasan and T. Palacios, Massachusetts Institute of Technology, USA

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**SESSION 11 - Advanced CMOS Technology: Si FinFET Device & Process [Shunju II, III]**

Thursday, June 18, 8:30-10:10

Chairpersons: T. Yamashita, Renesas Electronics Corp.  
W. Rachmady, Intel Corp.

**11-1 - 8:30**

**RMG nMOS 1<sup>st</sup> Process Enabling 10x Lower Gate Resistivity in N7 Bulk FinFETs**, L.-Å. Ragnarsson\*, H. Dekkers\*, T. Schram\*, S. A. Chew\*, B. Parvais\*, M. Dehan\*, K. Devriendt\*, Z. Tao\*, F. Sebaai\*, C. Baerts\*, S. Van Elshocht\*, N. Yoshida\*\*, A. Phatak\*\*, C. Lazik\*\*, A. Brand\*\*, W. Clark\*\*\*, D. Fried\*\*\*, D. Mocuta\*, K. Barla\*, N. Horiguchi\* and A. V.-Y. Thean\*, imec, Belgium, \*\*Applied Materials and \*\*\*Coventor, Inc., USA

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11-2 - 8:55

**High Sigma Measurement of Random Threshold Voltage Variation in 14nm Logic FinFET Technology**, M. D. Giles, N. A. Radhakrishna, D. Becher, A. Kornfeld, K. Maurice, S. Mudanai, S. Natarajan, P. Newman, P. Packan and T. Rakshit, Intel Corp., USA

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11-3 - 9:20

**High Voltage I/O FinFET Device Optimization for 16nm System-on-a-Chip (SoC) Technology**, T. Miyashita, K. C. Kwong, P. H. Wu, B. C. Hsu, P. N. Chen, C. H. Tsai, M. C. Chiang, C. Y. Lin and S. Y. Wu, TSMC, Taiwan

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11-4 - 9:45

**A Novel ALD SiBCN Low-k Spacer for Parasitic Capacitance Reduction in FinFETs**, T. Yamashita\*, S. Mehta\*, V. S. Basker\*, R. Southwick\*, A. Kumar\*\*, R. Kambhampati\*\*\*, R. Sathiyarayanan\*\*, J. Johnson\*\*, T. Hook\*, S. Cohen\*, J. Li\*, A. Madan\*, Z. Zhu\*, L. Tai\*, Y. Yao\*, P. Chinthamanipeta\*, M. Hopstaken\*, Z. Liu\*, D. Lu\*, F. Chen\*\*, S. Khan\*\*, D. Canaperi\*, B. Haran\*, J. Stathis\*, P. Oldiges\*, C.-H. Lin\*, S. Narasimha\*\*, A. Bryant\*, W. K. Henson\*\*, S. Kanakasabapathy\*, K. V. R. M. Murali\*\*, T. Gow\*, D. McHerron\*, H. Bu\* and M. Khare\*, \*IBM Research, \*\*IBM SRDC and \*\*\*GLOBALFOUNDRIES, USA

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**SESSION 12 - Memory Technology: MTJ and Related Devices [Shunju I]**

Thursday, June 18, 8:30-10:10

Chairpersons: S. Choi, Samsung Electronics Co., Ltd.  
N. Ramaswamy, Micron Technology, Inc.

12-1 - 8:30

**Novel Oxygen Showering Process (OSP) for Extreme Damage Suppression of Sub-20nm High Density p-MTJ Array without IBE Treatment**, J. H. Jeong\*\*\* and T. Endoh\*\*\*\*, \*Tohoku Univ., Japan, \*\*Samsung Electronics Co., Ltd., Korea and \*\*\*JST-ACCEL, Japan

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12-2 - 8:55

**10 nm $\phi$  Perpendicular-Anisotropy CoFeB-MgO Magnetic Tunnel Junction with Over 400°C High Thermal Tolerance by Boron Diffusion Control**, H. Honjo\*, H. Sato\*, S. Ikeda\*\*, S. Sato\*, T. Watanebe\*\*\*, S. Miura\*, T. Nasuno\*\*\*, Y. Noguchi\*\*\*, M. Yasuhira\*, T. Tanigawa\*\*\*, H. Koike\*\*\*, M. Muraguchi\*\*\*, M. Niwa\*, K. Ito\*, H. Ohno\* and T. Endoh\*\*\*, \*Tohoku Univ. and \*\*JST-ACCEL, Japan

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12-3 - 9:20

**An 8-bit Analog-to-Digital Converter Based on the Voltage-Dependent Switching Probability of a Magnetic Tunnel Junction**, W. H. Choi, Y. Lv, H. Kim, J.-P. Wang and C. H. Kim, Univ. of Minnesota, USA

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12-4 - 9:45

**Demonstration of an MgO Based Anti-Fuse OTP Design Integrated With a Fully Functional STT-MRAM at the Mbit Level**, G. Jan, L. Thomas, S. Le, Y.-J. Lee, H. Liu, J. Zhu, R.-Y. Tong, K. Pi, Y.-J. Wang, D. Shen, R. He, J. Haq, J. Teng, V. Lam, R. Annapragada, T. Zhong, T. Torng and P.-K. Wang, TDK-Headway Technologies, Inc., USA

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**SESSION 13 - Advanced CMOS Technology: X-On Insulator (X-OI) Devices [Shunju II, III]**

Thursday, June 18, 10:30-12:35

Chairpersons: K. Tateiwa, TowerJazz Panasonic Semiconductor Co., Ltd.  
C. Mazure, Soitec

13-1 - 10:30

**14nm FDSOI Upgraded Device Performance for Ultra-Low Voltage Operation**, O. Weber\*\*, E. Josse\*, J. Mazurier\*\*, N. Degors\*\*\*, S. Chhun\*, P. Maury\*, S. Lagrasta\*, D. Barge\*, J.-P. Manceau\*\*\* and M. Haond\*, \*STMicroelectronics, \*\*CEA-LETI and \*\*\*IBM, France

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13-2 - 10:55

**Novel Single p+Poly-Si/Hf/SiON Gate Stack Technology on Silicon-on-Thin-Buried-Oxide (SOTB) for Ultra-Low Leakage Applications**, Y. Yamamoto\*, H. Makiyama\*, T. Yamashita\*, H. Oda\*, S. Kamohara\*, N. Sugii\*, Y. Yamaguchi\*, T. Mizutani\*\*, M. Kobayashi\*\* and T. Hiramoto\*\*, \*LEAP and \*\*The Univ. of Tokyo, Japan

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13-3 - 11:20

**Confined Epitaxial Lateral Overgrowth (CELO): A Novel Concept for Scalable Integration of CMOS-Compatible InGaAs-on-Insulator MOSFETs on Large-Area Si Substrates**, L. Czornomaz\*, E. Uccelli\*, M. Sousa\*, V. Deshpande\*, V. Djara\*, D. Caimi\*, M. D. Rossell\*\*, R. Erni\*\* and J. Fompeyrine\*, \*IBM Research and \*\*EMPA, Switzerland

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13-4 - 11:45

**High Hole Mobility Front-Gate InAs/InGaSb-OI Single Structure CMOS on Si**, K. Nishi\*\*\*\*, M. Yokoyama\*, H. Yokoyama\*\*\*\*, T. Hoshi\*\*\*\*, H. Sugiyama\*\*\*\*, M. Takenaka\*\*\*\* and S. Takagi\*\*\*\*, \*The Univ. of Tokyo, \*\*NTT Corp. and \*\*\*JST-CREST, Japan

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13-5 - 12:10

**An InGaAs on Si Platform for CMOS with 200 nm InGaAs-OI Substrate, Gate-first, Replacement Gate Planar and FinFETs Down to 120 nm Contact Pitch**, V. Djara\*, V. Deshpande\*, E. Uccelli\*, N. Daix\*, D. Caimi\*, C. Rossel\*, M. Sousa\*, H. Siegwart\*, C. Marchiori\*, J. M. Hartmann\*\*, K.-T. Shiu\*\*\*, C.-W. Weng\*\*\*, M. Krishnan\*\*\*, M. Lofaro\*\*, R. Steiner\*\*, D. Sadana\*\*, D. Lubyshv\*\*\*\*, A. Liu\*\*\*\*, L. Czornomaz\* and J. Fompeyrine\*, \*IBM Research, Switzerland, \*\*Uni. Grenoble Alpes, France, \*\*\*IBM T. J. Watson Research Center and \*\*\*\*IQE, USA

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**SESSION 14 - Memory Technology: 3D NAND Flash & Other NVM [Shunju I]**

Thursday, June 18, 10:30-12:35

Chairpersons: H.-T. Lue, Macronix International Co., Ltd.  
J. Alsmeyer, SanDisk

14-1 - 10:30

**A Novel Dichotomic Programming Algorithm Applied to 3D NAND Flash**, C.-C. Hsieh, H.-T. Lue, Y. C. Li, T.-W. Chen, H.-P. Li and C.-Y. Lu, Macronix International Co., Ltd., Taiwan

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14-2 - 10:55

**Comprehensive Analysis of Retention Characteristics in 3-D NAND Flash Memory Cells with Tube-Type Poly-Si Channel Structure**, H.-J. Kang\*, N. Choi\*, S.-M. Joe\*, J.-H. Seo\*\*, E. Choi\*\*, S.-K. Park\*\*, B.-G. Park\* and J.-H. Lee\*, \*Seoul National Univ. and \*\*SK hynix Inc., Korea

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**14-3 - 11:20**

**Low Power 1T DRAM/NVM Versatile Memory Featuring Steep Sub-60-mV/decade Operation, Fast 20-ns Speed, and Robust 85°C-Extrapolated 10<sup>16</sup> Endurance**, Y.-C. Chiu\*, C.-H. Cheng\*\*, C.-Y. Chang\*\*\*\*, M.-H. Lee\*\*, H.-H. Hsu\*\*\*\* and S.-S. Yen\*, \*National Chiao Tung Univ., \*\*National Taiwan Normal Univ, \*\*\*Academia Sinica and \*\*\*\*TSMC, Taiwan

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**14-4 - 11:45**

**High Performance, Integrated 1T1R Oxide-Based Oscillator: Stack Engineering for Low-Power Operation in Neural Network Applications**, A. A. Sharma\*, T. C. Jackson\*, M. Schulaker\*\*, C. Kuo\*\*\*, C. Augustine\*\*\*, J. A. Bain\*, H.-S. P. Wong\*\*, S. Mitra\*\*, L. T. Pileggi\* and J. A. Weldon\*, \*Carnegie Mellon Univ., \*\*Stanford Univ. and \*\*\*Intel Corp., USA

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**14-5 - 12:10**

**Quantitative Endurance Failure Model for Filamentary RRAM**, R. Degraeve\*, A. Fantini\*, P. Roussel\*, L. Goux\*, A. Costantino\*\*, C. Y. Chen\*, S. Clima\*, B. Govoreanu\*, D. Linten\*, A. Thean\* and M. Jurczak\*, \*imec, Belgium and \*\*Univ. of Calabria, Italy

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**Luncheon Talk [Suzaku I]**

Thursday, June 18, 12:45-14:05

Organizers: S. Inaba, Toshiba Electronics Korea Corp.  
M. Motomura, Hokkaido Univ.

**DASSAI: Innovating Sake Brewing with Massive Usage of Data and IT**, K. Sakurai, Asahi Shuzo Co., Ltd.

**Technology / Circuits Joint Focus Session 3****Advanced Technology and Circuits for IoT [Suzaku II]**

Thursday, June 18, 14:20-16:00

Chairpersons: H. Noda, Micron Memory Japan, Inc.  
E. Yeo, Marvell Semiconductor

**JFS3-1 - 14:20****(Invited)**

**Technology Innovation in an IoT Era**, A. Steegen, imec, Belgium

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**JFS3-2 - 14:45**

**Fabrication of a 3000-6-Input-LUTs Embedded and Block-Level Power-Gated Nonvolatile FPGA Chip Using p-MTJ-Based Logic-in-Memory Structure**, D. Suzuki, M. Natsui, A. Mochizuki, S. Miura, H. Honjo, H. Sato, S. Fukami, S. Ikeda, T. Endoh, H. Ohno and T. Hanyu, Tohoku Univ., Japan

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**JFS3-3 - 15:10**

**Low-Voltage Metal-Fuse Technology Featuring a 1.6V-Programmable 1T1R Bit Cell with an Integrated 1V Charge Pump in 22nm Tri-gate Process**, S. H. Kulkarni, Z. Chen, B. Srinivasan, B. Pedersen, U. Bhattacharya and K. Zhang, Intel Corp., USA

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**JFS3-4 - 15:35**

**Holistic Technology Optimization and Key Enablers for 7nm Mobile SoC**, S. C. Song, J. Xu, N. N. Mojumder, K. Rim, D. Yang, J. Bao, J. Zhu, J. Wang, M. Badaroglu, V. Machkaoutsan, P. Narayanasetti, B. Bucki, J. Fischer and G. Yeap, Qualcomm Technologies, Inc., USA

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**SESSION 15 - Non-Si Substrates: III-V HEMT/FET/TFET [Shunju II, III]**

Thursday, June 18, 14:20-16:00

Chairpersons: T. Tsunomura, Tokyo Electron Ltd.  
W. Maszara, GLOBALFOUNDRIES

**15-1 - 14:20**

**High-Performance Low-Leakage Enhancement-Mode High-K Dielectric GaN MOS-HEMTs for Energy-Efficient, Compact Voltage Regulators and RF Power Amplifiers for Low-Power Mobile SoCs**, H. W. Then, L. A. Chow, S. Dasgupta, S. Gardner, M. Radosavljevic, V. R. Rao, S. H. Sung, G. Yang and R. S. Chau, Intel Corp., USA

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**15-2 - 14:45**

**In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSFETs with High Channel Mobility and Gate Stack Quality Fabricated on 300 mm Si Substrate**, M. L. Huang, S. W. Chang, M. K. Chen, C. H. Fan, H. T. Lin, C. H. Lin, R. L. Chu, K. Y. Lee, M. A. Khaderbad, Z. C. Chen, C. H. Lin, C. H. Chen, L. T. Lin, H. J. Lin, H. C. Chang, C. L. Yang, Y. K. Leung, Y.-C. Yeo, S. M. Jang, H. Y. Hwang and C. H. Diaz, TSMC, Taiwan

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**15-3 - 15:10**

**Demonstration of p-type In<sub>0.7</sub>Ga<sub>0.3</sub>As/GaAs<sub>0.35</sub>Sb<sub>0.65</sub> and n-type GaAs<sub>0.4</sub>Sb<sub>0.6</sub>/In<sub>0.65</sub>Ga<sub>0.35</sub>As Complimentary Heterojunction Vertical Tunnel FETs for Ultra-Low Power Logic**, R. Pandey\*, H. Madan\*, H. Liu\*, V. Chobpattana\*\*, M. Barth\*, B. Rajamohanam\*, M. J. Hollander\*, T. Clark\*, K. Wang\*, J.-H. Kim\*\*\*, D. Gundlach\*\*\*, K. P. Cheung\*\*, J. Suehle\*\*\*, R. Engel-Herbert\*, S. Stemmer\*\* and S. Datta\*, \*The Pennsylvania State Univ., \*\*Univ. of California, Santa Barbara and \*\*\*National Institute of Standards and Technology (NIST), USA

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**15-4 - 15:35**

**Indium Arsenide (InAs) Single and Dual Quantum-Well Heterostructure FinFETs**, A. V. Thathachary\*, N. Agrawal\*, K. K. Bhuiwarka\*\*, M. Cantoro\*\*, Y.-C. Heo\*\*, G. Lavallee\*, S. Maeda\*\* and S. Datta\*, \*The Pennsylvania State Univ., USA and \*\*Samsung Electronics Co., Ltd., Korea

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**SESSION 16 - Beyond CMOS and New Concepts [Shunju I]**

Thursday, June 18, 14:20-16:00

Chairpersons: K. Uchida, Keio Univ.  
E. Pop, Stanford Univ.

**16-1 - 14:20**

**Device Design Guideline for Steep Slope Ferroelectric FET Using Negative Capacitance in Sub-0.2V Operation: Operation Speed, Material Requirement and Energy Efficiency**, M. Kobayashi and T. Hiramoto, The Univ. of Tokyo, Japan

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**16-2 - 14:45**

**Silicon-Compatible Low Resistance S/D Technologies for High-Performance Top-Gate Self-Aligned InGaZnO TFTs with UTBB (Ultra-Thin Body and BOX) Structures**, K. Ota, T. Irisawa, K. Sakuma, C. Tanaka, K. Ikeda, T. Tezuka, D. Matsushita and M. Saitoh, Toshiba Corp., Japan

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**16-3 - 15:10**

**30-nm-Channel-Length C-Axis Aligned Crystalline In-Ga-Zn-O Transistors with Low Off-State Leakage Current and Steep Subthreshold Characteristics**, S. Matsuda, T. Hiramatsu, R. Honda, D. Matsubayashi, H. Tomisu, Y. Kobayashi, K. Tohibayashi, R. Hodo, H. Fujiki, Y. Yamamoto, M. Tsubuku, Y. Okazaki, Y. Yamamoto and S. Yamazaki, Semiconductor Energy Laboratory Co., Ltd., Japan

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**16-4 - 15:35**

**Energy Efficient 1-Transistor Active Pixel Sensor (APS) with FD SOI Tunnel FET**, N. Dagtekin and A. M. Ionescu, EPFL, Switzerland

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**Technology / Circuits Joint Focus Session 4**  
**3D and Heterogeneous Integration [Suzaku II]**  
Thursday, June 18, 16:15-17:55  
Chairpersons: B. Sheu, TSMC  
J. L. Nilles, Texas Instruments

**JFS4-1 - 16:15**

**Active-Lite Interposer for 2.5 & 3D Integration**, G. Hellings, M. Scholz, M. Detalle, D. Velenis, M. de Potter de ten Broeck, C. Roda Neve, Y. Li, S. Van Huylenbroek, S.-H. Chen, E.-J. Marinissen, A. La Manna, G. Van der Plas, D. Linten, E. Beyne and A. Thean, imec, Belgium **180**

**JFS4-2 - 16:40**

**An 82%-Efficient Multiphase Voltage-Regulator 3D Interposer with On-Chip Magnetic Inductors**, K. Tien\*, N. Sturcken\*\*, N. Wang\*\*\*, J.-W. Nah\*\*\*, B. Dang\*\*\*, E. O'Sullivan\*\*\*, P. Andry\*\*\*, M. Petracca\*\*\*\*, L. P. Carloni\*, W. Gallagher\*\*\* and K. Shepard\*, \*Columbia Univ., \*\*Ferric Inc., \*\*\*IBM T. J. Watson Research Center and \*\*\*\*Cadence Design Systems, USA **182**

**JFS4-3 - 17:05**

**15 dB Conversion Gain, 20 MHz Carrier Frequency AM Receiver in Flexible a-IGZO TFT Technology with Textile Antennas**, K. Ishida\*, R. Shabanpour\*, T. Meister\*, B. K. Boroujeni\*, C. Carta\*, L. Petti\*\*, N. Münzenrieder\*\*, G. A. Salvatore\*\*, G. Tröster\*\* and F. Ellinger\*, \*Technische Universität Dresden, Germany and \*\*Swiss Federal Institute of Technology Zurich, Switzerland **184**

**JFS4-4 - 17:30**

**Reconstruction of Multiple-User Voice Commands Using a Hybrid System Based on Thin-Film Electronics and CMOS**, L. Huang, J. Sanz-Robinson, T. Moy, Y. Hu, W. Rieutort-Louis, S. Wagner, J. C. Sturm and N. Verma, Princeton Univ., USA **186**