2015 10th International Symposium on Reconfigurable Communication-centric Systems-on-Chip

(ReCoSoC 2015)

Bremen, Germany
29 June – 1 July 2015

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ReCoSoC 2015 Technical Program

MONDAY

08:45 09:15 **Registration**

09:15 09:30 **Welcome message**

09:30 10:30 **Keynote session**

Dr. Cédric Lichtenau
Beyond many cores: Commercial workload acceleration in high-end systems

10:30 10:45 **Coffee break**

10:45 12:00 **Session 1. Reconfigurable and Self-Adaptive Systems**

Byron Navas, Ingo Sander and Johnny Öberg
Towards Cognitive Reconfigurable Hardware: Self-Aware Learning in RTR Fault-Tolerant SoCs м

Alfonso Rodriguez, Juan Valverde, César Castañares, Jorge Portilla, Eduardo de La Torre and Teresa Riesgo.
Execution Modeling in Self-Aware FPGA-Based Architectures for Efficient Resource Management ф

Charlotte Frenkel, Jean-Didier Legat and David Bol
A Partial Reconfiguration-Based Scheme to Mitigate Multiple-Bit Upsets for FPGAs in Low-Power Space Applications мт

12:00 13:30 **Lunch**

13:30 15:00 **Special Session SS1. Design and Verification of Long Term Autonomous Systems**

Embedded Keynote: Sergio Montenegro
Design to survive

Invited Talk: Rolf Drechsler, Goerschwin Fey, Rainer Koschke, Wolfgang Nebel
Vision for the Design of Long-term Autonomous Systems

Rolf Drechsler, Martin Fränzle and Robert Wille
Envisioning Self-Verification of Electronic Systems нп

15:00 15:30 **Coffee Break**

15:30 16:45 **Session 2. Taming Power and Temperature**

Sobhan Niknam, Arghavan Asad, Mahmood Fathy and Amir-Mohammad Rahmani.
Energy Efficient 3D Hybrid Processor-Memory Architecture for the Dark Silicon Age ол

Elisabeth Glocker, Qingqing Chen, Asheque M. Zaidi, Ulf Schlichtmann and Doris Schmitt-Landsiedel
Emulation of an ASIC Power and Temperature Monitor System for FPGA Prototyping оу

Wolfgang Büter, Yanqiu Huang, Daniel Gregorek and Alberto Garcia-Ortiz
A Decentralised, Autonomous, and Congestion-aware Thermal Monitoring Infrastructure for Photonic Network-on-Chip пс

16:45 17:00 **Demo preparation / Small break**

17:00 19:00 **Demos evening**

TUESDAY

09:00 10:30 **Special Session SS2. Reconfigurable Architectures for Big Data and Data Analytics**

Invited Talk: Dr. Christian De Schryver
Towards Run-Time Flexible Risk Management Systems on Hybrid Platforms

Dennis Heinrich, Stefan Werner, Marc Stelzner, Christopher Blochwitz, Thilo Pionteck and Sven Groppe
Hybrid FPGA Approach for a B+ Tree in a Semantic Web Database System рп

Stefan Werner, Dennis Heinrich, Jannik Piper, Sven Groppe, Rico Backasch, Christopher Blochwitz and Thilo Pionteck.
Automated Composition and Execution of Hardware-accelerated Operator Graphs сн

10:30 11:00 **Coffee Break**

11:00 12:15 **Session 3. Networks on Chip**

Martha Johanna Sepulveda, Daniel Florez, Satuajit Das and Guy Gogniat
Reconfigurable Security Architecture for disrupted protection zones in NoC−Based MPSoCs тл

Yunfeng Ma and Leandro Indrusiak
Hardware-accelerated Response Time Analysis for Priority-Preemptive Networks-on-Chip ту

Pietro Saltarelli, Behrad Niazmand, Ranganathan Hariharan, Jaan Raik, Gert Jervan and Thomas Hollstein.
Automated Minimization of Concurrent Online Checkers for Networks-on-Chip ус

12:15 14:00 **Lunch**

14:00 14:50 **Session 4. Bioinspired systems**

Mehdi Modarressi, Arash Firuzan and Masoud Daneshtalab
A Reconfigurable Network-on-Chip for Efficient Implementation of Neural Networks фп

Javier Mora, Andrés Otero, Eduardo de La Torre and Teresa Riesgo.
Fast and compact evolvable systolic arrays on dynamically reconfigurable FPGAs млн

14:50 15:15 **Poster Pitch 1**

Marco Antonio Zanata Alves, Paulo Santos, Matthias Diener and Luigi Carro.
Reconfigurable Vector Extensions inside the DRAM млф

Wolfgang Büter, Daniel Gregorek, Alberto Garcia-Ortiz and Awais Ahmed.
Predictable Photonic Interconnects using an Autonomous Channel Management and a TDMA-NoC ммр

Thomas Hollstein, Siavoosh Payandeh Azad, Thilo Kogge and Behrad Niazmand.
Mixed-Criticality MPSoC Partitioning based on the NoCDepend Dependability Technique мнм

Fynn Schwiegelshohn, Lars Girke and Michael Huebner.
FPGA Based Traffic Sign Detection for Automotive Camera Systems мнф

15:15 16:00 **Coffee Break and Poster Session 1**

16:00 17:15 **Special Session SS3. Energy Efficient Reconfigurable Many-Core Systems**

Karim M. A. Ali, Rabie Ben Atitallah, Jean-Luc Dekeyser and Nizar Fakhfakh.
Using Hardware Parallelism for Reducing Power Consumption in Video Streaming Applications мор

Robin Bonamy, Sébastien Bilavarn and Fabrice Muller.
An Energy-Aware Scheduler for Dynamically Reconfigurable Multi-Core Systems мпн

Parham Haririan and Alberto Garcia-Ortiz.
A Framework for Hardware-Based DVFS Management in Multicore Mixed-Criticality Systems мпу

18:00 19:00 **Stroll along the Weser**

19:00 22:30 **Gala Dinner**

WEDNESDAY

09:00 10:15 **Session 5. More secure and flexible architectures**

Timm Friedrich and Kurt Ackermann
A Flexible Co-Processing Approach for SoC-FPGAs based on Dynamic Partial Reconfiguration and Bitstream Relocation Methods мрр

Remy Druyer, Lionel Torres and Pascal Benoit
A Survey on Security Features in Modern FPGAs мсн

Osvaldo Navarro.
Configurable Cache Tuning with a Victim Cache мтл

10:15 10:45 **Poster Pitch 2**

Stefan Gehrer and Georg Sigl.
Using the Reconfigurability of Modern FPGAs for Highly Efficient PUF-Based Key Generation мтс

Luca Sterpone, Boyang Du, Lorenzo Venditti and David Merodio Codinachs.
On the Design of Highly Reliable System-on-Chip with Dynamic Reconfigurable FPGAs мун

Zahra Shirmohammadi and Seyed Ghassem Miremadi.
S2AP: An Efficient Numerical-based Crosstalk Avoidance Code For Reliable Data Transfer of NoCs муу

Amalin Prince and Vineeth Kartha.
A Framework for Remote and Adaptive Partial Reconfiguration of SoC Based Data Acquisition Systems Under Linux мфп

10:45 11:30 **Coffee Break and Poster Session 2**

11:30 12:30 **Panel discussion**

The next 10 years of ReCoSoc

12:30 12:45 **Closing session**

12:45 14:00 **Lunch snack**

14:00 14:45 **Xilinx talk**

High level synthesis and invitation to the Xilinx workshop

Presentation time for regular papers is 25 minutes.
Poster pitch presentation is 5 minutes.

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Mehdi Modarressi, Arash Firuzan and Masoud Daneshtalab
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