

2015 Fourth Berkeley Symposium on Energy Efficient Electronic Systems (E3S 2015)

**Berkeley, California, USA
1 – 2 October 2015**



IEEE Catalog Number: CFP15E3S-POD
ISBN: 978-1-4673-8569-5



Presentations

Specialization for Energy Efficiency Using Agile Development....1

B. Nikolic, J. Bachrach, E. Alon, K. Asanovic, and D. Patterson: University of California, Berkeley, USA (*Invited*)

Superconducting Computing: Lessons from an Emerging Technology....3

D. S. Holmes: IARPA, USA (*Invited*)

Millivolt Switches Will Support Better Energy-Reliability Tradeoffs....4

E. Debenedictis and H. Zima: Sandia National Laboratory, USA

SOTB Technology, which Enables Perpetually Reliable CPU for IoT Applications....7

K. Ishibashi, N. Sugii, K. Kobayashi, T. Koide, H. Nagatomi and S. Kamohara: University of Electro-Communications, Japan

mLogic: All Spin Logic Device and Circuits....10

J.-G. Zhu, D. M. Bromberg, M. Moneck, V. Sokalski, and L. Pileggi: Carnegie Mellon University, USA (*Invited*)

Electric-Field-Controlled MRAM based on Voltage Control of Magnetic Anisotropy (VCMA): Recent Progress and Perspectives....12

P. Khalili and K. Wang: University of California, Los Angeles, USA (*Invited*)

Magnonic Holographic Co-Processor: an Approach to Energy-Efficient Complementary Logic Circuitry....13

A. Khitun: University of California, Riverside, USA

Quantitative Comparison of Power-Gating Architectures for FinFET-based Nonvolatile SRAM using Spintronics Retention Technology....16

Y. Shuto, S. Yamamoto and S. Sugahara: Tokyo Institute of Technology, Japan

Anomalous Properties of Sub-10-nm Magnetic Tunneling Junctions....19

M. Stone, J. Hong, R. Guduru, A. Hadjikhani, A. Manossaukis, E. Stimpil, P. Liang, J. Bokor and S. Khizroev: Florida International University, USA

What the Brain Tells Us about the Future of Silicon....22

J. Hawkins: Numenta, USA (*Invited*)

From Microelectromechanical Switches to Nanoelectromechanical Switches: Lessons and Differences....26

J.-B. Yoon: KAIST, Korea (*Invited*)

Operating Micromechanical Logic Gates Below kBT: Physical vs Logical Reversibility....27

M. López-Suárez, I. Neri, and L. Gammaitno: University Perugia, Italy (*Invited*)

Body-Biased Operation for Improved MEM Relay Energy Efficiency....29

A. Peschot, C. Qian, D. J. Connelly and T.-J. King Liu: University of California, Berkeley, USA

Tunneling Nanoelectromechanical Switches....32

F. Niroui, E. Sletten, Y. Song, A. Wang, W. J. Ong, Jing Kong, E. Yablonovitch, T. Swager, J. Lang and V. Bulovic: MIT, USA

Van der Waals Heterostructures for Tunnel Transistors....35

T. Roy, M. Tosun, M. Amani, D.-H. Lien, D. Kiriya, P. Zhao, S. Desai, A. Sachid, S. R. Madhvapathy, and **A. Javey**: University of California, Berkeley, USA (*Invited*)

2D Tunnel Transistors for Ultra-Low Power Applications: Promises and Challenges....37

H. Ilatikhameneh, G. Klimeck and R. Rahman: Purdue University, USA

Understanding Negative Capacitance Dynamics in Ferroelectric Capacitors....40

A. Khan, K. Chatterjee, S. Salahuddin and R. Ramesh: University of California, Berkeley, USA

From Nanodevices to Nanosystems: The N3XT Information Technology....43

S. Mitra: Stanford University, USA (*Invited*)

Our Computer Systems Are Not Good Enough....44

R. Colwell: Formerly, DARPA, USA (*Invited*)

Impact of Interface Defects on Tunneling FET Turn-on Steepness....45

T. Xiao, X. Zhao, S. Agarwal and E. Yablonovitch: University of California, Berkeley, USA

A Framework for Generation and Recombination in Tunneling Field-Effect Transistors....47

J. Teherani, W. Chern, S. Agarwal, J. Hoyt and D. Antoniadis: MIT, USA

Influence of Interface Traps on the Performance of Tunnel FETs....50

D. Esseni, M. Pala, E. Gnani and E. Sangiorgi: University of Udine, Italy (*Invited*)

Challenges of Fulfilling the Promise of Tunnel FETs....51

S. Datta and R. Pandey: Pennsylvania State University, USA (*Invited*)

Tunneling FET Device Technologies Using III-V and Ge Materials....53

S. Takagi, M.-S. Kim, M. Noguchi, K. Nishi and M. Takenaka: University of Tokyo, Japan (*Invited*)

Optical Antenna-Enhanced Nano LED for Energy-Efficient Optical Interconnect....55

M. C. Wu, E. Yablonovitch, S. Fortuna, M. Eggleston, and K. Messer: University of California, Berkeley, USA (*Invited*)

Low Capacitance, High Speed Phototransistors with a Large Absorption Region....56

C. Lalau Keraly, R. Going, M.C. Wu and E. Yablonovitch: University of California, Berkeley, USA

High-density 3D Electronic-Photonic Integration....59

V. Stojanovic: UC Berkeley, USA (*Invited*)

Optoelectronic Integration for Reduced Power Dissipation in Optical Interconnect.... 61

De Dobbelaere: Luxtera, Inc, USA (*Invited*)



Posters

- Ambient Temperature Optimization for Enterprise Servers: Key to Large-Scale Energy Savings....63*
K. Vaidyanathan, K. Gross and S. Sondur: Oracle Corp., USA
- Not Faster nor Slower Tasks, but Less Energy Hungry and Parallel: Simulation Results....66*
S. Xavier-De-Souza, C. Barros, M. Jales and L. Silveira: Universidade Federal do Rio Grande do Norte, Brazil
- An Ultra-Low-Power Low-Noise Amplifier in 45nm SOI CMOS for Portable EEG Applications....69*
P. Gadfort: US Army Research Laboratory, USA
- Mapping 1D-FFT on an Energy Efficient 3D FPGA-DRAM Architecture....72*
P. Gadfort, A. Dasu and A. Akoglu: US Army Research Laboratory, USA
- Magneto-Electric Magnetic Tunnel Junction Logic Devices....75*
N. Sharma, A. Marshall, J. Bird and P. Dowben: University of Texas, Dallas, USA
- The Energy Scaling Advantages of RRAM Crossbars....78*
S. Agarwal, O. Parekh, T.-T. Quach, C. James, J. Aimone, and M. Marinella: Sandia National Laboratories, USA
- Ultrafast Spin Dynamics as Route to High Speed and Energy Efficient Information Technologies....81*
T. Rasing: Radboud University, Netherlands
- Defect and Temperature Dependence of Tunneling in InGaAs/GaAsSb Heterojunctions with Varying Band Alignments....84*
R. Iutzi, C. Heidelberger and E. Fitzgerald: MIT, USA
- Low-Noise Near-Ballistic BN-Graphene-BN Heterostructure Field-Effect Transistors for Energy Efficient Electronic Applications....87*
M. Stolyarov, A. Balandin, M. Shur and S. Rumyantsev: University of California, Riverside, USA
- An Improved Unipolar CMOS with Elevated Body and Spacer for Low-Power Application....89*
W.-H. Lee, J.-T. Lin, K.-C. Juang, T.-C. Chang, C.-K. Huang, C.-C. Lai, B.-C. Yan and Y.-H. Lin: National Sun Yat Sen University, Taiwan
- Monolayer Strain by NEMS for Low Power Application....92*
S. Almeida and D. Zubia: University of Texas at El Paso, USA
- Sub-5 nm Gap Formation for Low Power NEM Switches....94*
J. Cao, L. Li, K. Kato, T.-J. King Liu and H.-S.P. Wong: Stanford University, USA
- Electromechanically Actuating Molecules....97*
W. J. Ong, E. Sletten, F. Niroui, J. Lang, V. Bulović and T. Swager: MIT, USA
- Novel Device Functionalities Enabled by Substitutional Doping Against Native Propensity in 2D Semiconductors....100*
J. Suh, B. Saha and J. Wu: University of California, Berkeley, USA

Electrically Injected Nanoled with Large Spontaneous Emission Enhancement from an Optical Antenna....101

S. Fortuna, M. Eggleston, K. Messer, E. Yablonovitch and M. Wu: University of California, Berkeley, USA: University of California, Berkeley, USA

Optical Slot Antennas for Enhancement of WSe2 Spontaneous Emission Rate....104

K. Messer, M. Eggleston, S. Desai, S. Fortuna, S. Madhavapathy, P. Zhao, J. Xiao, X. Zhang, A. Javey, M. Wu and E. Yablonovitch: University of California, Berkeley, USA