2015 33rd IEEE International **Conference on Computer** Design (ICCD 2015)

New York City, New York, USA 18-21 October 2015



IEEE Catalog Number: CFP15ICD-POD ISBN:

978-1-4673-7167-4

Technical Papers

CSA 1	NOC Design
Date / Time	Monday, October 19, 2015/10:15 – 11:35
Session Chair	Paul Gratz, Texas A&M University
Room	405, Kimmel Center

Design of High-Performance, Power-Efficient Optical NoCs Using Silica-Embedded Silicon Nanophotonics 1

Elena Kakoulli, Vassos Soteriou, Charalambos Koutsides and Kyriacos Kalli

- A Fast and Energy Efficient Branch and Bound Algorithm for NoC Task Mapping 9

 Jiashen Li and Yun Pan
- PID Controlled Thermal Management in Photonic Network-on-Chip 17
 Dharanidhar Dang, Rabi Mahapatra and Eun Jung Kim

TVS 1	Verification
Date / Time	Monday, October 19, 2015/10:15 – 11:35
Session Chair	Masahiro Fujita, University of Tokyo
Room	406, Kimmel Center

Power-Aware Multi-Voltage Custom Memory Models for Enhancing RTL and Low Power Verification 24

Vijay Kiran Kalyanam, Martin Saint-Laurent and Jacob A. Abraham

- Clustering-Based Revision Debug in Regression Verification 32

 Djordje Maksimovic, Andreas Veneris and Zissis Poulos
- SI-SMART: Functional Test Generation for RTL Circuits Using Loop Abstraction and Learning Recurrence Relationships 38

 Prateek Puri and Michael S. Hsiao
- Emulation-Based Selection and Assessment of Assertion Checkers for Post-Silicon Validation 46
 Pouya Taatizadeh and Nicola Nicolici

CSA 2	Energy and Performance Optimization
Date / Time	Monday, October 19, 2015/11:40 – 13:00
Session Chair	Mingoo Seok, Columbia University
Room	405, Kimmel Center

Exploring Multiple Sleep Modes in On/Off Based Energy Efficient HPC Networks 54 Karthikeyan P. Saravanan, Paul M. Carpenter and Alex Ramirez

- Wide I/O or LPDDR? Exploration and Analysis of Performance, Power and Temperature Trade-Offs of Emerging DRAM Technologies in Embedded MPSoCs 62

 Mohammad Hossein Hajkazemi, Mohammad Khavari Tavana and Houman Homayoun
- Improving the Interface Performance of Synthesized Structural FAME Simulators Through Scheduling 70

 David A. Penry
- Using M/G/1 Queueing Models with Vacations to Analyze Virtualized Logic Computations 78

 Michael J. Hall and Roger D. Chamberlainn

EDA 1	Error and Fault Tolerant Circuits
Date / Time	Monday, October 19, 2015/11:40 – 13:00
Session Chair	Donatella Sciuto, Politecnico di Milano, Italy
Room	406, Kimmel Center

- An Automated Design Flow for Approximate Circuits Based on Reduced Precision Redundancy 86

 Daniele Jahier Pagliari, Andrea Calimera, Enrico Macii and Massimo Poncino
- Logic Simplification by Minterm Complement for Error Tolerant Application 94

 Hideyuki Ichihara, Tomoya Inaoka, Tsuyoshi Iwagaki and Tomoo Inoue
- Fault-Tolerant In-Memory Crossbar Computing using Quantified Constraint Solving 101

 Alvaro Velasquez and Sumit Kumar Jha
- Improving Reliability, Performance, and Energy Efficiency of STT-MRAM with Dynamic Write Latency 109

Ali Ahari, Mojtaba Ebrahimi, Fabian Oboril and Mehdi Tahoori

CSA 3	Reliability and Memory Organization
Date / Time	Monday October 19, 2015/14:00 – 15:20
Session Chair	Karthik Swaminathan, IBM
Room	405, Kimmel Center

- Clotho: Proactive Wearout Deceleration in Chip-Multiprocessor Interconnects 117

 Arseniy Vitkovskiy, Paul V. Gratz and Vassos Soteriou
- DLB: Dynamic Lane Borrowing for Improving Bandwidth and Performance in Hybrid Memory Cube 125 Xianwei Zhang, Youtao Zhang and Jun Yang
- Memory Design for Selective Error Protection 133
 Yanan Cao, Long Chen and Zhao Zhang
- POS: A Popularity-based Online Scaling Scheme for RAID-Structured Storage Systems 141 Si Wu, Yinlong Xu, Yongkun Li and Yunfeng Zhu

PA 1	Optimizing Cache Access
Date / Time	Monday, October 19, 2015/14:00 – 15:20
Chair	Gang Quan, Florida International University
Room	406, Kimmel Center

- Immediate Sleep: Reducing Energy Impact of Peripheral Circuits in STT-MRAM Caches 149
 Eishi Arima, Hiroki Noguchi, Takashi Nakada, Shinobu Miwa, Susumu Takeda, Shinobu Fujita and Hiroshi Nakamura
- Exploit Common Source-Line to Construct Energy Efficient Domain Wall Memory Based Caches 157 Xianwei Zhang, Lei Zhao, Youtao Zhang and Jun Yang
- SCP: Synergistic Cache Compression and Prefetching 164
 Bhargavraj Patel, Gokhan Memik and Nikos Hardavellas
- Application Behavior Aware Re-reference Interval Prediction for Shared LLC 172

 Parth Lathigara, Shankar Balachandran and Virendra Singh

LCD 1	Application Oriented Design
Date / Time	Monday, October 19, 2015/15:30 – 16:30
Session Chair	Jie Gu, Northwestern University
Room	KC 405

InvArch: A Hardware-Efficient Architecture for Matrix Inversion 180
Umer I. Cheema, Gregory Nash, Rashid Ansari and Ashfaq A. Khokhar

SS 1	Data Mining for Computer Design
Date / Time	Monday, October 19, 2015/15:30 – 16:30
Session Chair	Antonio Miele, Politecnico di Milano, Italy
Room	KC 406

- Applied Statistical Inference for System Design and Management 188
 Benjamin C. Lee, Duke University
- Exploiting GPU Architectures for Dynamic Invariant Mining 192

 Nicola Bombieri, Federico Busato, Alessandro Danese, Luca Piccolboni and Graziano Pravadelli,

 University of Verona
- ItHELPS: Iterative High-Accuracy Error Localization in Post-Silicon 196 Valeria Bertacco and Wade Bonkowski, University of Michigan

CSA 4	Heterogeneous Computing Systems
Date / Time	Tuesday, October 20, 2015/09:30 – 10:30
Session Chair	Houman Homayoun, George Mason University
Room	KC 405

- An Orchestrated Approach to Efficiently Manage Resources in Heterogeneous System Architectures 200 Gabriele Pallotta, Gianluca C. Durelli, Antonio Miele, Cristiana Bolchini and Marco D. Santambrogio
- Energy-Efficient Execution of Data-Parallel Applications on Heterogeneous Mobile Platforms 208

 Alok Prakash, Siqi Wang, Alexandru Eugen Irimiea and Tulika Mitra
- Sequential C-code to Distributed Pipelined Heterogeneous MPSoC Synthesis for Streaming Applications 216

Jude Angelo Ambrose, Jorgen Peddersen, Yusuke Yachide, Kapil Batra and Sri Parameswaran

SS 2	Cyber-physical Integration and Design Automation for Microfluidic Biochips
Date / Time	Tuesday, October 20, 2015/09:30 – 10:30
Session Chair	Moderator: Jiang Hu, Texas A&M University
Room	KC 406

- Wet Computers: The Need for Design Automation and Programmability in Microfluidics N/A William Grover, University of California at Riverside
- **Cyber-Physical Integration in Programmable Microfluidic Biochips 224** *Tsung-Yi Ho, William Grover, Shiyan Hu and Krishnendu Chakrabarty, Duke University*
- Physical Design for Cyber-Physical Microfluidic Biochips: Co-Optimization and Co-Scheduling of Biochemical Operations and On-Chip Sensors N/A

 Tsung-Yi Ho, National Tsinghua University

EDA 2	Logic and Layout Synthesis
Date / Time	Tuesday, October 20, 2015/10:50 – 12:30
Session Chair	Kyle Rupnow, Advanced Digital Sciences Center, Singapore
Room	KC 405

- SOP Based Logic Synthesis for Memristive IMPLY Stateful Logic 228
 Felipe S. Marranghello, Vinicius Callegaro, Andrěl. Reis and Renato P. Ribas
- CSL: Coordinated and Scalable Logic Synthesis Techniques for Effective NBTI Reduction 236 Chen-Hsuan Lin, Subhendu Roy, Chun-Yao Wang, David Z. Pan and Deming Chen
- A Pre-search Assisted ILP Approach to Analog Integrated Circuit Routing 244
 Chia-Yu Wu, Helmut Graeb and Jiang Hu

- Trace-Based Automated Logical Debugging for High-Level Synthesis Generated Circuits 251

 Pietro Fezzardi, Michele Castellana and Fabrizio Ferrandi
- Physical Synthesis of DNA Circuits with Spatially Localized Gates 259

 Jinwook Jung, Daijoon Hyun and Youngsoo Shin

TVS 2	Security
Date / Time	Tuesday, October 20, 2015/10:50 – 12:30
Session Chair	Simha Sethumadhavan, Columbia University
Room	KC 406

- Deep Packet Field Extraction Engine (DPFEE): A Pre-processor for Network Intrusion Detection and Denial-of-Service Detection Systems 266
 Vinayaka Jyothi, Sateesh K. Addepalli and Ramesh Karri
- **3D Integration:** New Opportunities in Defense Against Cache-Timing Side-Channel Attacks 273 Chongxi Bao and Ankur Srivastava
- Side-Channel Power Analysis of a GPU AES Implementation 281 Chao Luo, Yunsi Fei, Pei Luo, Saoni Mukherjee and David Kaeli
- Performance Optimization for On-Chip Sensors to Detect Recycled Ics 289
 Bicky Shakya, Ujjwal Guin, Mark Tehranipoor and Domenic Forte
- From Theory to Practice of Private Circuit: A Cautionary Note 296
 Debapriya Basu Roy, Shivam Bhasin, Sylvain Guilley, Jean-Luc Danger and Debdeep Mukhopadhyay

PA 2	Optimization for Power and Speed
Date / Time	Tuesday, October 20, 2015/13:50 – 15:30
Session Chair	Nikos Hardavellas, Northwestern University
Room	KC 405

- © Comparison of Single-ISA Heterogeneous versus Wide Dynamic Range Processors for Mobile Applications 304
 - Hamid Reza Ghasemi, Ulya R. Karpuzcu and Nam Sung Kim
- Effective Hardware-Level Thread Synchronization for High Performance and Power Efficiency in Application Specific Multithreaded Embedded Processors 311

 Mahanama Wickramasinghe and Hui Guo
- Dynamic Core Scaling: Trading off Performance and Energy Beyond DVFS 319
 Wei Zhang, Hang Zhang and John Lach
- Online Mechanism for Reliability and Power-Efficiency Management of a Dynamically Reconfigurable Core 327
 - Sudarshan Srinivasan, Israel Koren and Sandip Kundu

LCD 2	Resistive Memories
Date / Time	Tuesday, October 20, 2015/13:50 – 15:30
Session Chair	Mihalis Maniatakos, New York University Abu Dhabi
Room	406, Kimmel Center

- Fast Boolean Logic Mapped on Memristor Crossbar 335

 Lei Xie, Hoang Anh Du Nguyen, Mottaqiallah Taouil, Said Hamdioui and Koen Bertels
- Reliable and High Performance STT-MRAM Architectures Based on Controllable-Polarity Devices 343

 Kaveh Shamsi, Yu Bi, Yier Jin, Pierre-Emmanuel Gaillardon, Michael Niemier and X. Sharon Hu
- Increasing Reconfigurability with Memristive Interconnects 351

 John Demme, Steven M. Nowick, Bipin Rajendran and Simha Sethumadhavan
- Optimizing Latency, Energy, and Reliability of 1T1R Re Through Appropriate Voltage Settings 359

 Manging Mao, Yu Cao, Shimeng Yu and Chaitali Chakrabarti
- A Thermal Adaptive Scheme for Reliable Write Operation on RRAM Based Architectures 367 Fernando García-Redondo, Marisa Lopez-Vallejo and Pablo Ituero

PS 1	Poster Session
Date / Time	Tuesday, October 20, 2015/15:30 – 16:30
Room	Eisner & Lubin Auditorium

- Power Management of Pulsed-Index Communication Protocols 375
 Shahzad Muzaffar and Ibrahim (Abe) M. Elfadel
- Big Data on Low Power Cores Are Low Power Embedded Processors a Good Fit for the Big Data Workloads? 379

 Maria Malik and Houman Homayoun
- Energy-Optimal Voltage Model Supporting a Wide Range of Nodal Switching Rates for Early Design-Space Exploration 383

 Doyun Kim, Jiangyi Li and Mingoo Seok
- On the Conditions of Guaranteed k-Fault Tolerant Systems Supporting On-The-Fly Repairs 387 Soumya Banerjee and Wenjing Rao
- Exploring the Viability of Stochastic Computing 391

 Joao Marcos de Aguiar and Sunil P. Khatri
- A New Encoding Mechanism for Low Power Inter-Chip Serial Communication in Asynchronous Circuits 395

Tomohiro Yoneda and Masashi Imai

- Energy-Efficient Data Movement with Sparse Transition Encoding 399 Yanwei Song, Mahdi Nazm Bojnordi and Engin Ipek
- A Low Power Buffer-Aided Vector Register File for LTE Baseband Signal Processing 403

 Liu Zhiguo, Zhu Ziyuan, Shi Jinglin, Liu Jinbao and Li Shiqiang
- An Aging-Aware Battery Charge Scheme for Mobile Devices Exploiting Plug-in Time Patterns 407

 Alberto Bocca, Alessandro Sassone, Alberto Macii, Enrico Macii and Massimo Poncino

- Analytic Processor Model for Fast Design-Space Exploration 411
 Rik Jongerius, Giovanni Mariani, Andreea Simona Anghel, Gero Dittmann, Erik Vermij and Henk Corporaal
- A Pair Selection Algorithm for Robust RO-PUF Against Environmental Variations and Aging 415

 Md. Tauhidur Rahman, Domenic Forte, Fahim Rahman and Mark Tehranipoor
- Chameleon: Adaptive Energy-Efficient Heterogeneous Network-on-Chip 419

 Ji Wu, Dezun Dong, Xiangke Liao and Li Wang
- Combative Cache Efficacy Techniques: Cache Replacement in the Context of Independent Prefetching in Last Level Cache 423

 Cesar Gomes and Mark Hempstead
- Shift-Aware Racetrack Memory 427
 Ehsan Atoofian and Ahsan Saghir
- ROST-C: Reliability Driven Optimisation and Synthesis Techniques for Combinational Circuits 431
 Satish Grandhi, David McCarthy, Christian Spagnol, Emanuel Popovici and Sorin Cotofana
- Data-Driven Logic Synthesizer for Acceleration of Forward Propagation in Artificial Neural Networks 435 Khaled Z. Mahmoud, William E. Smith, Mark Fishkin and Timothy N. Miller
- Fixed-Function Hardware Sorting Accelerators for Near Data MapReduce Execution 439
 Seth H. Pugsley, Arjun Deb, Rajeev Balasubramonian and Feifei Li
- Energy-Efficient Reconstruction of Compressively Sensed Bioelectrical Signals with Stochastic 443 Computing Circuits

 Yufei Ma, Minkyu Kim, Yu Cao, Jae-Sun Seo and Sarma Vrudhula
- Exploiting Request Characteristics and Internal Parallelism to Improve SSD Performance 447

 Bo Mao and Suzhen Wu
- FDRAM: DRAM Architecture Flexible in Successive Row and Column Accesses 451

 Jeongjae Yu and Wooyoung Jang
- Runtime Multi-Optimizations for Energy Efficient On-chip Interconnections 455

 Yuan He, Masaaki Kondo, Takashi Nakada, Hiroshi Sasaki, Shinobu Miwa and Hiroshi Nakamura
- A Hardware-based Multi-objective Thread Mapper for Tiled Manycore Architectures 459
 Ravi Kumar Pujari, Thomas Wild and Andreas Herkersdorf
- Automatic Identification of Assertions and Invariants with Small Numbers of Test Vectors 463

 Masahiro Fujita
- A Novel 3D Graphics DRAM Architecture for High-Performance and Low-Energy Memory Accesses 467

 Ishan G Thakkar and Sudeep Pasricha
- M-MAP: Multi-Factor Memory Authentication for Secure Embedded Processors 471
 Syed Kamran Haider, Masab Ahmad, Farrukh Hijaz, Astha Patni, Ethan Johnson, Matthew Seita, Omer Khan and Marten van Dijk
- Acceleration of Microwave Imaging Algorithms for Breast Cancer Detection via High-Level Synthesis 475

 Daniele Jahier Pagliari, Mario R. Casu and Luca P. Carloni
- Power and Performance Characterization, Analysis and Tuning for Energy-efficient Edge Detection on Atom and ARM Based Platforms 479

 Paul Otto, Maria Malik, Nima Akhlaghi, Rebel Sequeira, Houman Homayoun and Siddhartha Sikdar
- Security Implications of Cyberphysical Digital Microfluidic Biochips 483
 Sk Subidh Ali, Mohamed Ibrahim, Ozgur Sinanoglu, Krishnendu Chakrabarty and Ramesh Karri
- Hardware Support for Production Run Diagnosis of Performance Bugs 487

 Abdullah Muzahid
- Pre-Promotion: Synergizing Prefetching and Anti-thrashing Replacement Policy N/A
 [Work in Progress]

 Midoriko Chikara, Hidetsugu Irie, Makoto Sahoda, Masato Yoshimi and Tsutomu Yoshinaga

LCD 3	Design of Special Function Circuits
Date / Time	Wednesday, October 21, 2015/08:30 – 10:10
Session Chair	Bo Yuan, City College NY
Room	KC 405

- A Methodology for Power Characterization of Associative Memories 491

 Dawei Li, Siddhartha Joshi, Seda Ogrenci-Memik, James Hoff, Sergo Jindariani, Tiehui Liu, Jamieson Olsen and Nhan Tran
- Exploring Well Configurations for Voltage Level Converter Design in 28nm UTBB FDSOI technology 499

 Pasquale Corsonello, Stefania Perri and Fabio Frustaci
- A Wirelessly Powered System with Charge Recovery Logic 505
 Leo Filippini, Emre Salman and Baris Taskin
- Reactive Clocks with Variability-Tracking Jitter 511

 Jordi Cortadella, Luciano Lavagno, Pedro López, Marc Lupon, Alberto Moreno, Antoni Roca and Sachin S. Sapatnekar
- Methods for Analysing and Improving the Fault Resilience of Delay-Insensitive Codes 519

 Jakob Lechner, Andreas Steininger and Florian Huemer

PA 3	Architecting Processors Using New Circuit Technologies and Topologies
Date / Time	Wednesday, October 21, 2015/08:30 – 10:10
Session Chair	Shinobu Miwa, The University of Electro-Communications
Room	KC 406

- Architecting a MOS Current Mode Logic (MCML)Processor for Fast, Low Noise and Energy-Efficient Computing in the Near-Threshold Regime 527
 - Yuxin Bai, Yanwei Song, Mahdi Nazm Bojnordi, Alexander Shapiro, Engin Ipek and Eby. G. Friedman
- VLSI Implementation of High-Throughput, Low-Energy, Configurable MIMO Detector 535

 Pierce I-Jen Chuang, Manoj Sachdev and Vincent C. Gaudett
- Exploring Early & Late ALUs for Single-Issue In-Order Pipelines 543

 Alen Bardizbanyan and Per Larsson-Edefors
- Improving Memristor Memory with Sneak Current Sharing 549

 Manjunath Shevgoor, Naveen Muralimanohar, Rajeev Balasubramonian and Yoocharn Jeon

CSA 5	Managing Multi-Core Systems
Date / Time	Wednesday, October 21, 2015/10:30 – 12:10
Session Chair	Ann Gordon-Ross, University of Florida
Room	KC 405

Pool Directory: Efficient Coherence Tracking with Dynamic Directory Allocation in Many-Core Systems 557

Sudhanshu Shukla and Mainak Chaudhuri

- A Multicore Vacation Scheme for Thermal-Aware Packet Processing 565 Chih-Hsun Chou and Laxmi N. Bhuyan
- Dark Silicon Aware Runtime Mapping for Many-Core Systems: A Patterning Approach 573

 Anil Kanduri, Mohammad-Hashem Haghbayan, Amir-Mohammad Rahmani, Axel Jantsch, Pasi Liljeberg and Hannu Tenhunen
- Realizing Complexity-Effective On-Chip Power Delivery for Many-Core Platforms by Exploiting Optimized Mapping 581

 Mohammad Khavari Tavana, Divya Pathak, Mohammad Hossein Hajkazemi, Maria Malik, Ioannis Savidis and Houman Homayoun
- Cache Allocation for Fixed-Priority Real-Time Scheduling on Multi-Core Platforms 589

 Gustavo A. Chaparro-Baquero, Soamar Homsi, Omara Vichot, Shaolei Ren, Gang Quan and Shangping Ren

TVS 3	Test Optimization
Date / Time	Wednesday, October 21, 2015/10:30 – 12:10
Session Chair	Adit Singh, Auburn University
Room	KC 406

- A Novel TSV Probing Technique with Adhesive Test Interposer 597

 Li Jiang, Xiangwei Huang, Hongfeng Xie, Qiang Xu, Chao Li, Xiaoyao Liang and Huiyun Li
- A Methodology To Generate Evenly Distributed Input Stimuli By Clustering Of Variable Domain 605

 Jomu George M. P. and O. Ait Mohamed
- A Scan Chain Optimization Method for Diagnosis 613
 Huajun Chen, Zichu Qi, Lin Wang and Chao Xu
- A One-Pass Test-Selection Method for Maximizing Test Coverage 621 Cheng Xue and R.D. (Shawn) Blanton
- Non-Enumerative Correlation-Aware Path Selection 629

 Ahish Mysore Somashekar, Spyros Tragoudas and Rathish Jayabharathi

CSA 6	Performance Monitoring and Characterization
Date / Time	Wednesday, October 21, 2015/13:30 – 15:10
Session Chair	Sisu Xi, Two Sigma Securities
Room	KC 405

- RAPITIMATE: Rapid Performance Estimation of Pipelined Processing Systems Containing Shared Memory 635
 - Su Myat Min Shwe, Kapil Batra, Yusuke Yachide, Jorgen Peddersen and Sri Parameswaran
- Power Agility Metrics: Measuring Dynamic Characteristics of Energy Proportionality 643
 Rizwana Begum and Mark Hempstead
- VPM: Virtual Power Meter Tool for Low-Power Many-Core/Heterogeneous Data Center Prototype 651
 Santhosh Kumar Rethinagiri, Oscar Palomar, Javier Arias Moreno, Osman Unsal and Adrian Cristal

- TriState-SET: Proactive SET for Improved Performance of MLC Phase Change Memories 659

 Xianwei Zhang, Youtao Zhang and Jun Yang
- OpenNVM: An Open-Sourced FPGA-Based NVM Controller for Low Level Memory Characterization 666

 Jie Zhang, Gieseo Park, David Donofrio, Mustafa M Shihab, John Shalf and Myoungsoo Jung

EDA 3	Improving Computational Efficiency of Circuit Analysis
Date / Time	Wednesday, October 21, 2015/13:30 – 15:10
Session Chair	Tsung-Yi Ho, National Cheng Kung University, Taiwan
Room	KC 406

- **GPU Acceleration for PCA-Based Statistical Static Timing Analysis** 674 *Yiren Shen and Jiang Hu*
- Bottom-Up Disjoint-Support Decomposition Based on Cofactor and Boolean Difference Analysis 680 Vinicius Callegaro, Felipe S. Marranghello, Mayler G. A. Martins, Renato P.Ribas and Andre I. Reis
- Optimized Local Control Strategy for Voice-Based Interaction-Tracking Badges for Social Applications 688

 Xiaowei Liu, Alex Doboli and Fan Ye
- FPGA-SPICE: A Simulation-based Power Estimation Framework for FPGAs 696

 Xifan Tang, Pierre-Emmanuel Gaillardon and Giovanni De Micheli

CSA 7	Application-Specific Computation
Date / Time	Wednesday, October 21, 2015/15:30 – 16:30
Chair	Jiang Li, Shanghai Jiao Tong University
Room	KC 405

- Energy-Efficient Implementations of GF(p)and GF(2^m)Elliptic Curve Cryptography 704

 Andrew D. Targhetta, Donald E. Owen Jr., Francis L. Israel and Paul V. Gratz
- Hybrid Sratchpad and Cache Memory Management for Energy-Efficient Parallel HEVC Encoding 712

 Chang Song, Lei Ju and Zhiping Jia
- Mobile Ecosystem Driven Application-Specific Low-Power Control Microarchitecture 720

 Garo Bournoutian and Alex Orailoglu

SS 3	Reliable and Secure Mobile Cognition
Date / Time	Wednesday, October 21, 2015/15:30 – 16:30
Session Chair	Karthik Swaminathan, IBM T. J. Watson
Room	KC 406

- Resilient Mobile Cognition: Algorithms, Innovations, and Architectures 728

 R. Viguier, C-C. Lin, K. Swaminathan, A. Vega, A. Buyuktosunoglu, S. Pankanti, P. Bose, H. Akbarpour, F. Bunyak, K. Palaniappan, G. Seetharaman
- A Testing Platform for On-drone Computation 732
 Wang Zhou, Dhruv Nair, Oki Gunawan, Theodore van Kessel and Hendrik F. Hamann
- Resilient, UAV-Embedded Real-Time Computing 736

 Augusto Vega, Chung-Ching Lin, Karthik Swaminathan, Alper Buyuktosunoglu, Sharathchandra Pankanti and Pradip Bose