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Technical Program

Technical Program

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Co-Chair	**Jürgen Teich**, *Friedrich-Alexander-Universität Erlangen-Nürnberg, DE*

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Antun Domic

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Chair	**Muhammad Shafique**, *Karlsruhe Institute of Technology, DE*
Co-Chair	**Umit Ogras**, *Arizona State University, US*

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Co-Chair	**Rolf Ernst**, *TU Braunschweig, DE*

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Chair	**Vikas Chandra**, *ARM, US*
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Co-Chair	**Damien Hardy**, *University of Rennes 1/IRISA, FR*

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Co-Chair	**Michel Renovell**, *LIRMM, FR*

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Chair	**Wim Schoenmaker**, *Magwel NV, Leuven, BE*
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Md. Maruf Hossain, Tetsuya Iizuka, Toru Nakura and Kunihiro Asada

Session Title	Interactive Presentations
Session Code / Room	IP2
Date / Time	Wednesday, 16 March 2016 / 10:00 – 10:30

Session Title	**SPECIAL DAY Hot Topic: Formal Methods for Automotive Software**
Session Code / Room	**6.1 / Saal 2**
Date / Time	**Wednesday, 16 March 2016 / 11:00 – 12:30**
Chair	**Marc Geilen**, *Eindhoven University of Technology, NL*
Co-Chair	**Wolfgang Ecker**, *Infineon Technologies, DE*

6.1.1
11:00 – 11:30
Requirements Engineering for Software-Intensive Automotive Embedded Systems N/A
Manfred Broy

6.1.2
11:30 – 12:00
Formal Specification and Verification of Automotive Software in Practice N/A
Ravindra Metta

6.1.3
12:00 – 12:30
Timing Analysis of Automotive Architectures and Software
Nicolas Navet

Session Title	**Panel: Looking Backwards and Forwards**
Session Code / Room	**6.2 / Konferenz 6**
Date / Time	**Wednesday, 16 March 2016 / 11:00 – 12:30**
Organiser	**Marco Casale-Rossi**, *Synopsys, US*
Chair	**Marco Casale-Rossi**, *Synopsys, US*
Co-Chair	**Giovanni De Micheli**, *EPFL, CH*

6.2.1
11:00 – 12:30
Panel: Looking Backwards and Forwards 571
Marco Casale-Rossi, Giovanni De Micheli, Antun Domic, Enrico Macii, Domenico Rossi and Joe Sawicki

6.2.2
11:00 – 12:30
Panelist
Enrico Macii

6.2.3
11:00 – 12:30
Panelist
Antun Domic

6.2.4
11:00 – 12:30
Panelist
Domenico Rossi

6.2.5
11:00 – 12:30
Panelist
Joseph Sawicki

6.2.6
11:00 – 12:30
Moderator
Giovanni De Micheli

Session Title	**Anti-aging and Error protection using Checkpointing and DVFS**
Session Code / Room	**6.3 / Konferenz 1**
Date / Time	**Wednesday, 16 March 2016 / 11:00 – 12:30**
Chair	**Antonio Rosario Miele**, *Polimi, IT*
Co-Chair	**Jose L. Ayala**, *Complutense University of Madrid, ES*

Session Title	**Power Modeling and Power Aware Synthesis**
Session Code / Room	**6.4 / Konferenz 2**
Date / Time	**Wednesday, 16 March 2016 / 11:00 – 12:30**
Chair	**Alberto Garcia Ortiz**, *University of Bremen, DE*
Co-Chair	**Qi Zhu**, *UCR, US*

Session Title	**Biochips**
Session Code / Room	**6.5 / Konferenz 3**
Date / Time	**Wednesday, 16 March 2016 / 11:00 – 12:30**
Chair	**Robert Wille**, *JKU, AT*
Co-Chair	**Ian O'Connor**, *Ecole Centrale de Lyon, FR*

6.5.1
11:00 – 11:30
Architecture Synthesis for Cost-Constrained Fault-Tolerant Flow-based Biochips 618
Morten Chabert Eskesen, Paul Pop and Seetal Potluri

6.5.2
11:30 – 12:00
Sieve-valve-aware Synthesis of Flow-based Microfluidic Biochips Considering Specific Biological Execution Limitations 624
Mengchu Li, Tsun-Ming Tseng, Bing Li, Tsung-Yi Ho and Ulf Schlichtmann

6.5.3
12:00 – 12:30
Integrated and Real-Time Quantitative Analysis Using Cyberphysical Digital-Microfluidic Biochips 630
Mohamed Ibrahim, Krishnendu Chakrabarty and Kristin Scott

Session Title	**Modelling and Control of Cyber-Physical Systems**
Session Code / Room	**6.6 / Konferenz 4**
Date / Time	**Wednesday, 16 March 2016 / 11:00 – 12:30**
Chair	**Donatella Sciuto**, *Politecnico di Milano, IT*
Co-Chair	**Paul Pop**, *Technical University of Denmark, DK*

6.6.1
11:00 – 11:30
Self-Triggered Controllers and Hard Real-Time Guarantees 636
Amir Aminifar, Paulo Tabuada, Petru Eles and Zebo Peng

6.6.2
11:30 – 12:00
A Spatio-Temporal Fractal Model for a CPS Approach to Brain-Machine-Body Interfaces 642
Yuankun Xue, Saul Rodriguez and Paul Bogdan

6.6.3
12:00 – 12:15
Modular Code Generation for Emulating the Electrical Conduction System of the Human Heart 648
Nathan Allen, Sidharta Andalam, Partha Roop, Avinash Malik, Mark Trew and Nitish Patel

6.6.4
12:15 – 12:30
Resource Utilization and Quality-of-Control Trade-off for a Composable Platform 654
Juan Valencia, E.P. (Eelco) van Horssen, Dip Goswami, W. P. M. H. (Maurice) Heemels and Kees Goossens

Session Title	**Fault Tolerant Systems and Methods**
Session Code / Room	**6.7 / Konferenz 5**
Date / Time	**Wednesday, 16 March 2016 / 11:00 – 12:30**
Chair	**Viacheslav Izosimov**, *Semcon Sweden AB, SE*
Co-Chair	**Zebo Peng**, *Linköping University, SE*

6.7.1
11:00 – 11:30
Inexact Designs for Approximate Low Power Addition by Cell Replacement 660
Haider A. F. Almurib, T. Nandha Kumar and Fabrizio Lombardi

6.7.2
11:30 – 12:00
A General Approach for Highly Defect Tolerant Parallel Prefix Adder Design 666
Soumya Banerjee and Wenjing Rao

6.7.3
12:00 – 12:30
Inverters' Self-Checking Monitors for Reliable Photovoltaic Systems 672
M. Omaña, A. Fiore and C. Metra

Session	**Lunch Time Keynote Session**
Session Code / Room	**7.0**
Date / Time	**Wednesday, 16 March 2016 / 14:00 – 14:30**
Chair	**Luca Fanucci**, *University of Pisa, IT*
Co-Chair	**Wolfgang Ecker**, *Infineon Technologies, DE*

7.0.1
14:00 – 14:30
[Keynote] The Car of the Future will reinvent personal mobility xxx
Patrick Leteinturier

Session Title	**SPECIAL DAY Panel: Which EDA Solutions can the Automotive Domain Reuse? Very Few or All?**
Session Code / Room	**7.1 / Saal 2**
Date / Time	**Wednesday, 16 March 2016 / 14:30 – 16:00**
Chair	**Adam Morawiec**, *European Chips & Systems Design Initiative (ESCI), FR*

7.1.2
14:30 – 16:00
Panelist
Rainer Kress

7.1.3
14:30 – 16:00
Panelist
Gabriele Ernst

7.1.4
14:30 – 16:00
Panelist
Jean-Marie Saint-Paul

7.1.5 **14:30 – 16:00**	Panelist *Silvano Motto*
7.1.6 **14:30 – 16:00**	Panelist *Christoph Störmer*
7.1.1 **14:30 – 16:00**	Moderator *Oliver Bringmann*

Session Title	**EU Projects Special Session: Energy Efficiency drives Design**
Session Code / Room	**7.2 / Konferenz 6**
Date / Time	**Wednesday, 16 March 2016 / 14:30 – 16:00**
Organiser	**Roberto Giorgi**, *University of Siena, IT*
Chair	**Martin Schoeberl**, *Technical University of Denmark, DK*
Co-Chair	**Roberto Giorgi**, *University of Siena, IT*

7.2.1 **14:30 – 14:45**	EUROSERVER: Share-Anything Scale-Out Micro-Server Design 678 *Manolis Marazakis, John Goodacre, Didier Fuin, Paul Carpenter, John Thomson, Emil Matus, Antimo Bruno, Per Stenstrom, Jerome Martin, Yves Durand and Isabelle Dor*
7.2.2 **14:45 – 15:00**	Energy Minimization at All Layers of the Data Center: The ParaDIME Project 684 *Oscar Palomar, Santhosh Rethinagiri, Gulay Yalcin, Ruben Titos-Gil, Pablo Prieto, Emma Torrella, Osman Unsal, Adrian Cristal, Pascal Felber, Anita Sobe, Yaroslav Hayduk, Mascha Kurpicz, Christof Fetzer, Thomas Knauth, Malte Schneegaß, Jens Struckmeier and Dragomir Milojevic*
7.2.3 **15:00 – 15:15**	Rack-scale Disaggregated Cloud Data Centers: The dReDBox Project Vision 690 *K. Katrinis, D. Syrivelis, D. Pnevmatikatos, G. Zervas, D. Theodoropoulos, I. Koutsopoulos, K. Hasharoni, D. Raho, C. Pinto, F. Espina, S. Lopez-Buedo, Q. Chen, M. Nemirovsky, D. Roca, H. Klos and T. Berends*
7.2.4 **15:15 – 15:30**	ECOSCALE: Reconfigurable Computing and Runtime System for Future Exascale Systems 696 *Iakovos Mavroidis, Ioannis Papaefstathiou, Luciano Lavagno, Dimitrios S. Nikolopoulos, Dirk Koch, John Goodacre, Ioannis Sourdis, Vassilis Papaefstathiou, Marcello Coppola and Manuel Palomino*
7.2.5 **15:30 – 15:45**	Enabling HPC for QoS-sensitive Applications: The MANGO Approach 702 *José Flich, Giovanni Agosta, Philipp Ampletzerz, David Atienza Alonso, Carlo Brandolese, Alessandro Cilardo, William Fornaciari, Ynse Hoornenborg, Mario Kovac, Bruno Maitre, Giuseppe Massari, Hrvoje Mlinarić, Ermis Papastefanakis, Fabrice Roudet, Rafael Tornero and Davide Zoni*

7.2.6 **15:45 – 16:00**	AutoTuning and Adaptivity appRoach for Energy Efficient eXascale HPC Systems: The ANTAREX Approach 708 *Cristina Silvano, Giovanni Agosta, Andrea Bartolini, Andrea R. Beccari, Luca Benini, João Bispo, Radim Cmar, João M. P. Cardoso, Carlo Cavazzoni, Jan Martinovic, Gianluca Palermo, Martin Palkovic, Pedro Pinto, Erven Rohou, Nico Sanna and Katerina Slaninová*

Session Title	**Low Power Devices and Methods for Healthcare and Assisted Living**
Session Code / Room	**7.3 / Konferenz 1**
Date / Time	**Wednesday, 16 March 2016 / 14:30 – 16:00**
Chair	**José M. Moya**, *Technical University of Madrid, ES*
Co-Chair	**Giovanni Ansaloni**, *University of Lugano, CH*

7.3.1 **14:30 – 15:00**	A Digital Processor Architecture for Combined EEG/EMG Falling Risk Prediction 714 *V. F. Annese, M. Crepaldi, D. Demarchi and D. De Venuto*
7.3.2 **15:00 – 15:30**	Distributed-neuron-network based Machine Learning on Smart-gateway Network Towards Real-time Indoor Data Analytics 720 *Hantao Huang, Yuehua Cai and Hao Yu*
7.3.3 **15:30 – 15:45**	Touch-Based System for Beat-to-Beat Impedance Cardiogram Acquisition and Hemodynamic Parameters Estimation 726 *Dionisije Sopic, Srinivasan Murali, Francisco Rincón and David Atienza*
7.3.4 **15:45 – 16:00**	Quantifying the Benefits of Compressed Sensing on a WBSN-based Real-Time Biosignal Monitor 732 *Daniele Bortolotti, Bojan Milosevic, Andrea Bartoliniy, Elisabetta Farellaand Luca Benini*

Session Title	**System-Level Synthesis**
Session Code / Room	**7.4 / Konferenz 2**
Date / Time	**Wednesday, 16 March 2016 / 14:30 – 16:00**
Chair	**Cathal McCabe**, *Xilinx, Inc. Ireland, IE*
Co-Chair	**Yuichi Nakamura**, *NEC Japan, JP*

7.4.1 **14:30 – 15:00**	System Level Synthesis for Virtual Memory Enabled Hardware Threads 738 *Nicolas Estibals, Gaël Deest, Ali Hassan El Moussawi and Steven Derrien*
7.4.2 **15:00 – 15:30**	Composable, Parameterizable Templates for High-Level Synthesis 744 *Janarbek Matai, Dajung Lee, Alric Althoff and Ryan Kastner*

7.4.3 **15:30 – 16:00**	Leveraging Power Spectral Density for Scalable System-Level Accuracy Evaluation 750 *Benjamin Barrois, Karthick Parashar and Olivier Sentieys*

Session Title	**Emerging Memory Architectures**
Session Code / Room	**7.5 / Konferenz 3**
Date / Time	**Wednesday, 16 March 2016 / 14:30 – 16:00**
Chair	**Amara Amara**, *ISEP, FR*
Co-Chair	**Fabian Oboril**, *Karlsruhe Institute of Technology, DE*
7.5.1 **14:30 – 15:00**	Leader: Accelerating ReRAM-based Main Memory by Leveraging Access Latency Discrepancy in Crossbar Arrays 756 *Hang Zhang, Nong Xiao, Fang Liu and Zhiguang Chen*
7.5.2 **15:00 – 15:30**	Sliding Basket: An Adaptive ECC Scheme for Runtime Write Failure Suppression of STT-RAM Cache* 762 *Xue Wang, Mengjie Mao, Enes Eken, Wujie Wen, Hai Li and Yiran Chen*
7.5.3 **15:30 – 16:00**	Exploiting More Parallelism from Write Operations on PCM 768 *Zheng Li, Fang Wang, Yu Hua, Wei Tong, Jingning Liu, Yu Chen and Dan Feng*

Session Title	**Statistical and Symbolic Techniques for the Analysis and Testing of Embedded Software**
Session Code / Room	**7.6 / Konferenz 4**
Date / Time	**Wednesday, 16 March 2016 / 14:30 – 16:00**
Chair	**Jian-Jia Chen**, *Technische Universität Dortmund, DE*
Co-Chair	**Petru Eles**, *Linköping University, SE*
7.6.1 **14:30 – 15:00**	Dynamic Partitioning Strategy to Enhance Symbolic Execution 774 *Brendan A. Marcellino and Michael S. Hsiao*
7.6.2 **15:00 – 15:30**	Quantitative Timing Analysis of UML Activity Diagrams Using Statistical Model Checking 780 *Fan Gu, Xinqian Zhang, Mingsong Chen, Daniel Große and Rolf Drechsler*
7.6.3 **15:30 – 16:00**	Integrating Symbolic and Statistical Methods for Testing Intelligent Systems Applications to Machine Learning and Computer Vision 786 *Arvind Ramanathan, Laura L. Pullum, Faraz Hussain, Dwaipayan Chakrabarty and Sumit Kumar Jha*

Session Title	Aging Mitigation to Improve System Robustness
Session Code / Room	7.7 / Konferenz 5
Date / Time	Wednesday, 16 March 2016 / 14:30 – 16:00
Chair	**Maria Michael**, *University of Cyprus, CY*
Co-Chair	**Carles Hernandez**, *Barcellona Supercomputer Center, ES*

7.7.1
14:30 – 15:00
Path Selection and Sensor Insertion Flow for Age Monitoring in FPGAs 792
Mohammad Ebrahimi, Zana Ghaderi, Eli Bozorgzadeh and Zain Navabi

7.7.2
15:00 – 15:30
Design and Evaluation of Reliability-oriented Task Re-Mapping in MOSoCs using Time-Series Analysis of Intermittent Faults 798
Siva Satyendra Sahoo, Akash Kumar and Bharadwaj Veeravalli

7.7.3
15:30 – 16:00
Lifetime-aware Load Distribution Policies in Multi-core Systems: An In-depth Analysis 804
Cristiana Bolchini, Luca Cassano and Antonio Miele

Session Title	Interactive Presentations
Session Code / Room	IP3
Date / Time	Wednesday, 16 March 2016 / 16:00 – 16:30

IP3-1
A Flexible Inexact TMR Technique for SRAM-based FPGAs 810
Shyamsundar Venkataraman, Rui Santos and Akash Kumar

IP3-2
Accurate Verification of RC Power Grids 814
Mohammad Fawaz and Farid N. Najm

IP3-3
Security-Aware Development of Cyber-Physical Systems Illustrated with Automotive Case Study 818
Viacheslav Izosimov, Alexandros Asvestopoulos, Oscar Blomkvist and Martin Törngren

IP3-4
Online Heuristic for the Multi-objective Generalized Traveling Salesman Problem 822
Joost van Pinxten, Marc Geilen, Twan Basten, Umar Waqas and Lou Somers

IP3-5
Towards Low Overhead Control Flow Checking Using Regular Structured Control 826
Zhiqi Zhu and Joseph Callenes-Sloan

IP3-6
Emulation-Based Hierarchical Fault-Injection Framework for Coarse-to-Fine Vulnerability Analysis of Hardware-Accelerated Approximate Algorithms 830
Ioannis Chadjiminas, Ioannis Savva, Christos Kyrkou, Maria K. Michael and Theocharis Theocharides

Session Title	**EU Projects Special Session: Towards Better EU-projects – Success Stories**
Session Code / Room	**8.2 / Konferenz 6**
Date / Time	**Wednesday, 16 March 2016 / 17:00 – 18:30**
Organiser	**Roberto Giorgi**, *University of Siena, IT*
Chair	**Cristina Silvano**, *Politecnico of Milan, IT*
Co-Chair	**Roberto Giorgi**, *University of Siena, IT*

8.2.1
17:00 – 17:15
Collective Knowledge: Towards R&D Sustainability 864
Grigori Fursin, Anton Lokhmotov and Ed Plowman

8.2.2
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Lessons Learned from the EU Project T-CREST 870
Martin Schoeberl

8.2.3
17:30 – 17:45
MULTI-POS: Marie Curie Network in Multi-technology Positioning 876
Jari Nurmi and Elena-Simona Lohan

8.2.4
17:45 – 18:00
Program Transformations in the POLCA Project 882
Jan Kuper, Lutz Schubert, Kilian Kempf, Colin Glass, Daniel Rubio Bonilla and Manuel Carro

8.2.5
18:00 – 18:15
Computation and Communication Challenges to Deploy Robots in Assisted Living Environments 888
Georgios Keramidas, Christos Antonopoulos, Nikolaos S. Voros, Fynn Schwiegelshohn, Philipp Wehner, Jens Rettkowski, Diana Göhringer, Michael Hübner, Stasinos Konstantopoulos, Theodore Giannakopoulos, Vangelis Karkaletsis and Vaggelis Mariatos

8.2.6
18:15 – 18:30
ATHENIS_3D: Automotive Tested High-voltage and Embedded Non-volatile Integrated SoC Platform with 3D Technology 894
E. Wachmann, S. Saponara, C. Zambelli, P. Tisserand, J. Charbonnier, T. Erlbacher, S. Gruenler, C. Hartler, J. Siegert, P. Chassard, D. M. Ton, L. Ferrari and L. Fanucci

Session Title	**Hot Topic: Managing Heterogeneous Computing Resources at Runtime**
Session Code / Room	**8.3 / Konferenz 1**
Date / Time	**Wednesday, 16 March 2016 / 17:00 – 18:30**
Organisers	**Christian Plessl**, *University of Paderborn, DE* **David Andrews**, *University of Arkansas, US*
Chair	**Daniel Ziener**, *Hamburg University of Technology, DE*
Co-Chair	**José L. Ayala**, *Complutense University of Madrid, ES*

8.3.1
17:00 – 17:30
Run Time Interpretation for Creating Custom Accelerators 900
Sen Ma, Zeyad Aklah and David Andrews

8.3.2
17:30 – 18:00
A Self-Adaptive Approach to Efficiently Manage Energy and Performance in Tomorrow's Heterogeneous Computing Systems 906
E. M. G. Trainiti, G. C. Durelli, A. Miele, C. Bolchini and M. D. Santambrogio

8.3.3
18:00 – 18:30
Performance-Centric Scheduling with Task Migration for a Heterogeneous Compute Node in the Data Center 912
Achim Lösch, Tobias Beisel, Tobias Kenter, Christian Plessl and Marco Platzner

Session Title	**Advanced Methods in High-Level Design**
Session Code / Room	**8.4 / Konferenz 2**
Date / Time	**Wednesday, 16 March 2016 / 17:00 – 18:30**
Chair	**Fabian Oboril**, *KIT Germany, DE*
Co-Chair	**Luciano Lavagno**, *Politecnico di Torino, IT*

8.4.1
17:00 – 17:30
Adaptive Threshold Non-Pareto Elimination: Re-thinking Machine Learning for System Level Design Space Exploration on FPGAs 918
Pingfan Meng, Alric Althoff, Quentin Gautier and Ryan Kastner

8.4.2
17:30 – 18:00
Monitoring of MTL Specifications With IBM's Spiking-Neuron Model 924
Konstantin Selyunin, Thang Nguyen, Ezio Bartocci, Dejan Nickovic and Radu Grosu

8.4.3
18:00 – 18:30
Formal Probabilistic Analysis of Distributed Resource Management Schemes in On-Chip Systems 930
Shafaq Iqtedar, Osman Hasan, Muhammad Shafique and Jörg Henkel

Session Title	Non-volatile Memory Design Methodologies
Session Code / Room	8.5 / Konferenz 3
Date / Time	Wednesday, 16 March 2016 / 17:00 – 18:30
Chair	**Michael Huebner**, *RUB, DE*
Co-Chair	**Michael Niemier**, *University of Notre Dame, US*

8.5.1
17:00 – 17:30
An Operating System Level Data Migration Scheme in Hybrid DRAM-NVM Memory Architecture 936
Reza Salkhordeh and Hossein Asadi

8.5.2
17:30 – 18:00
Unified DRAM and NVM Hybrid Buffer Cache Architecture for Reducing Journaling Overhead 942
Zhiyong Zhang, Lei Ju and Zhiping Jia

8.5.3
18:00 – 18:30
Fast Logic Synthesis for RRAM-based In-Memory Computing using Majority-Inverter Graphs 948
Saeideh Shirinzadeh, Mathias Soeken, Pierre-Emmanuel Gaillardon and Rolf Drechsler

Session Title	Dataflow Modeling and Natural Language Processing
Session Code / Room	8.6 / Konferenz 4
Date / Time	Wednesday, 16 March 2016 / 17:00 – 18:30
Chair	**Dominique Borrione**, *Laboratoire TIMA, FR*
Co-Chair	**Marc Geilen**, *Eindhoven University of Technology, NL*

8.6.1
17:00 – 17:30
Exploiting Resource-constrained Parallelism in Hard Real-Time Streaming Applications 954
Jelena Spasic, Di Liu and Todor Stefanov

8.6.2
17:30 – 18:00
Transaction Parameterized Dataflow: A Model for Context-Dependent Streaming Applications 960
Xuan Khanh Do, Stephane Louise and Albert Cohen

8.6.3
18:00 – 18:30
GLAsT: Learning Formal Grammars to Translate Natural Language Specifications into Hardware Assertions 966
Christopher B. Harris and Ian G. Harris

Session Title	**Test Methods Handling Unkowns, 2.50 Integration and Realistic Memory Defects**
Session Code / Room	**8.7 / Konferenz 5**
Date / Time	**Wednesday, 16 March 2016 / 17:00 – 18:30**
Chair	**Friedrich Hapke**, *Mentor Graphics Hamburg, DE*

8.7.1
17:00 – 17:30
Accurate CEGAR-based ATPG in Presence of Unknown Values for Large Industrial Designs 972
Karsten Scheibler, Dominik Erb and Bernd Becker

8.7.2
17:30 – 18:00
Pre-Bond Testing of the Silicon Interposer in 2.5D ICs 978
Ran Wang, Zipeng Li, Sukeshwar Kannan and Krishnendu Chakrabarty

8.7.3
18:00 – 18:30
Improving SRAM Test Quality by Leveraging Self-timed Circuits 984
Josef Kinseher, Leonardo B. Zordan, Ilia Polian and Andreas Leininger

Session Title	**SPECIAL DAY Embedded Tutorial: Embedded Systems Security**
Session Code / Room	**9.1 / Saal 2**
Date / Time	**Thursday, 17 March 2016 / 08:30 – 10:00**
Chair	**Matthias Schunter**, *Intel, DE*
Co-Chair	**Wieland Fischer**, *Infineon Technologies, DE*

9.1.1
08:30 – 10:00
Software Security: Vulnerabilities and Countermeasures for Two Attacker Models 990
Frank Piessens and Ingrid Verbauwhede

Session Title	**Managing the Traffic Jam in NoC**
Session Code / Room	**9.2 / Konferenz 6**
Date / Time	**Thursday, 17 March 2016 / 08:30 – 10:00**
Chair	**Nader Bagherzadeh**, *University of California Irvine, US*
Co-Chair	**Massoud Daneshtalab**, *KTH, SE*

9.2.1
08:30 – 09:00
OLITS: An Ohm's Law-like Traffic Splitting Model Based on Congestion Prediction 1000
Gaoming Du, Yanghao Ou, Xiangyang Li, Ping Song, Zhonghai Lu and Minglun Gao

9.2.2
09:00 – 09:30
MCAPI-compliant Hardware Buffer Manager Mechanism to Support Communication in Multi-Core Architectures 1006
Thiago Raupp da Rosa, Thomas Mesquida, Romain Lemaire and Fabien Clermidy

9.2.3 **09:30 – 10:00**	Slack-Based Resource Arbitration for Real-Time Networks-On-Chip 1012 *Adam Kostrzewa, Selma Saidi and Rolf Ernst*

Session Title	**Industrial Experiences**
Session Code / Room	**9.3 / Konferenz 1**
Date / Time	**Thursday, 17 March 2016 / 08:30 – 10:00**
Chair	**Norbert Wehn**, *University of Kaiserslautern, DE*
Co-Chair	**Stephan Diestelhorst**, *ARM, US*

9.3.1 **08:30 – 08:45**	Challenges of Using On-Chip Performance Monitors for Process and Environmental Variation Compensation 1018 *Mahroo Zandrahimi, Zaid Al-Ars, Philippe Debaudand Armand Castillejo*
9.3.2 **08:45 – 09:00**	Study of Workload Impact on BTI HCI Induced Aging of Digital Circuits 1020 *Ajith Sivadasan, Florian Cacho, Sidi Ahmed Benhassain, Vincent Huard and Lorena Anghel*
9.3.3 **09:00 – 09:15**	Fast Prototyping Platform for Navigation Systems with Sensors Fusion 1022 *Charly Bechara, Karim Ben Chehida, Mickael Guibert, Renaud Schmit, Maria Lepecq, Laurent Soulier, Thomas Dombek and Yann Leclerc*
9.3.4 **09:15 – 09:30**	Precision Timed Industrial Automation Systems 1024 *Matthew M. Y. Kuo, Sidharta Andalam and Partha S. Roop*
9.3.5 **09:30 – 09:45**	AUTOSAR-based Communication Coprocessor for Automotive ECUs 1026 *Ahmed Hamed, Mona Safar, M. Watheq El-Kharashiand Ashraf Salem*
9.3.6 **09:45 – 10:00**	Mantissa-Masking for Energy-Efficient Floating-Point LTE Uplink MIMO Baseband Processing 1028 *D. Guenther, T. Henriksson, R. Leupers, G. Ascheid*

Session Title	**Optimization for Logic and Physical Design**
Session Code / Room	**9.4 / Konferenz 2**
Date / Time	**Thursday, 17 March 2016 / 08:30 – 10:00**
Chair	**Valeria Bertacco**, *Univ. of Michigan, US*
Co-Chair	**Sven Peyer**, *IBM, DE*

9.4.1 **08:30 – 09:00**	Optimizing Majority-Inverter Graphs With Functional Hashing 1030 *Mathias Soeken, Luca Gaetano Amarù, Pierre-Emmanuel Gaillardon and Giovanni De Micheli*
9.4.2 **09:00 – 09:30**	Resource-Aware Functional ECO Patch Generation 1036 *An-Che Cheng, Iris Hui-Ru Jiang and Jing-Yang Jou*

9.4.3 **09:30 – 10:00**	Simultaneous Slack Matching, Gate Sizing and Repeater Insertion for Asynchronous Circuits 1042 *Gang Wu and Chris Chu*

Session Title	**Formal Bit Precise Reasoning**
Session Code / Room	**9.5 / Konferenz 3**
Date / Time	**Thursday, 17 March 2016 / 08:30 – 10:00**
Chair	**Markus Wedler**, *Synopsys GmbH, DE*
Co-Chair	**Julien Schmaltz**, *Eindhoven University of Technology, NL*

9.5.1 **08:30 – 09:00**	Formal Verification of Integer Multipliers by Combining Gröbner Basis with Logic Reduction 1048 *Amr Sayed-Ahmed, Daniel Große, Ulrich Kühne, Mathias Soeken and Rolf Drechsler*
9.5.2 **09:00 – 09:30**	Root-Cause Analysis for Memory-Locked Errors 1054 *John Adler, Djordje Maksimovic and Andreas Veneris*
9.5.3 **09:30 – 10:00**	Formal Verification of Clock Domain Crossing using Gate-level Models of Metastable Flip-Flops 1060 *Ghaith Tarawneh, Andrey Mokhov and Alex Yakovlev*

Session Title	**Real-Time Scheduling**
Session Code / Room	**9.6 / Konferenz 4**
Date / Time	**Thursday, 17 March 2016 / 08:30 – 10:00**
Chair	**Frank Slomka**, *Universität Ulm, DE*
Co-Chair	**Kai Lampka**, *Uppsala University, SE*

9.6.1 **08:30 – 09:00**	Response-Time Analysis of DAG Tasks under Fixed Priority Scheduling with Limited Preemptions 1066 *Maria A. Serrano, Alessandra Melani, Marko Bertogna and Eduardo Quinones*
9.6.2 **09:00 – 09:30**	Speed Optimization for Tasks with Two Resources 1072 *Alessandra Melani, Renato Mancuso, Daniel Cullina, Marco Caccamo and Lothar Thiele*
9.6.3 **09:30 – 10:00**	Self-Suspension Real-Time Tasks under Fixed-Relative-Deadline Fixed-Priority Scheduling 1078 *Wen-Hung Huang and Jian-Jia Chen*

Session Title	**Temperature Awareness in Computing Systems**
Session Code / Room	**9.7 / Konferenz 5**
Date / Time	**Thursday, 17 March 2016 / 08:30 – 10:00**
Chair	**Muhammad Shafique**, *Karlsruhe Institute of Technology, DE*
Co-Chair	**Marina Zapater**, *Complutense University of Madrid, ES*

9.7.1
08:30 – 09:00
Thermal-aware Dynamic Page Allocation Policy by Future Access Patterns for Hybrid Memory Cube (HMC) 1084
Wei-Hen Lo, Kai-zen Liang and TingTing Hwang

9.7.2
09:00 – 09:30
Minimizing Peak Temperature for Pipelined Hard Real-time Systems 1090
Long Cheng, Kai Huang, Gang Chen, Biao Hu and Alois Knoll

9.7.3
09:30 – 10:00
Thermal Aware Scheduling and Mapping of Multiphase Applications onto Chip Multiprocessor 1096
Aryabartta Sahu

Session Title	**Embedded Tutorial: Analog-/Mixed-Signal Verification Methods for AMS Coverage Analysis**
Session Code / Room	**9.8 / Exhibition Theater**
Date / Time	**Thursday, 17 March 2016 / 08:30 – 10:00**
Organisers	**Gregor Nitsche**, *OFFIS, DE*
Chair	**Lars Hedrich**, *Johann Wolfgang Goethe-Universität, DE*
Co-Chair	**Christoph Grimm**, *University of Kaiserslautern, DE*

9.8.0
08:30 – 10:00
Embedded Tutorial: Analog-/Mixed-Signal Verification Methods for AMS Coverage Analysis 1102
Erich Barke, Andreas Fürtig, Georg Gläser, Christoph Grimm, Lars Hedrich, Stefan Heinen, Eckhard Hennig, Hyun-Sek Lukas Lee, Wolfgang Nebel, Gregor Nitsche, Markus Olbrich, Carna Radojicic and Fabian Speicher

9.8.1
08:30 – 09:00
Towards More Dependable Verification Using Symbolic Simulation N/A
Carna Radojicic, Christoph Grimm, Fabian Speicher and Stefan Heinen

9.8.2
09:00 – 09:30
Identification of Critical Scenarios in AMS Verification: Methodology for Finding the Safe Operating Area of AMS Systems N/A
Georg Gläser, Hyun-Sek Lukas Lee, Markus Olbrich, Erich Barke and Eckhard Hennig

9.8.3
09:30 – 10:00
AMS Leaf-Component Characterization with Contracts and Satisfaction Checking vs. Electronic Circuit Schematics N/A
Gregor Nitsche, Andreas Fürtig, Lars Hedrich and Wolfgang Nebel

Session Title	Interactive Presentations
Session Code / Room	IP4
Date / Time	Thursday, 17 March 2016 / 10:00 – 10:30

IP4-1 A *q*-gram Birthmarking Approach to Predicting Reusable Hardware 1112
Kevin Zeng and Peter Athanas

IP4-2 Captopril: Reducing the Pressure of Bit Flips on Hot Locations in Non-Volatile Main Memories 1116
Majid Jalili and Hamid Sarbazi-Azad

IP4-3 Handling Complex Dependencies in System Design 1120
Mischa Moestl and Rolf Ernst

IP4-4 A Synthesis-Agnostic Behavioral Fault Model for High Gate-Level Fault Coverage 1124
Anton Karputkin and Jaan Raik

IP4-6 Combining Graph-based Guidance with Error Effect Simulation for Efficient Safety Analysis 1132
Jo Laufenberg, Sebastian Reiter, Alexander Viehl, Oliver Bringmann, Thomas Kropf and Wolfgang Rosenstiel

IP4-7 Packet Security with Path Sensitization for NoCs 1136
Travis Boraten and Avinash Karanth Kodi

IP4-8 Synthesis of Approximate Coders for On-chip Interconnects Using Reversible Logic 1140
Robert Wille, Oliver Keszocze, Stefan Hillmich, Marcel Walter and Alberto Garcia-Ortiz

IP4-9 Design-Synthesis Co-Optimisation Using Skewed and Tapered Gates 1144
Ayan Datta, James D. Warnock, Ankur Shukla, Saurabh Gupta, Yiu. H. Chan, Karthik Mohan and Charudhattan Nagarajan

IP4-10 A Synthesis-Parameter Tuning System for Autonomous Design-Space Exploration 1148
Matthew M. Ziegler, Hung-Yi Liu, George Gristede, Bruce Owens, Ricardo Nigaglioni and Luca P. Carloni

IP4-11 Unbounded Safety Verification for Hardware Using Software Analyzers 1152
Rajdeep Mukherjee, Peter Schrammel, Daniel Kroening and Tom Melham

IP4-12 Verilog2SMV: A Tool for Word-level Verification 1156
Ahmed Irfan, Alessandro Cimatti, Alberto Griggio, Marco Roveri and Roberto Sebastiani

IP4-13 Towards Formal Verification of Real-World SystemC TLM Peripheral Models — A Case Study 1160
Hoang M. Le, Vladimir Herdt, Daniel Große and Rolf Drechsler

IP4-14	Frequency Scheduling For Resilient Chip Multi-Processors Operating at Near Threshold Voltage 1164 *Ying Wang, Huawei Li and Xiaowei Li*
IP4-15	A Low Overhead Error Confinement Method based on Application Statistical Characteristics 1168 *Zheng Wang, Georgios Karakonstantis and Anupam Chattopadhyay*

Session Title	**SPECIAL DAY Hot Topic: Lightweight Security for Embedded Processors**
Session Code / Room	**10.1 / Saal 2**
Date / Time	**Thursday, 17 March 2016 / 11:00 – 12:30**
Chair	**Tilo Müller**, *Friedrich-Alexander-Universität Erlangen-Nürnberg, DE*
Co-Chair	**Patrick Schaumont**, *Virginia Tech, US*
10.1.1 **11:00 – 11:30**	Scaling Down: Lightweight Approaches to IoT Security N/A *Patrick Koeberl*
10.1.2 **11:30 – 12:00**	SOFIA: Software and Control Flow Integrity Architecture 1172 *Ruan de Clercq, Ronald De Keulenaer, Bart Coppens, Bohan Yang, Pieter Maene, Koen de Bosschere, Bart Preneel, Bjorn de Sutter and Ingrid Verbauwhede*
0.1.3 **12:00 – 12:30**	Trust, But Verify: Why and How to Establish Trust in Embedded Devices 1178 *Aurélien Francillon*

Session Title	**Does it Work or NoC?**
Session Code / Room	**10.2 / Konferenz 6**
Date / Time	**Thursday, 17 March 2016 / 11:00 – 12:30**
Chair	**Davide Bertozzi**, *University of Ferrara, IT*
Co-Chair	**Kees Goossens**, *Eindhoven University of Technology, NL*
10.2.1 **11:00 – 11:30**	CrossOver: Clock Domain Crossing under Virtual-Channel Flow Control 1183 *Michalis Paschou, Anastasios Psarras, Chrysostomos Nicopoulos and Giorgos Dimitrakopoulos*
10.2.2 **11:30 – 12:00**	Correct Runtime Operation for NoCs through Adaptive-Region Protection 1189 *Rawan Abdel-Khalek and Valeria Bertacco*
10.2.3 **12:00 – 12:30**	Fault-Tolerant 3-D Network-on-Chip Design using Dynamic Link Sharing 1195 *Seyyed Hossein Seyyedaghaei Rezaei, Mehdi Modarressi, Reza Yazdani Aminabadi and Masoud Daneshtalab*

Session Title	**Design Experiences for Multimedia and Communication Applications**
Session Code / Room	**10.3 / Konferenz 1**
Date / Time	**Thursday, 17 March 2016 / 11:00 – 12:30**
Chair	**Theocharis THEOCHARIDES**, *University of Cyprus, CY*
Co-Chair	**Steffen Paul**, *University Bremen, DE*

10.3.1
11:00 – 11:30
Enabling the Heterogeneous Accelerator Model on Ultra-Low Power Microcontroller Platforms 1201
Francesco Conti, Daniele Palossi, Andrea Marongiu, Davide Rossi and Luca Benini

10.3.2
11:30 – 12:00
Thermal Optimization using Adaptive Approximate Computing for Video Coding 1207
Daniel Palomino, Muhammad Shafique, Altamiro Susin and Jörg Henkel

10.3.3
12:00 – 12:15
High Performance Time-of-Flight and Color Sensor Fusion with Image-Guided Depth Super Resolution 1213
Hannes Plank, Gerald Holweg, Thomas Herndl and Norbert Druml

10.3.4
12:15 – 12:30
Saturated Min-Sum Decoding: An "Afterburner" for LDPC Decoder Hardware 1219
S. Scholl, P. Schläfer and N. When

Session Title	**Stochastic Methods for Circuit Analysis & Synthesis**
Session Code / Room	**10.4 / Konferenz 2**
Date / Time	**Thursday, 17 March 2016 / 11:00 – 12:30**
Chair	**Michal Rewienski**, *Technical University of Gdansk, PL*
Co-Chair	**L. Miguel Silveira**, *INESC-ID, IST, U Lisboa, PT*

10.4.1
11:00 – 11:30
Utilizing Macromodels in Floating Random Walk Based Capacitance Extraction 1225
Wenjian Yu, Bolong Zhang, Chao Zhang, Haiquan Wang and Luca Daniel

10.4.2
11:30 – 12:00
Variability and Statistical Analysis Flow for Dynamic Linear Systems with Large Number of Inputs 1231
A. Lucas Martins, Jorge Fernández Villena and L. Miguel Silveira

10.4.3
12:00 – 12:30
Variation-Aware Near Threshold Circuit Synthesis 1237
Mohammad Saber Golanbari, Saman Kiamehr, Mojtaba Ebrahimi and Mehdi B. Tahoori

Session Title	Enhancing Memory in Next-Generation Platforms
Session Code / Room	10.5 / Konferenz 3
Date / Time	Thursday, 17 March 2016 / 11:00 – 12:30
Chair	**Fancisco Cazorla**, *Barcelona Supercomputing Center, ES*
Co-Chair	**Jeronimo Castrillon**, *Technische Universität Dresden, DE*

10.5.1
11:00 – 11:30
Buffered Compares: Excavating the Hidden Parallelism Inside DRAM Architectures with Lightweight Logic 1243
Jinho Lee, Jung Ho Ahn and Kiyoung Choi

10.5.2
11:30 – 12:00
Large Vector Extensions Inside the HMC 1249
Marco A. Z. Alves, Matthias Diener, Paulo C. Santos and Luigi Carro

10.5.3
12:00 – 12:30
minFlash: A Minimalistic Clustered Flash Array 1255
Ming Liu, Sang-Woo Jun, Sungjin Lee, Jamey Hicks and Arvind

Session Title	Compilers and Tools for GPUs and MPSoCs
Session Code / Room	10.6 / Konferenz 4
Date / Time	Thursday, 17 March 2016 / 11:00 – 12:30
Chair	**Frank Hannig**, *University of Erlangen-Nürnberg, DE*
Co-Chair	**Lars Bauer**, *Karlsruhe Institute of Technology, DE*

10.6.1
11:00 – 11:30
An Optimized Task-Based Runtime System for Resource-Constrained Parallel Accelerators 1261
Daniele Cesarini, Andrea Marongiu and Luca Benini

10.6.2
11:30 – 12:00
A Fine-grained Performance Model for GPU Architectures 1267
Nicola Bombieri, Federico Busato and Franco Fummi

10.6.3
12:00 – 12:15
Critical Points Based Register-Concurrency Autotuning for GPUs 1273
Ang Li, Shuaiwen Leon Song, Akash Kumar, Eddy Z. Zhang, Daniel Chavarrìa-Miranda and Henk Corporaal

10.6.4
12:15 – 12:30
GRATER: An Approximation Workflow for Exploiting Data-Level Parallelism in FPGA Acceleration 1279
Atieh Lotfi, Abbas Rahimi, Amir Yazdanbakhsh, Hadi Esmaeilzadeh and Rajesh K. Gupta

Session Title	**Reliable System Design**
Session Code / Room	**10.7 / Konferenz 5**
Date / Time	**Thursday, 17 March 2016 / 11:00 – 12:30**
Chair	**Mohamed Sabry Aly**, *Stanford University, US*
Co-Chair	**Semeen Rehman**, *Karlsruhe Institute of Technology, DE*

10.7.1
11:00 – 11:30
A Holistic Tri-region MLC STT-RAM Design with Combined Performance, Energy, and Reliability Optimizations 1285
Wujie Wen, Mengjie Mao, Hai Li, Yiran Chen, Yukui Pei and Ning Ge

10.7.2
11:30 – 12:00
Thermal-aware TSV Repair for Electromigration in 3D ICs 1291
Shengcheng Wang, Mehdi B. Tahoori and Krishnendu Chakrabarty

10.7.3
12:00 – 12:30
Electrothermal Simulation of Bonding Wire Degradation under Uncertain Geometries 1297
Thorben Casper, Herbert De Gersem, Renaud Gillon, Tomas Gotthans, Tomas Kratochvil, Peter Meuris, Sebastian Schöps

Session Title	**Lunch Time Keynote Session**
Session Code / Room	**11.0**
Date / Time	**Thursday, 17 March 2016 / 13:30 – 14:00**
Chair	**Luca Fanucci**, *University of Pisa, IT*
Co-Chair	**Matthias Schunter**, *Intel Corporation, DE*

11.0.1
13:30 – 14:00
[Keynote] Secure Silicon: Enabler for the Internet of Things xxxi
Walden C. Rhines

Session Title	**SPECIAL DAY Hot Topic: Embedded Security Applications**
Session Code / Room	**11.1 / Saal 2**
Date / Time	**Thursday, 17 March 2016 / 14:00 – 15:30**
Chair	**Tim Güneysu**, *University of Bremen, DE*
Co-Chair	**X. Sharon Hu**, *University of Notre Dame, US*

11.1.1
14:00 – 14:30
Smart Grid Security
Klaus Kursawe

11.1.2
14:30 – 15:00
Security In Industrie 4.0 — Challenges and Solutions for the Fourth Industrial Revolution 1303
Michael Waidner and Michael Kasper

11.1.3 **15:00 – 15:30**	Security for Automotive and the Internet of Things N/A *Paul Duplys, Hans Löhr, Herve Seudie and Robert Szerwinski*

Session Title	**Beating New Technology Paths for NoC**
Session Code / Room	**11.2 / Konferenz 6**
Date / Time	**Thursday, 17 March 2016 / 14:00 – 15:30**
Chair	**Partha Pande**, *WSU, US*
Co-Chair	**Sébastien Le Beux**, *Le Beux, FR*

11.2.1 **14:00 – 14:30**	Cross-layer Floorplan Optimization For Silicon Photonic NoCs In Many-core Systems 1309 *Ayse K. Coskun, Anjun Gu, Warren Jin, Ajay Joshi, Andrew B. Kahng, Jonathan Klamkin, Yenai Ma, John Recchio, Vaishnav Srinivas and Tiansheng Zhang*
11.2.2 **14:30 – 15:00**	Adaptive Multi-Voltage Scaling in Wireless NoC for High Performance Low Power Applications 1315 *Hemanta Kumar Mondal, Sri Harsha Gade, Raghav Kishore and Sujay Deb*
11.2.3 **15:00 – 15:30**	Energy Efficient Transceiver in Wireless Network on Chip Architectures 1321 *Vincenzo Catania, Andrea Mineo, Salvatore Monteleone, Maurizio Palesi and Davide Patti*

Session Title	**Microarchitectures and Workload Allocation for Energy Efficiency**
Session Code / Room	**11.3 / Konferenz 1**
Date / Time	**Thursday, 17 March 2016 / 14:00 – 15:30**
Chair	**Andrea Bartolini**, *Univ. of Bologna, IT*
Co-Chair	**Andreas Burg**, *EPFL, CH*

11.3.1 **14:00 – 14:30**	Resistive Configurable Associative Memory for Approximate Computing 1327 *Mohsen Imani, Abbas Rahimi and Tajana S. Rosing*
11.3.2 **14:30 – 15:00**	Exploiting CPU-Load and Data Correlations in Multi-Objective VM Placement for Geo-Distributed Data Centers 1333 *Ali Pahlevan, Pablo Garcia del Valle and David Atienza*
11.3.3 **15:00 – 15:15**	Energy Efficiency in Cloud-Based MapReduce Applications through Better Performance Estimation 1339 *Seyed Morteza Nabavinejad and Maziar Goudarzi*
11.3.4 **15:15 – 15:30**	Unsupervised Power Modeling of Co-Allocated Workloads for Energy Efficiency in Data Centers 1345 *Juan C. Salinas-Hilburg, Marina Zapater, José L. Risco-Martín, José M. Moya and José L. Ayala*

Session Title	**Automating Test Generation, Assertions and Diagnosis**
Session Code / Room	**11.4 / Konferenz 2**
Date / Time	**Thursday, 17 March 2016 / 14:00 – 15:30**
Chair	**Pablo Sanchez**, *University of Cantabria, ES*
Co-Chair	**Ronny Morad**, *IBM, IL*

11.4.1
14:00 – 14:30
Automated Test Generation for Debugging Arithmetic Circuits 1351
Farimah Farahmandi and Prabhat Mishra

11.4.2
14:30 – 15:00
MCXplore: An Automated Framework for Validating Memory Controller Designs 1357
Mohamed Hassan and Hiren Patel

11.4.3
15:00 – 15:15
EAST: Efficient Assertion Simulation Techniques 1363
Debjyoti Bhattacharjee, Soumi Chattopadhyay and Ansuman Banerjee

11.4.4
15:15 – 15:30
Combinational Trace Signal Selection with Improved State Restoration for Post-Silicon Debug 1369
Siamack BeigMohammadi and Bijan Alizadeh

Session Title	**Design of Efficient Microarchitectures**
Session Code / Room	**11.5 / Konferenz 3**
Date / Time	**Thursday, 17 March 2016 / 14:00 – 15:30**
Chair	**Dionisios Pnevmatikatos**, *Technical University of Crete, GR*
Co-Chair	**Todd Austin**, *University of Michigan, US*

11.5.1
14:00 – 14:30
Practical Way Halting by Speculatively Accessing Halt Tags 1375
Daniel Moreau, Alen Bardizbanyan, Magnus Själander, David Whalley and Per Larsson-Edefors

11.5.2
14:30 – 15:00
Lazy Pipelines: Enhancing Quality in Approximate Computing 1381
G. Tziantzioulis, A. M. Gok, S. M. Faisal, N. Hardavellas, S. Ogrenci-Memik and S. Parthsarathy

11.5.3
15:00 – 15:30
High-Efficiency Logarithmic Number Unit Design based on an Improved Cotransformation Scheme 1387
Youri Popoff, Florian Scheidegger, Michael Schaffner, Michael Gautschi, Frank K. Gürkaynak and Luca Benini

Session Title	Applications of Reconfigurable Computing
Session Code / Room	11.6 / Konferenz 4
Date / Time	Thursday, 17 March 2016 / 14:00 – 15:30
Chair	**Alessandro Cilardo**, *University of Naples Federico II, IT*
Co-Chair	**Koen Bertels**, *Delft University of Technology, NL*

Session Title	Naked Analog Synthesis
Session Code / Room	11.7 / Konferenz 5
Date / Time	Thursday, 17 March 2016 / 14:00 – 15:30
Chair	**Árpád Árpád Bürmen**, *University of Ljubljana, SI*
Co-Chair	**Francisco Fernandez**, *IMSE-CNM, ES*

Session Title	Interactive Presentations
Session Code / Room	IP5
Date / Time	Thursday, 17 March 2016 / 15:30 – 16:00

Session Title	**SPECIAL DAY Hot Topic: Design Methods for Security and Trust**
Session Code / Room	**12.1 / Saal 2**
Date / Time	**Thursday, 17 March 2016 / 16:00 – 17:30**
Chair	**Jean-Luc Danger**, *Télécom ParisTech, FR*
Co-Chair	**Ilia Polian**, *Universität Passau, DE*

Session Title	**Hot Topic: Exploiting New Transistor Technologies to Enhance Hardware Security (without PUFs!)**
Session Code / Room	**12.2 / Konferenz 6**
Date / Time	**Thursday, 17 March 2016 / 16:00 – 17:30**
Organisers	**Michael Niemier**, *University of Notre Dame, South Bend, US*
Chair	**Sri Parameswaran**, *The University of New South Wales, AU*

12.2.1
16:00 – 16:30
Hardware Security Through Chain Assurance 1535
Yaw Obeng, Colm Nolan and David Brown

12.2.2
16:30 – 17:00
Leverage Emerging Technologies For DPA-Resilient Block Cipher Design 1538
Yu Bi, Kaveh Shamsi, Jiann-Shiun Yuan, Francois-Xavier Standaer and Yier Jin

12.2.3
17:00 – 17:30
Using Emerging Technologies for Hardware Security Beyond PUFs 1544
An Chen, X. Sharon Hu, Yier Jin, Michael Niemier and Xunzhao Yin

Session Title	**System Support for Resilience and Robustness**
Session Code / Room	**12.3 / Konferenz 1**
Date / Time	**Thursday, 17 March 2016 / 16:00 – 17:30**
Chair	**Oliver Bringmann**, *University of Tuebingen, DE*
Co-Chair	**Dirk Stroobandt**, *Ghent University, BE*

12.3.1
16:00 – 16:30
Effect of LFSR Seeding, Scrambling and Feedback Polynomial on Stochastic Computing Accuracy 1550
Jason H. Anderson, Yuko Hara-Azumi and Shigeru Yamashita

12.3.2
16:30 – 17:00
Efficient Program Tracing and Monitoring Through Power Consumption — With a Little Help from the Compiler 1556
Carlos Moreno, Sean Kauffman and Sebastian Fischmeister

12.3.3
17:00 – 17:15
FLIC: Fast, Lightweight Checkpointing for Mobile Virtualization using NVRAM 1562
Kan Zhong, Duo Liu, Liang Liang, Linbo Long, Yi Lin and Zili Shao

12.3.4
17:15 – 17:30
PAIS: Parallelization Aware Instruction Scheduling for Improving Soft-error Reliability of GPU-based Systems 1568
Haeseung Lee, Hsinchung Chen and Mohammad Abdullah Al Faruque

Session Title	Simulating Everything: From Timing to Instructions
Session Code / Room	12.4 / Konferenz 2
Date / Time	Thursday, 17 March 2016 / 16:00 – 17:30
Chair	**Elena Ioana Vatajelu**, *Politecnico di Torino, IT*
Co-Chair	**Valeria Bertacco**, *University of Michigan, US*

12.4.1
16:00 – 16:30
Accelerating Source-Level Timing Simulation 1574
Simon Schulz and Oliver Bringmann

12.4.2
16:30 – 17:00
Sparsity-Oriented Sparse Solver Design for Circuit Simulation 1580
Xiaoming Chen, Lixue Xia, Yu Wang and Huazhong Yang

12.4.3
17:00 – 17:15
Integration of Mixed-signal Components into Virtual Platforms for Holistic Simulation of Smart Systems 1586
Enrico Fraccaroli, Michele Lora, Sara Vinco, Davide Quaglia and Franco Fummi

12.4.4
17:15 – 17:30
Decision Tree Generation for Decoding Irregular Instructions 1592
Katsumi Okuda and Haruhiko Takeyama

Session Title	Accelerator Design and Heterogeneous Architectures
Session Code / Room	12.5 / Konferenz 3
Date / Time	Thursday, 17 March 2016 / 16:00 – 17:30
Chair	**Cristina Silvano**, *Politecnico di Milano, IT*
Co-Chair	**Todd Austin**, *University of Michigan, US*

12.5.1
16:00 – 16:30
A Reconfigurable Heterogeneous Multicore with a Homogeneous ISA 1598
Jeckson Dellagostin Souza, Luigi Carro, Mateus Beck Rutzig and Antonio Carlos Schneider Beck

12.5.2
16:30 – 17:00
The Neuro Vector Engine: Flexibility to Improve Convolutional Net Efficiency for Wearable Vision 1604
Maurice Peemen, Runbin Shi, Sohan Lal, Ben Juurlink, Bart Mesman and Henk Corporaal

12.5.3
17:00 – 17:15
Improving Scalability of CMPs with Dense ACCs Coverage 1610
Nasibeh Teimouri, Hamed Tabkhi and Gunar Schirner

12.5.4
17:15 – 17:30
Hardware Accelerator for Analytics of Sparse Data 1616
Eriko Nurvitadhi, Asit Mishra, Yu Wang, Ganesh Venkatesh and Debbie Marr

Session Title	Reconfigurable Computing Platforms and Architectures
Session Code / Room	12.6 / Konferenz 4
Date / Time	Thursday, 17 March 2016 / 16:00 – 17:30
Chair	**Dirk Stroobandt**, *Ghent University, BE*
Co-Chair	**Jürgen Becker**, *Karlsruhe Institute of Technology, DE*

12.6.1
16:00 – 16:30
Securing the Cloud with Reconfigurable Computing: An FPGA Accelerator for Homomorphic Encryption 1622
Alessandro Cilardo and Domenico Argenziano

12.6.2
16:30 – 17:00
Throughput Oriented FPGA Overlays Using DSP Blocks 1628
Abhishek Kumar Jain, Douglas L. Maskell and Suhaib A. Fahmy

12.6.3
17:00 – 17:30
Run-time Phase Prediction for a Reconfigurable VLIW Processor 1634
Qi Guo, Anderson Sartor, Anthony Brandon, Antonio C. S. Beck, Xuehai Zhou and Stephan Wong

Session Title	Formal System Level Verification
Session Code / Room	12.7 / Konferenz 5
Date / Time	Thursday, 17 March 2016 / 16:00 – 17:30
Chair	**Mathias Soeken**, *EPFL, CH*
Co-Chair	**Gianpiero Cabodi**, *Politecnio di Torino, IT*

12.7.1
16:00 – 16:30
ADVOCAT: Automated Deadlock Verification for On-chip Cache Coherence and Interconnects 1640
Freek Verbeek, Pooria M. Yaghini, Ashkan Eghbal and Nader Bagherzadeh

12.7.2
16:30 – 17:00
Guarantees for Runnable Entities with Heterogeneous Real-Time Requirements 1646
Leonie Ahrendts, Zain A. H. Hammadeh and Rolf Ernst

12.7.3
17:00 – 17:30
Validating Scheduling Transformation for Behavioral Synthesis 1652
Zhenkun Yang, Kecheng Hao, Kai Cong, Li Lei, Sandip Ray and Fei Xie

Additional Papers:

HPAZ: A High-Throughput Pipeline Architecture of ZUC in Hardware 269
Zongbin Liu, Qinglong Zhang, Cunqing Ma, Changline, Jiwu Jing

Recursive Hierarchical DFT Methodology with Multi-Level Clock Control and Scan Pattern Retargeting 1128
Dan Trock, Rick Fisette