

2016 Design, Automation & Test in Europe Conference & Exhibition (DATE 2016)

**Dresden, Germany
14-18 March 2016**

Pages 1-829



**IEEE Catalog Number: CFP16162-POD
ISBN: 978-1-4673-9228-0**

**Copyright ©2016, European Design Automation Association (EDAA)
All Rights Reserved**

******This publication is a representation of what appears in the IEEE
Digital Libraries. Some format issues inherent in the e-media version may
also appear in this print version.***

IEEE Catalog Number:	CFP16162-POD
ISBN (Print-On-Demand):	978-1-4673-9228-0
ISBN (Online):	978-3-9815370-7-9
ISSN:	1530-1591

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

Technical Program

Technical Program

Tuesday, 15 March 2016											
1.1	2.1	2.2	2.3	2.4	2.5	2.6	2.7	3.1	3.2	3.3	3.4
3.5	3.6	3.7	IP1	4.1	4.2	4.3	4.4	4.5	4.6	4.7	
Wednesday, 16 March 2016											
5.1	5.2	5.3	5.4	5.5	5.6	5.7	IP2	6.1	6.2	6.3	6.4
6.5	6.6	6.7	7.0	7.1	7.2	7.3	7.4	7.5	7.6	7.7	IP3
8.1	8.2	8.3	8.4	8.5	8.6	8.7					
Thursday, 17 March 2016											
9.1	9.2	9.3	9.4	9.5	9.6	9.7	9.8	IP4	10.1	10.2	10.3
10.4	10.5	10.6	10.7	11.0	11.1	11.2	11.3	11.4	11.5	11.6	11.7
IP5	12.1	12.2	12.3	12.4	12.5	12.6	12.7				

Session	Opening Session: Plenary, Awards Ceremony & Keynote Addresses
Session Code / Room	1.1 / Großer Saal
Date / Time	Tuesday, 15 March 2016 / 08:30 – 10:30
Chair	Luca Fanucci, <i>University of Pisa, IT</i>
Co-Chair	Jürgen Teich, <i>Friedrich-Alexander-Universität Erlangen-Nürnberg, DE</i>

1.1.1 09:15 – 09:45	[Keynote] From the Happy Few to the Happy Many Towards an Intuitive Internet of Things <i>Luc Van den hove</i>
1.1.2 09:45 – 10:15	[Keynote] Design Will Make Everything Different <i>Antun Domic</i>

Session Title	Executive Track Panel: Enabling a Connected World via Internet of Things
Session Code / Room	2.1 / Saal 2
Date / Time	Tuesday, 15 March 2016 / 11:30 – 13:00
Organiser	Yervant Zorian, Synopsys, US

2.1.1 Presenter
11:30 – 13:00 *Mohamed Djadoudi*

2.1.2 Presenter
11:30 – 13:00 *Christoph Heer*

2.1.3 Presenter
11:30 – 13:00 *Jamil Kawa*

2.1.4 Presenter
11:30 – 13:00 *Rudy Lauwereins*

2.1.5 Presenter
11:30 – 13:00 *Cheng-Wen Wu*

Session Title	Embedded Tutorial: The Dark Silicon Problem: Technology to the Rescue?
Session Code / Room	2. 2 / Konferenz 6
Date / Time	Tuesday, 15 March 2016 / 11:30 – 13:00
Organisers	Siddharth Garg, New York University, US Michael Niemier, University of Notre Dame, South Bend, US
Chair	Muhammad Shafique, Karlsruhe Institute of Technology, DE
Co-Chair	Umit Ogras, Arizona State University, US

2.2.1 Towards Performance and Reliability-Efficient Computing in the Dark Silicon Era 1
11:30 – 12:00 *Jörg Henkel, Santiago Pagani, Heba Khdr, Florian Kriebel, Semeen Rehman and Muhammad Shafique*

2.2.2 Towards Near-Threshold Server Processors 7
12:00 – 12:30 *Ali Pahlevan, Javier Picorel, Arash Pourhabibi Zarandi, Davide Rossi, Marina Zapater, Andrea Bartolini, Pablo G. Del Valle, David Atienza, Luca Benini and Babak Falsafi*

2.2.3 Can Beyond-CMOS Devices Illuminate Dark Silicon? 13
12:30 – 13:00 *Robert Perricone, X. Sharon Hu, Joseph Nahas and Michael Niemier*

Session Title	Automotive Systems and Smart Energy Systems
Session Code / Room	2.3 / Konferenz 1
Date / Time	Tuesday, 15 March 2016 / 11:30 – 13:00
Chair	David Boyle, Imperial College London, GB
Co-Chair	Felix Reimann, Audi Electronics Venture, DE
2.3.1 11:30 – 12:00	OTEM: Optimized Thermal and Energy Management for Hybrid Electrical Energy Storage in Electric Vehicles 19 <i>Korosh Vatanparvar and Mohammad Abdullah Al Faruque</i>
2.3.2 12:00 – 12:30	Supertask: Maximizing Runnable-level Parallelism in AUTOSAR Applications 25 <i>Sebastian Kehr, Miloš Panić, Eduardo Quiñones, Bert Bötdeker, Jorge Becerril Sandoval, Jaume Abella, Francisco J. Cazorla and Günter Schäfer</i>
2.3.3 12:30 – 12:45	Formal Analysis Based Evaluation of Software Defined Networking for Time-Sensitive Ethernet 31 <i>Daniel Thiele and Rolf Ernst</i>
2.3.4 12:45 – 13:00	Accelerated Artificial Neural Networks on FPGA for Fault Detection in Automotive Systems 37 <i>Shanker Shreejith, Bezborah Anshuman and Suhaib A. Fahmy</i>

Session Title	Physical Design for Cutting-edge Lithography
Session Code / Room	2.4 / Konferenz 2
Date / Time	Tuesday, 15 March 2016 / 11:30 – 13:00
Chair	Jens Lienig, Technische Universität Dresden, DE
Co-Chair	Patrick Groeneveld, Synopsys Inc., US
2.4.1 11:30 – 12:00	Optimization for Multiple Patterning Lithography with Cutting Process and Beyond 43 <i>Jian Kuang and Evangeline F. Y. Young</i>
2.4.2 12:00 – 12:30	A Fast Manufacturability Aware Optical Proximity Correction (OPC) Algorithm with Adaptive Wafer Image Estimation 49 <i>Ahmed Awad, Atsushi Takahashi and Chikaaki Kodama</i>
2.4.3 12:30 – 12:45	Redundant Via Insertion in Directed Self-Assembly Lithography 55 <i>Woohyun Chung, Seongbo Shim and Youngsoo Shin</i>
2.4.4 12:45 – 13:00	Improved Performance of 3DIC Implementations Through Inherent Awareness of Mix-and-Match Die Stacking 61 <i>Kwangsoo Han, Andrew B. Kahng and Jiajia Li</i>

Session Title	Energy Efficient Systems and Architectures
Session Code / Room	2.5 / Konferenz 3
Date / Time	Tuesday, 15 March 2016 / 11:30 – 13:00
Chair	Mladen Berekovic, TU Braunschweig, DE
Co-Chair	Rolf Ernst, TU Braunschweig, DE

- 2.5.1** A Discrete Thermal Controller for Chip-Multiprocessors 67
11:30 – 12:00 *Yingnan Cui, Wei Zhang and Bingsheng He*
- 2.5.2** Swallow: Building an Energy-Transparent Many-Core Embedded Real-Time System 73
12:00 – 12:30 *Simon J. Hollis and Steve Kerrison*
- 2.5.3** A Novel Cache-Utilization Based Dynamic Voltage Frequency Scaling (DVFS) Mechanism for Reliability Enhancements 79
12:30 – 12:45 *Yen-Hao Chen, Yi-Lun Tang, Yi-Yu Liu, Allen C.-H. Wu and TingTing Hwang*
- 2.5.4** Efficient Kernel Management on GPUs 85
12:45 – 13:00 *Xiuhong Li and Yun Liang*

Session Title	Fault-Tolerant Embedded Systems
Session Code / Room	2.6 / Konferenz 4
Date / Time	Tuesday, 15 March 2016 / 11:30 – 13:00
Chair	Lothar Thiele, ETH Zurich, CH
Co-Chair	Jian-Jia Chen, TU Dortmund, DE

- 2.6.1** Probabilistic WCET Estimation in Presence of Hardware for Mitigating the Impact of Permanent Faults 91
11:30 – 12:00 *Damien Hardy, Isabelle Puaut and Yiannakis Sazeides*
- 2.6.2** A Four-Mode Model for Efficient Fault-Tolerant Mixed-Criticality Systems 97
12:00 – 12:30 *Zaid Al-bayati, Jonah Caplan, Brett H. Meyer and Haibo Zeng*
- 2.6.3** Providing Formal Latency Guarantees for ARQ-based Protocols in Networks-on-Chip 103
12:30 – 13:00 *Eberle A. Rambo, Selma Saidi and Rolf Ernst*

Session Title	Variability Challenges in Nanoscale Designs
Session Code / Room	2.7 / Konferenz 5
Date / Time	Tuesday, 15 March 2016 / 11:30 – 13:00
Chair	Vikas Chandra, ARM Research, US
Co-Chair	Said Hamdioui, TU Delft, NL

- 2.7.1** Achieving 100% Cell-Aware Coverage by Design 109
11:30 – 12:30 *Zeye (Dexter) Liu, Ben Niewenhuis, Soumya Mittal and R. D. (Shawn) Blanton*
- 2.7.2** Modeling Fabrication Non-Uniformity in Chip-Scale Silicon Photonic
Interconnects 115
12:00 – 12:30 *Mahdi Nikdast, Gabriela Nicolescu, Jelena Trajkovic and Odile Liboiron-Ladouceur*
- 2.7.3** Efficient Spatial Variation Modeling via Robust Dictionary Learning 121
12:30 – 13:00 *Changhai Liao, Jun Tao, Xuan Zeng, Yangfeng Su, Dian Zhou and Xin Li*

Session Title	Executive Track Panel: New Opportunities in Automotive Electronics
Session Code / Room	3.1 / Saal 2
Date / Time	Tuesday, 15 March 2016 / 14:30 – 16:00
Organiser	Yervant Zorian, Synopsys, US

- 3.1.1** Presenter
14:30 – 16:00 *Josef Stockinger*
- 3.1.2** Presenter
14:30 – 16:00 *Rainer Kress*
- 3.1.3** Presenter
14:30 – 16:00 *Dan Kochpatcharin*
- 3.1.4** Presenter
14:30 – 16:00 *Frank Schirrmeister*

Session Title	Hot Topic: 3D ICs: Leap Forward to 1,000X Performance
Session Code / Room	3.2 / Konferenz 6
Date / Time	Tuesday, 15 March 2016 / 14:30 – 16:00
Organiser	Vikas Chandra, ARM, US
Chair	Vikas Chandra, ARM, US
Co-Chair	Norbert Wehn, University of Kaiserslautern, DE

- 3.2.1** The N3XT 1,000X N/A
14:30 – 15:00 *Subhasish Mitra, Stanford University, US*
- 3.2.2** 3D Sequential Integration for Monolithic 3DIC Design N/A
15:00 – 15:30 *Olivier Billoint, CEA-Leti, FR*
- 3.2.3** 3D Technology Driven by 3D Application Requirements: A 3D-Landscape for
15:30 – 14:30 3D System Design N/A
Dragomir Milojevic, IMEC, BE

Session Title	On-Chip Security Testing
Session Code / Room	3.3 / Konferenz 1
Date / Time	Tuesday, 15 March 2016 / 14:30 – 16:00
Chair	Giorgio Di Natale, LIRMM, FR
Co-Chair	Marc Witteman, Riscure, NL

- 3.3.1** TOTAL: TRNG On-the-fly Testing for Attack Detection using Lightweight
14:30 – 15:00 Hardware 127
Bohan Yang, Vladimir Rožic, Nele Mentens, Wim Dehaene and Ingrid Verbauwhede
- 3.3.2** On-chip Fingerprinting of IC Topology for Integrity Verification 133
15:00 – 15:30 *Maxime Lecomte, Jacques J.A. Fournier and Philippe Maurine*
- 3.3.3** Activation of Logic Encrypted Chips: Pre-Test or Post-Test? 139
15:30 – 16:00 *Muhammad Yasin, Samah Mohamed Saeed, Jeyavijayan (JV) Rajendran and Ozgur Sinanoglu*

Session Title	Application-specific Low-power Techniques
Session Code / Room	3.4 / Konferenz 2
Date / Time	Tuesday, 15 March 2016 / 14:30 – 16:00
Chair	Sheldon X.-D. Tan, <i>University of California at Riverside, US</i>
Co-Chair	Masaaki Kondo, <i>University of Tokyo, JP</i>

- 3.4.1**
14:30 – 15:00 Multiplier-less Artificial Neurons Exploiting Error Resiliency for Energy-Efficient Neural Computing 145
Syed Shakib Sarwar, Swagath Venkataramani, Anand Raghunathan and Kaushik Roy
- 3.4.2**
15:00 – 15:30 Significance Driven Hybrid 8T-6T SRAM for Energy-Efficient Synaptic Storage in Artificial Neural Networks 151
Gopalakrishnan Srinivasan, Parami Wijesinghe, Syed Shakib Sarwar, Akhilesh Jaiswal and Kaushik Roy
- 3.4.3**
15:30 – 16:00 Network Delay-Aware Energy Management for Mobile Systems 157
Minho Ju, Hyeonggyu Kim and Soontae Kim

Session Title	Emerging Devices and Methodologies for Energy Efficient Systems
Session Code / Room	3.5 / Konferenz 3
Date / Time	Tuesday, 15 March 2016 / 14:30 – 16:00
Chair	Mehdi Tahoori, <i>Karlsruhe Institute of Technology, DE</i>
Co-Chair	Aida Todri-Sanial, <i>LIRMM, FR</i>

- 3.5.1**
14:30 – 15:00 Enabling Simultaneously Bi-Directional TSV Signaling for Energy and Area Efficient 3D-ICs 163
Sunghyun Park, Alice Wang, Uming Ko, Li-Shiuan Peh and Anantha P. Chandrakasan
- 3.5.2**
15:00 – 15:30 Reconfigurable Nanowire Transistors with Multiple Independent Gates for Efficient and Programmable Combinational Circuits 169
Jens Trommer, André Heinzig, Tim Baldauf, Thomas Mikolajick, Walter M. Weber, Michael Raitza and Marcus Völp
- 3.5.3**
15:30 – 16:00 Exploiting Inherent Characteristics of Reversible Circuits for Faster Combinational Equivalence Checking 175
Luca Amarú, Pierre-Emmanuel Gaillardon, Robert Wille and Giovanni De Micheli

Session Title	Timing Analysis and Measurement
Session Code / Room	3.6 / Konferenz 4
Date / Time	Tuesday, 15 March 2016 / 14:30 – 16:00
Chair	Marko Bertogna, Università di Modena e Reggio Emilia, IT
Co-Chair	Damien Hardy, University of Rennes I/IRISA, FR

- 3.6.1**
14:30 – 15:00 Conservative Modeling of Shared Resource Contention for Dependent Tasks in Partitioned Multi-Core Systems 181
Junchul Choi, Donghyun Kang and Soonhoi Ha
- 3.6.2**
15:00 – 15:30 Formal Worst-Case Timing Analysis of Ethernet TSN's Burst-Limiting Shaper 187
Daniel Thiele and Rolf Ernst
- 3.6.3**
15:30 – 15:45 Real-Time Analysis of Engine Control Applications with Speed Estimation 193
Alessandro Biondi and Giorgio Buttazzo
- 3.6.4**
15:45 – 16:00 Trace-based Analysis Methodology of Program Flash Contention in Embedded Multicore Systems 199
Lin Li and Albrecht Mayer

Session Title	Dealing with Runtime Failures
Session Code / Room	3.7 / Konferenz 5
Date / Time	Tuesday, 15 March 2016 / 14:30 – 16:00
Chair	Lorena Anghel, TIMA Laboratory, FR
Co-Chair	Michel Renovell, LIRMM, FR

- 3.7.1**
14:30 – 15:00 A Cross-Layer Analysis of Soft Error, Aging and Process Variation in Near Threshold Computing 205
Anteneh Gebregiorgis, Saman Kiamehr, Fabian Oboril, Rajendra Bishnoi and Mehdi B. Tahoori
- 3.7.2**
15:00 – 15:30 Fast-yet-accurate Variation-Aware Current and Voltage Modelling of Radiation-Induced Transient Fault 211
Hsuan-Ming (Ryan) Huang, Yuwen (Dave) Lin and Charles H.-P. Wen
- 3.7.3**
15:30 – 15:45 A Detailed Methodology to Compute Soft Error Rates in Advanced Technologies 217
Marc Riera, Ramon Canal, Jaume Abella and Antonio Gonzalez
- 3.7.4**
15:45 – 16:00 Analysis of NBTI Effects on High Frequency Digital Circuits 223
Ahmet Unutulmaz, Domenik Helms, Reef Eilers, Malte Metzdorf, Ben Kaczer and Wolfgang Nebel

Session Title	Interactive Presentations
Session Code / Room	IP1
Date / Time	Tuesday, 15 March 2016 / 16:00 – 16:30
IP1-1	A Scalable Lane Detection Algorithm on COTSS with OpenCL 229 <i>Kai Huang, Biao Hu, Jan Botsch, Nikhil Madduri and Alois Knoll</i>
IP1-2	Simulation of Falling Rain for Robustness Testing of Video-Based Surround Sensing Systems 233 <i>Dennis Hospach, Stefan Mueller, Wolfgang Rosenstiel and Oliver Bringmann</i>
IP1-3	Proposal for Fast Directional Energy Interchange Used in MCMC-Based Autonomous Decentralized Mechanism toward Resilient Microgrid 237 <i>Yusuke Sakumoto and Itetsu Taniguchi</i>
IP1-4	Grid-based Self-Aligned Quadruple Patterning Aware Two Dimensional Routing Pattern 241 <i>Takeshi Ihara, Toshiyuki Hongo, Atsushi Takahashi and Chikaaki Kodama</i>
IP1-5	Practical ILP-based Routing of Standard Cells 245 <i>Hsueh-Ju Lu, En-Jang Jang, Ang Lu, Yu Ting Zhang, Yu-He Chang, Chi-Hung Lin and Rung-Bin Lin</i>
IP1-6	A Procedure for Improving the Distribution of Congestion in Global Routing 249 <i>Daohang Shi, Azadeh Davoodi and Jeffrey Linderoth</i>
IP1-7	Machine Learned Machines: Adaptive Co-optimization of Caches, Cores, and On-chip Network 253 <i>Rahul Jain, Preeti Ranjan Panda and Sreenivas Subramoney</i>
IP1-8	Improving Performance by Monitoring While Maintaining Worst-Case Guarantees 257 <i>Syed Md Jakaria Abdullah, Kai Lampka and Wang Yi</i>
IP1-9	Fault Tolerant Non-Volatile Spintronic Flip-Flop 261 <i>Rajendra Bishnoi, Fabian Oboril and Mehdi B. Tahoori</i>
IP1-10	Towards Automatic Diagnosis of Minority Carriers Propagation Problems in HV/HT Automotive Smart Power ICs 265 <i>Yasser Moursy, Hao Zou, Ramy Iskander, Pierre Tisserand, Dieu-My Ton, Giuseppe Pasetti, Ehrenfried Seebacher, Alexander Steinmair, Thomas Gneiting and Heidrun Alius</i>
IP1-12	Towards a Highly Reliable SRAM-based PUFs 273 <i>Elena Ioana Vatajelu, Giorgio Di Natale and Paola Prinetto</i>
IP1-13	Current based PUF Exploiting Random Variations in SRAM Cells 277 <i>Fengchao Zhang, Shuo Yang, Jim Plusquellic and Swarup Bhunia</i>
IP1-14	Behavioral Modeling of Timing Slack Variation in Digital Circuits Due to Power Supply Noise 281 <i>Taesik Na and Saibal Mukhopadhyay</i>

- IP1-15** Lossless Compression Algorithm Based on Dictionary Coding for Multiple E-Beam Direct Write System 285
Pei-Chun Lin, Yu-Hsuan Pai, Yu-Hsiang Chiu, Shao-Yuan Fang and Charlie Chung-Ping Chen
- IP1-16** PhoNoCMap: an Application Mapping Tool for Photonic Networks-on-Chip 289
Edoardo Fusella and Alessandro Cilardo
- IP1-17** Design of an Efficient Ready Queue for Earliest-Deadline-First (EDF) Scheduler 293
Risat Mahmud Pathan
- IP1-18** RT Level Timing Modeling for Aging Prediction 297
Nils Koppaetzky, Malte Metzendorf, Reef Eilers, Domenik Helms and Wolfgang Nebel

Session Title	Executive Track Panel: Trends & Challenges to Ensure Security
Session Code / Room	4.1 / Saal 2
Date / Time	Tuesday, 15 March 2016 / 17:00 – 18:30
Organiser	Yervant Zorian, Synopsys, US

4.1.1 Presenter
17:00 – 18:30 *Mike Borza*

4.1.2 Presenter
17:00 – 18:30 *Rob Aitken*

4.1.3 Presenter
17:00 – 18:30 *Serge Leef*

Session Title	Hot Topic: Nanoelectronic Design Tools Addressing Coupled Problems for 3D-IC Integration
Session Code / Room	4.2 / Konferenz 6
Date / Time	Tuesday, 15 March 2016 / 17:00 – 18:30
Organisers	Jan ter Maten, University of Wuppertal, DE Caren Tischendorf, Humboldt University of Berlin, DE
Chair	Wim Schoenmaker, Magwel NV, Leuven, BE
Co-Chair	Caren Tischendorf, Humboldt University of Berlin, DE

4.2.1 Fast Time-Domain Simulation for Reliable Fault Detection 301
17:00 – 17:22 *Bratislav Tasić, Jos J. Dohmen, Rick Janssen, E. Jan W. ter Maten, Roland Pulch and Theo G. J. Beelen*

4.2.2 Holistic Coupled Field and Circuit Simulation 307
17:22 – 17:44 *Wim Schoenmaker, Peter Meuris, Christian Strohm and Caren Tischendorf*

4.2.3 Model Order Reduction for Nanoelectronics Coupled Problems with Many Inputs 313
17:44 – 18:06 *N. Banagaaya, L. Feng, W. Schoenmaker, P. Meuris, A. Wieers, R. Gillonz and P. Benner*

4.2.4 Shape Optimization of a Power MOS Device Under Uncertainties 319
18:06 – 17:00 *Piotr Putek, Peter Meuris, Roland Pulch, E. Jan W. ter Maten, Michael Günther, Wim Schoenmaker, Frederik Deleu and Aarnout Wieers*

Session Title	Firmware Security
Session Code / Room	4.3 / Konferenz 1
Date / Time	Tuesday, 15 March 2016 / 17:00 – 18:30
Chair	Nele Mentens, Katholieke Universiteit Leuven, BE
Co-Chair	Aurelien Francillon, EURECOM, FR

4.3.1 Practical Evaluation of Code Injection in Encrypted Firmware Updates 325
17:00 – 17:30 *Oscar M. Guillen, Dawin Schmidt and Georg Sigl*

4.3.2 Integration of ROP/JOP Monitoring IPs in an ARM-based SoC 331
17:30 – 18:00 *Yongje Lee, Jinyong Lee, Ingoo Heo, Dongil Hwang and Yunheung Paek*

4.3.3 Verifying Information Flow Properties of Firmware using Symbolic Execution 337
18:00 – 18:30 *Pramod Subramanyan, Sharad Malik, Hareesh Khattri, Abhranil Maiti and Jason Fung*

Session Title	System-level Energy Management
Session Code / Room	4.4 / Konferenz 2
Date / Time	Tuesday, 15 March 2016 / 17:00 – 18:30
Chair	William Fornaciari, Politecnico di Milano – DEIB, IT
Co-Chair	Soontae Kim, KAIST, KR

4.4.1 Low-Overhead Adaptive Contrast Enhancement and Power Reduction for OLEDs 343
17:00 – 17:30 *Daniele Jahier Pagliari, Massimo Poncino and Enrico Macii*

4.4.2 Dynamic Energy Burst Scaling for Transiently Powered Systems 349
17:30 – 18:00 *Andres Gomez, Lukas Sigrist, Michele Magno, Luca Benini and Lothar Thiele*

4.4.3 Low-power Multichannel Spectro-temporal Feature Extraction Circuit for Audio Pattern Wake-up 355
18:00 – 17:00 *Dinko Oletic, Vedran Bilas, Michele Magno, Norbert Felber and Luca Benini*

Session Title	Ultra-low Energy Memory Devices
Session Code / Room	4.5 / Konferenz 3
Date / Time	Tuesday, 15 March 2016 / 17:00 – 18:30
Chair	Fabien Clermidy, CEA-Leti, FR
Co-Chair	Walter Weber, Namlab, DE
4.5.1 17:00 – 17:30	3T-TFET bitcell based TFET-CMOS Hybrid SRAM design for Ultra-Low Power Applications 361 <i>Navneet Gupta, Adam Makosiej, Andrei Vladimirescu, Amara Amara and Costin Anghel</i>
4.5.2 17:30 – 18:00	Design of Latches and Flip-Flops using Emerging Tunneling Devices 367 <i>Xunzhao Yin, Behnam Sedighi, Michael Niemier and X. Sharon Hu</i>
4.5.3 18:00 – 17:00	MASC: Ultra-Low Energy Multiple-Access Single-Charge TCAM for Approximate Computing 373 <i>Mohsen Imani, Shruti Patil and Tajana S. Rosing</i>
Session Title	Managing Multi-Core and Flash Memory
Session Code / Room	4.6 / Konferenz 4
Date / Time	Tuesday, 15 March 2016 / 17:00 – 18:30
Chair	Akash Kumar, Technische Universität Dresden, DE
Co-Chair	Olivier Sentiyes, INRIA, FR
4.6.1 17:00 – 17:30	Distributed Fair Scheduling for Many-Cores 379 <i>Anuj Pathania, Vanchinathan Venkataramani, Muhammad Shafique, Tulika Mitra and Jörg Henkel</i>
4.6.2 17:30 – 18:00	Keep It Slow and in Time: Online DVFS with Hard Real-Time Workloads 385 <i>Kai Lampka and Björn Forsberg</i>
4.6.3 18:00 – 18:30	Exploiting Process Variation for Retention Induced Refresh Minimization on Flash Memory 391 <i>Yeji Di, Liang Shi, Kaijie Wu and Chun Jason Xue</i>

Session Title	Modeling of Devices and Mixed-Signal Circuits
Session Code / Room	4.7 / Konferenz 5
Date / Time	Tuesday, 15 March 2016 / 17:00 – 18:30
Chair	Nuno Horta, Instituto de Telecomunicacoes, PT
Co-Chair	Jaijeet Roychowdhury, UC Berkeley, US
4.7.1 17:00 – 17:30	Accurate Synthesis of Integrated RF Passive Components Using Surrogate Models 397 <i>F. Passos, R. González-Echevarría, E. Roca, R. Castro-López and F. V. Fernández</i>
4.7.2 17:30 – 18:00	Implementation and Quality Testing for Compact Models Implemented in Verilog-A 403 <i>Anindya Mukherjee, Andreas Pawlak, Michael Schroter, Didier Celi and Zoltan Huszka</i>
4.7.3 18:00 – 18:30	Multi-Harmonic Nonlinear Modeling of Low-power PWM DC-DC Converters Operating in CCM and DCM 409 <i>Ya Wang, Di Gao, Dani A. Tannir and Peng Li</i>

Session Title	SPECIAL DAY Hot Topic: Building Confidence in Advanced Driver Assistance Systems
Session Code / Room	5.1 / Saal 2
Date / Time	Wednesday, 16 March 2016 / 08:30 – 10:00
Organiser	Samarjit Chakraborty, Technische Universität München (TUM), DE Wolfgang Ecker, Infineon Technologies, DE
Chair	Sebastian Steinhorst, TUM CREATE, SG
Co-Chair	Kai Lampka, Uppsala University, SE
5.1.1 08:30 – 09:00	Availability and Interpretability of Optimal Control for Criticality Estimation in Vehicle Active Safety 415 <i>Stephan Herrmann and Wolfgang Utschick</i>
5.1.2 09:00 – 10:00	Certification Issues in Automotive Driver Assistance Systems N/A <i>Udo Steininger</i>
5.1.3 09:30 – 10:00	Deep Learning in Advanced Driver Assistance Systems N/A <i>Qing Rao</i>

Session Title	Hot Topic: In-memory Computing: Status and Trends
Session Code / Room	5.2 / Konferenz 6
Date / Time	Wednesday, 16 March 2016 / 08:30 – 10:00
Organiser	Pierre-Emmanuel Gaillardon, University of Utah, Salt Lake City, US
Chair	Ian O'Connor, Institute des Nanotechnologies de Lyon, Ecully, FR
Co-Chair	Michael Niemier, University of Notre Dame, South Bend, US

5.2.1 08:30 – 08:52	Software and System Co-Optimization in the ERA of Heterogeneous Computing N/A <i>Ruchir Puri</i>
5.2.2 08:52 – 09:14	Fading Memory Effects in a Memristor for Cellular Nanoscale Network Applications 421 <i>A. Ascoli, R. Tetzlaff, L. O. Chua, J. P. Strachan and R. S. Williams</i>
5.2.3 09:14 – 09:36	Digital Memcomputing Machines 426 <i>Massimiliano Di Ventra and Fabio L. Traversa</i>
5.2.4 09:36 – 10:00	The <i>Programmable Logic-in-Memory</i> (PLiM) Computer 427 <i>Pierre-Emmanuel Gaillardon, Luca Amarú, Anne Siemon, Eike Linn, Rainer Waser, Anupam Chattopadhyay and Giovanni De Micheli</i>

Session Title	Physical Attacks and Countermeasures
Session Code / Room	5.3 / Konferenz 1
Date / Time	Wednesday, 16 March 2016 / 08:30 – 10:00
Chair	Assia Tria, CEA-Leti, FR
Co-Chair	Francesco Regazzoni, ALaRI, CH

5.3.1 08:30 – 09:00	Oracle-Guided Incremental SAT Solving to Reverse Engineer Camouflaged Logic Circuits 433 <i>Duo Liu, Cunxi Yu, Xiangyu Zhang and Daniel Holcomb</i>
5.3.2 09:00 – 09:30	A Fully-Digital EM Pulse Detector 439 <i>David El-Baze, Jean-Baptiste Rigaud and Philippe Maurine</i>
5.3.3 09:30 – 10:00	On the Development of a New Countermeasure Based on a Laser Attack RTL Fault Model 445 <i>Charalampos Ananiadis, Athanasios Papadimitriou, David Hély, Vincent Beroulle, Paolo Maistri and Régis Leveugle</i>

Session Title	Architectural-level Low-power Design
Session Code / Room	5.4 / Konferenz 2
Date / Time	Wednesday, 16 March 2016 / 08:30 – 10:00
Chair	Alberto Macii, Politecnico di Torino, IT
Co-Chair	Pascal Vivet, CEA LETI, FR

- 5.4.1** Multi-Story Power Distribution Networks for GPUs 451
08:30 – 09:00 *Qixiang Zhang, Liangzhen Lai, Mark Gottscho and Puneet Gupta*
- 5.4.2** Energy-Efficient Cache Memories using a Dual-V t 4T SRAM Cell with Read-Assist Techniques 457
09:00 – 09:30 *Alireza Shafaei and Massoud Pedram*
- 5.4.3** Learning-Based Dynamic Reliability Management For Dark Silicon Processor Considering EM Effects 463
09:30 – 10:00 *Taeyoung Kim, Xin Huang, Hai-Bao Chen, Valeriy Sukharev and Sheldon X.-D. Tan*

Session Title	Alternative Computing Models
Session Code / Room	5.5 / Konferenz 3
Date / Time	Wednesday, 16 March 2016 / 08:30 – 10:00
Chair	Yiyu Shi, University of Notre Dame, US
Co-Chair	Sébastien Le Beux, Ecole Centrale de Lyon, FR

- 5.5.1** MNSIM: Simulation Platform for Memristor-based Neuromorphic Computing System 469
08:30 – 09:00 *Lixue Xia, Boxun Li, Tianqi Tang, Peng Gu, Xiling Yin, Wenqin Huangfu, Pai-Yu Chen, Shimeng Yu, Yu Cao, Yu Wang, Yuan Xie and Huazhong Yang*
- 5.5.2** Conditional Deep Learning for Energy-Efficient and Enhanced Pattern Recognition 475
09:00 – 09:30 *Priyadarshini Panda, Abhronil Sengupta and Kaushik Roy*
- 5.5.3** Probabilistic Error Models for Machine Learning Kernels Implemented on Stochastic Nanoscale Fabrics 481
09:30 – 10:00 *Sai Zhang and Naresh R. Shanbhag*

Session Title	Efficient System Modeling with SystemC
Session Code / Room	5.6 / Konferenz 4
Date / Time	Wednesday, 16 March 2016 / 08:30 – 10:00
Chair	Gunar Schirner, Northeastern University, US
Co-Chair	Christian Haubelt, University of Rostock, DE

- 5.6.1** A New Parallel SystemC Kernel Leveraging Manycore Architectures 487
08:30 – 09:00 *Nicolas Ventroux and Tanguy Sassolas*
- 5.6.2** SystemC-Link: Parallel SystemC Simulation using Time-Decoupled Segments 493
09:00 – 09:30 *Jan Henrik Weinstock, Rainer Leupers, Gerd Ascheid, Dietmar Petras and Andreas Hoffmann*
- 5.6.3** Orthogonal Signal Modeling and Operational Computation of AMS Circuits for Fast and Accurate System Simulation 499
09:30 – 10:00 *Leandro Gil and Martin Radetzki*

Session Title	RF, Power Converters, and ADC: Innovative Design and Test Solutions
Session Code / Room	5.7 / Konferenz 5
Date / Time	Wednesday, 16 March 2016 / 08:30 – 10:00
Chair	Marie-Minerve Louerat, Université Pierre & Marie Curie, (UPMC - Paris 6), FR
Co-Chair	Christoph Grimm, University of Kaiserslautern, DE

- 5.7.1** Built-in Test of Millimeter-Wave Circuits Based on Non-Intrusive Sensors 505
08:30 – 09:00 *Athanasios Dimakos, Haralampos-G. Stratigopoulos, Alexandre Siligaris, Salvador Mir and Emeric De Foucauld*
- 5.7.2** Adaptive Delay Monitoring for Wide Voltage-Range Operation 511
09:00 – 09:30 *Jongho Kim, Gunhee Lee, Kiyoung Choi, Yonghwan Kim, Wook Kim, Kyungtae Do and Jungyun Choi*
- 5.7.3** Analytical Design Optimization of Sub-ranging ADC Based on Stochastic Comparator 517
09:30 – 10:00 *Md. Maruf Hossain, Tetsuya Iizuka, Toru Nakura and Kunihiro Asada*

Session Title	Interactive Presentations
Session Code / Room	IP2
Date / Time	Wednesday, 16 March 2016 / 10:00 – 10:30
IP2-1	Analyzing the Impact of Injected Sensor Data on an Advanced Driver Assistance System using the OP ₂ TIMUS Prototyping Platform 523 <i>Alexander Stühning, Günter Ehmen and Sibylle Fröschle</i>
IP2-2	Hardware Trojans in Incompletely Specified On-chip Bus Systems 527 <i>Nicole Fern, Ismail San, Çetin Kaya Koç and Kwang-Ting (Tim) Cheng</i>
IP2-3	Workload-aware Power Optimization Strategy for Asymmetric Multiprocessors 531 <i>E. Del Sozzo, G. C. Durelli, E. M. G. Trainiti, A. Miele, M. D. Santambrogio and C. Bolchini</i>
IP2-4	The Slowdown or Race-to-idle Question: Workload-Aware Energy Optimization of SMT Multicore Platforms under Process Variation 535 <i>Anup Das, Geoff V. Merrett and Bashir M. Al-Hashimi</i>
IP2-5	Towards General Purpose Computations on Low-End Mobile GPUs 539 <i>Matina Maria Trompouki and Leonidas Kosmidis</i>
IP2-6	Estimating Delay Differences of Arbiter PUFs Using Silicon Data 543 <i>S. V. Sandeep Avvaru, Chen Zhou, Saroj Satapathy, Yingjie Lao, Chris H. Kim and Keshab K. Parhi</i>
IP2-7	On the Use of Forward Body Biasing to Decrease the Repeatability of Laser-Induced Faults 547 <i>Marc Lacruche, Noemie Beringuier-Boher, Jean-Max Dutertre, Jean-Baptiste Rigaud and Edith Kussener</i>
IP2-8	Sequential Analysis Driven Reset Optimization to Improve Power, Area and Routability 551 <i>Srihari Yechangunja, Raj Shekhar, Mohit Kumar, Nikhil Tripathi, Abhishek Mittal, Abhishek Ranjan, Jianfeng Liu, Minyoung Mo, Kyungtae Do, Jung Yun Choi and SungHo Park</i>
IP2-9	Efficient Global Optimization of MEMS Based on Surrogate Model Assisted Evolutionary Algorithm 555 <i>Bo Liua and Anna Nikolaeva</i>
IP2-10	Efficient Monitoring of Loose-Ordering Properties for SystemC/TLM 559 <i>Yuliia Romenska and Florence Maraninchi</i>
IP2-11	Testable Design of Repeaterless Low Swing On-Chip Interconnect 563 <i>K. Naveen and Dinesh K. Sharma</i>
IP2-12	Il-digital Hybrid-control Buck Converter for Integrated Voltage Regulator Applications 567 <i>Ta-Tung Yen, Bin Yu, Visvesh S. Sathe</i>

Session Title	SPECIAL DAY Hot Topic: Formal Methods for Automotive Software
Session Code / Room	6.1 / Saal 2
Date / Time	Wednesday, 16 March 2016 / 11:00 – 12:30
Chair	Marc Geilen, Eindhoven University of Technology, NL
Co-Chair	Wolfgang Ecker, Infineon Technologies, DE
6.1.1 11:00 – 11:30	Requirements Engineering for Software-Intensive Automotive Embedded Systems N/A <i>Manfred Broy</i>
6.1.2 11:30 – 12:00	Formal Specification and Verification of Automotive Software in Practice N/A <i>Ravindra Metta</i>
6.1.3 12:00 – 12:30	Timing Analysis of Automotive Architectures and Software <i>Nicolas Navet</i>
Session Title	Panel: Looking Backwards and Forwards
Session Code / Room	6.2 / Konferenz 6
Date / Time	Wednesday, 16 March 2016 / 11:00 – 12:30
Organiser	Marco Casale-Rossi, Synopsys, US
Chair	Marco Casale-Rossi, Synopsys, US
Co-Chair	Giovanni De Micheli, EPFL, CH
6.2.1 11:00 – 12:30	Panel: Looking Backwards and Forwards 571 <i>Marco Casale-Rossi, Giovanni De Micheli, Antun Domic, Enrico Macii, Domenico Rossi and Joe Sawicki</i>
6.2.2 11:00 – 12:30	Panelist <i>Enrico Macii</i>
6.2.3 11:00 – 12:30	Panelist <i>Antun Domic</i>
6.2.4 11:00 – 12:30	Panelist <i>Domenico Rossi</i>
6.2.5 11:00 – 12:30	Panelist <i>Joseph Sawicki</i>
6.2.6 11:00 – 12:30	Moderator <i>Giovanni De Micheli</i>

Session Title	Anti-aging and Error protection using Checkpointing and DVFS	
Session Code / Room	6.3 / Konferenz 1	
Date / Time	Wednesday, 16 March 2016 / 11:00 – 12:30	
Chair	Antonio Rosario Miele, Polimi, IT	
Co-Chair	Jose L. Ayala, Complutense University of Madrid, ES	
6.3.1 11:00 – 11:30	Aging-Aware Voltage Scaling 576 <i>Victor M. van Santen, Hussam Amrouch, Narendra Parihar, Souvik Mahapatra and Jörg Henkel</i>	
6.3.2 11:30 – 12:00	RECORD: Reducing Register Traffic for Checkpointing in Embedded Processors 582	
	<i>Tuo Li, Jude Angelo Ambrose and Sri Parameswaran</i>	
6.3.3 12:00 – 12:15	Error Resilience and Energy Efficiency: An LDPC Decoder Design Study 588 <i>Philipp Schläfer, Chu-Hsiang Huang, Clayton Schoeny, Christian Weis, Yao Li, Norbert Wehn and Lara Dolecek</i>	
6.3.4 12:15 – 12:30	Runtime Interval Optimization and Dependable Performance for Application-Level Checkpointing 594 <i>Apostolos Kokolis, Alexandros Mavrogiannis, Dimitrios Rodopoulos, Christos Strydis and Dimitrios Soudris</i>	
Session Title	Power Modeling and Power Aware Synthesis	
Session Code / Room	6.4 / Konferenz 2	
Date / Time	Wednesday, 16 March 2016 / 11:00 – 12:30	
Chair	Alberto Garcia Ortiz, University of Bremen, DE	
Co-Chair	Qi Zhu, UCR, US	
6.4.1 11:00 – 11:30	A Systematic Approach to Automated Construction of Power Emulation Models 600	
	<i>Benjamin A. Bjørnseth, Asbjørn Djupdal and Lasse Natvig</i>	
6.4.2 11:30 – 12:00	Automatic Generation of Power State Machines through Dynamic Mining of Temporal Assertions 606 <i>Alessandro Danese, Graziano Pravadelli and Ivan Zandonà</i>	
6.4.3 12:00 – 12:30	Approximation through Logic Isolation for the Design of Quality Configurable Circuits 612 <i>Shubham Jain, Swagath Venkataramani and Anand Raghunathan</i>	

Session Title	Biochips
Session Code / Room	6.5 / Konferenz 3
Date / Time	Wednesday, 16 March 2016 / 11:00 – 12:30
Chair	Robert Wille, JKU, AT
Co-Chair	Ian O’Connor, Ecole Centrale de Lyon, FR
6.5.1 11:00 – 11:30	Architecture Synthesis for Cost-Constrained Fault-Tolerant Flow-based Biochips 618 <i>Morten Chabert Eskesen, Paul Pop and Seetal Potluri</i>
6.5.2 11:30 – 12:00	Sieve-valve-aware Synthesis of Flow-based Microfluidic Biochips Considering Specific Biological Execution Limitations 624 <i>Mengchu Li, Tsun-Ming Tseng, Bing Li, Tsung-Yi Ho and Ulf Schlichtmann</i>
6.5.3 12:00 – 12:30	Integrated and Real-Time Quantitative Analysis Using Cyberphysical Digital-Microfluidic Biochips 630 <i>Mohamed Ibrahim, Krishnendu Chakrabarty and Kristin Scott</i>

Session Title	Modelling and Control of Cyber-Physical Systems
Session Code / Room	6.6 / Konferenz 4
Date / Time	Wednesday, 16 March 2016 / 11:00 – 12:30
Chair	Donatella Sciuto, Politecnico di Milano, IT
Co-Chair	Paul Pop, Technical University of Denmark, DK
6.6.1 11:00 – 11:30	Self-Triggered Controllers and Hard Real-Time Guarantees 636 <i>Amir Aminifar, Paulo Tabuada, Petru Eles and Zebo Peng</i>
6.6.2 11:30 – 12:00	A Spatio-Temporal Fractal Model for a CPS Approach to Brain-Machine-Body Interfaces 642 <i>Yuankun Xue, Saul Rodriguez and Paul Bogdan</i>
6.6.3 12:00 – 12:15	Modular Code Generation for Emulating the Electrical Conduction System of the Human Heart 648 <i>Nathan Allen, Sidharta Andalām, Partha Roop, Avinash Malik, Mark Trew and Nitish Patel</i>
6.6.4 12:15 – 12:30	Resource Utilization and Quality-of-Control Trade-off for a Composable Platform 654 <i>Juan Valencia, E.P. (Eelco) van Horssen, Dip Goswami, W. P. M. H. (Maurice) Heemels and Kees Goossens</i>

Session Title	Fault Tolerant Systems and Methods
Session Code / Room	6.7 / Konferenz 5
Date / Time	Wednesday, 16 March 2016 / 11:00 – 12:30
Chair	Viacheslav Izosimov, Semcon Sweden AB, SE
Co-Chair	Zebo Peng, Linköping University, SE

- 6.7.1** Inexact Designs for Approximate Low Power Addition by Cell Replacement 660
11:00 – 11:30 *Haider A. F. Almurib, T. Nandha Kumar and Fabrizio Lombardi*
- 6.7.2** A General Approach for Highly Defect Tolerant Parallel Prefix Adder Design 666
11:30 – 12:00 *Soumya Banerjee and Wenjing Rao*
- 6.7.3** Inverters' Self-Checking Monitors for Reliable Photovoltaic Systems 672
12:00 – 12:30 *M. Omaña, A. Fiore and C. Metra*

Session	Lunch Time Keynote Session
Session Code / Room	7.0
Date / Time	Wednesday, 16 March 2016 / 14:00 – 14:30
Chair	Luca Fanucci, University of Pisa, IT
Co-Chair	Wolfgang Ecker, Infineon Technologies, DE

- 7.0.1** [Keynote] The Car of the Future will reinvent personal mobility xxx
14:00 – 14:30 *Patrick Leteinturier*

Session Title	SPECIAL DAY Panel: Which EDA Solutions can the Automotive Domain Reuse? Very Few or All?
Session Code / Room	7.1 / Saal 2
Date / Time	Wednesday, 16 March 2016 / 14:30 – 16:00
Chair	Adam Morawiec, European Chips & Systems Design Initiative (ESCI), FR

- 7.1.2** Panelist
14:30 – 16:00 *Rainer Kress*
- 7.1.3** Panelist
14:30 – 16:00 *Gabriele Ernst*
- 7.1.4** Panelist
14:30 – 16:00 *Jean-Marie Saint-Paul*

- 7.1.5 Panelist
14:30 – 16:00 *Silvano Motto*
- 7.1.6 Panelist
14:30 – 16:00 *Christoph Störmer*
- 7.1.1 Moderator
14:30 – 16:00 *Oliver Bringmann*

Session Title	EU Projects Special Session: Energy Efficiency drives Design
Session Code / Room	7.2 / Konferenz 6
Date / Time	Wednesday, 16 March 2016 / 14:30 – 16:00
Organiser	Roberto Giorgi, University of Siena, IT
Chair	Martin Schoeberl, Technical University of Denmark, DK
Co-Chair	Roberto Giorgi, University of Siena, IT

- 7.2.1 EUROSERVER: Share-Anything Scale-Out Micro-Server Design 678
14:30 – 14:45 *Manolis Marazakis, John Goodacre, Didier Fuin, Paul Carpenter, John Thomson, Emil Matus, Antimo Bruno, Per Stenstrom, Jerome Martin, Yves Durand and Isabelle Dor*
- 7.2.2 Energy Minimization at All Layers of the Data Center: The ParaDIME Project 684
14:45 – 15:00 *Oscar Palomar, Santhosh Rethinagiri, Gulay Yalcin, Ruben Titos-Gil, Pablo Prieto, Emma Torrella, Osman Unsal, Adrian Cristal, Pascal Felber, Anita Sobe, Yaroslav Hayduk, Mascha Kurpicz, Christof Fetzer, Thomas Knauth, Malte Schneegaß, Jens Struckmeier and Dragomir Milojevic*
- 7.2.3 Rack-scale Disaggregated Cloud Data Centers: The dReDBox Project Vision 690
15:00 – 15:15 *K. Katrinis, D. Syrivelis, D. Pnevmatikatos, G. Zervas, D. Theodoropoulos, I. Koutsopoulos, K. Hasharoni, D. Raho, C. Pinto, F. Espina, S. Lopez-Buedo, Q. Chen, M. Nemirovsky, D. Roca, H. Klos and T. Berends*
- 7.2.4 ECOSCALE: Reconfigurable Computing and Runtime System for Future Exascale Systems 696
15:15 – 15:30 *Iakovos Mavroidis, Ioannis Papaefstathiou, Luciano Lavagno, Dimitrios S. Nikolopoulos, Dirk Koch, John Goodacre, Ioannis Sourdis, Vassilis Papaefstathiou, Marcello Coppola and Manuel Palomino*
- 7.2.5 Enabling HPC for QoS-sensitive Applications: The MANGO Approach 702
15:30 – 15:45 *José Flich, Giovanni Agosta, Philipp Ampletzerz, David Atienza Alonso, Carlo Brandolese, Alessandro Cilardo, William Fornaciari, Ynse Hoornenborg, Mario Kovac, Bruno Maitre, Giuseppe Massari, Hrvoje Mlinarić, Ermis Papastefanakis, Fabrice Roudet, Rafael Tornero and Davide Zoni*

7.2.6 AutoTuning and Adaptivity approach for Energy Efficient eXascale HPC
15:45 – 16:00 Systems: The ANTAREX Approach 708
Cristina Silvano, Giovanni Agosta, Andrea Bartolini, Andrea R. Beccari, Luca Benini, João Bispo, Radim Cmar, João M. P. Cardoso, Carlo Cavazzoni, Jan Martinovic, Gianluca Palermo, Martin Palkovic, Pedro Pinto, Erven Rohou, Nico Sanna and Katerina Slaninová

Session Title	Low Power Devices and Methods for Healthcare and Assisted Living
Session Code / Room	7.3 / Konferenz 1
Date / Time	Wednesday, 16 March 2016 / 14:30 – 16:00
Chair	José M. Moya , <i>Technical University of Madrid, ES</i>
Co-Chair	Giovanni Ansaloni , <i>University of Lugano, CH</i>

7.3.1 A Digital Processor Architecture for Combined EEG/EMG Falling Risk
14:30 – 15:00 Prediction 714
V. F. Annese, M. Crepaldi, D. Demarchi and D. De Venuto

7.3.2 Distributed-neuron-network based Machine Learning on Smart-gateway Network
15:00 – 15:30 Towards Real-time Indoor Data Analytics 720
Hantao Huang, Yuehua Cai and Hao Yu

7.3.3 Touch-Based System for Beat-to-Beat Impedance Cardiogram Acquisition and
15:30 – 15:45 Hemodynamic Parameters Estimation 726
Dionisije Sopic, Srinivasan Murali, Francisco Rincón and David Atienza

7.3.4 Quantifying the Benefits of Compressed Sensing on a WBSN-based Real-Time
15:45 – 16:00 Biosignal Monitor 732
Daniele Bortolotti, Bojan Milosevic, Andrea Bartolini, Elisabetta Farella and Luca Benini

Session Title	System-Level Synthesis
Session Code / Room	7.4 / Konferenz 2
Date / Time	Wednesday, 16 March 2016 / 14:30 – 16:00
Chair	Cathal McCabe , <i>Xilinx, Inc. Ireland, IE</i>
Co-Chair	Yuichi Nakamura , <i>NEC Japan, JP</i>

7.4.1 System Level Synthesis for Virtual Memory Enabled Hardware Threads 738
14:30 – 15:00 *Nicolas Estivals, Gaël Deest, Ali Hassan El Moussawi and Steven Derrien*

7.4.2 Composable, Parameterizable Templates for High-Level Synthesis 744
15:00 – 15:30 *Janarbek Matai, Dajung Lee, Alric Althoff and Ryan Kastner*

7.4.3 Leveraging Power Spectral Density for Scalable System-Level Accuracy
15:30 – 16:00 Evaluation 750
Benjamin Barrois, Karthick Parashar and Olivier Sentieys

Session Title	Emerging Memory Architectures
Session Code / Room	7.5 / Konferenz 3
Date / Time	Wednesday, 16 March 2016 / 14:30 – 16:00
Chair	Amara Amara, ISEP, FR
Co-Chair	Fabian Oboril, Karlsruhe Institute of Technology, DE

7.5.1 Leader: Accelerating ReRAM-based Main Memory by Leveraging Access
14:30 – 15:00 Latency Discrepancy in Crossbar Arrays 756
Hang Zhang, Nong Xiao, Fang Liu and Zhiguang Chen

7.5.2 Sliding Basket: An Adaptive ECC Scheme for Runtime Write Failure
15:00 – 15:30 Suppression of STT-RAM Cache* 762
Xue Wang, Mengjie Mao, Enes Eken, Wujie Wen, Hai Li and Yiran Chen

7.5.3 Exploiting More Parallelism from Write Operations on PCM 768
15:30 – 16:00 *Zheng Li, Fang Wang, Yu Hua, Wei Tong, Jingning Liu, Yu Chen and Dan Feng*

Session Title	Statistical and Symbolic Techniques for the Analysis and Testing of Embedded Software
Session Code / Room	7.6 / Konferenz 4
Date / Time	Wednesday, 16 March 2016 / 14:30 – 16:00
Chair	Jian-Jia Chen, Technische Universität Dortmund, DE
Co-Chair	Petru Eles, Linköping University, SE

7.6.1 Dynamic Partitioning Strategy to Enhance Symbolic Execution 774
14:30 – 15:00 *Brendan A. Marcellino and Michael S. Hsiao*

7.6.2 Quantitative Timing Analysis of UML Activity Diagrams Using Statistical Model
15:00 – 15:30 Checking 780
Fan Gu, Xinqian Zhang, Mingsong Chen, Daniel Große and Rolf Drechsler

7.6.3 Integrating Symbolic and Statistical Methods for Testing Intelligent Systems
15:30 – 16:00 Applications to Machine Learning and Computer Vision 786
Arvind Ramanathan, Laura L. Pullum, Faraz Hussain, Dwaipayan Chakrabarty and Sumit Kumar Jha

Session Title	Ageing Mitigation to Improve System Robustness
Session Code / Room	7.7 / Konferenz 5
Date / Time	Wednesday, 16 March 2016 / 14:30 – 16:00
Chair	Maria Michael, <i>University of Cyprus, CY</i>
Co-Chair	Carles Hernandez, <i>Barcelona Supercomputer Center, ES</i>

- 7.7.1** Path Selection and Sensor Insertion Flow for Age Monitoring in FPGAs 792
14:30 – 15:00 *Mohammad Ebrahimi, Zana Ghaderi, Eli Bozorgzadeh and Zain Navabi*
- 7.7.2** Design and Evaluation of Reliability-oriented Task Re-Mapping in MOSoCs using Time-Series Analysis of Intermittent Faults 798
15:00 – 15:30 *Siva Satyendra Sahoo, Akash Kumar and Bharadwaj Veeravalli*
- 7.7.3** Lifetime-aware Load Distribution Policies in Multi-core Systems: An In-depth Analysis 804
15:30 – 16:00 *Cristiana Bolchini, Luca Cassano and Antonio Miele*

Session Title	Interactive Presentations
Session Code / Room	IP3
Date / Time	Wednesday, 16 March 2016 / 16:00 – 16:30

- IP3-1** A Flexible Inexact TMR Technique for SRAM-based FPGAs 810
Shyamsundar Venkataraman, Rui Santos and Akash Kumar
- IP3-2** Accurate Verification of RC Power Grids 814
Mohammad Fawaz and Farid N. Najm
- IP3-3** Security-Aware Development of Cyber-Physical Systems Illustrated with Automotive Case Study 818
Viacheslav Izosimov, Alexandros Asvestopoulos, Oscar Blomkvist and Martin Törngren
- IP3-4** Online Heuristic for the Multi-objective Generalized Traveling Salesman Problem 822
Joost van Pinxten, Marc Geilen, Twan Basten, Umar Waqas and Lou Somers
- IP3-5** Towards Low Overhead Control Flow Checking Using Regular Structured Control 826
Zhiqi Zhu and Joseph Callenes-Sloan
- IP3-6** Emulation-Based Hierarchical Fault-Injection Framework for Coarse-to-Fine Vulnerability Analysis of Hardware-Accelerated Approximate Algorithms 830
Ioannis Chadjiminias, Ioannis Savva, Christos Kyrkou, Maria K. Michael and Theocharis Theocharides

IP3-7	Technology Transfer in Computing Systems: The TETRACOM Approach 834 <i>Rainer Leupers</i>
IP3-8	Energy vs. Reliability Trade-offs Exploration in Biomedical Ultra-Low Power Devices 838 <i>Loris Duch, P. Garcia del Valle, Shrikanth Ganapathy, Andreas Burg and David Atienza</i>
IP3-9	A Machine Learning Approach for Medication Adherence Monitoring Using Body-Worn Sensors 842 <i>Nilloofar Hezarjaribi, Ramin Fallahzadeh and Hassan Ghasemzadeh</i>
IP3-10	Requirements-Centric Closed-Loop Validation of Implantable Cardiac Devices 846 <i>Weiwei Ai, Nitish Patel and Partha Roop</i>
IP3-11	Low Normalized Energy Derivation Asynchronous Circuit Synthesis Flow through Fork-Join Slack Matching for Cryptographic Applications 850 <i>Nan Liu, Kwen-Siong Chong, Weng-Geng Ho, Bah-Hwee Gwee and Joseph S. Chang</i>
IP3-12	A Lifetime-Aware Runtime Mapping Approach for Many-core Systems in the Dark Silicon Era 854 <i>Mohammad-Hashem Haghbayan, Antonio Miele, Amir M. Rahmani, Pasi Liljeberg and Hannu Tenhunen</i>

Session Title	SPECIAL DAY Hot Topic: Connectivity in the Automotive Domain: From Micro to Macro
Session Code / Room	8.1 / Saal 2
Date / Time	Wednesday, 16 March 2016 / 17:00 – 18:30
Chair	Henk Corporaal, Eindhoven University of Technology, NL
Co-Chair	Samarjit Chakraborty, Technische Universität München (TUM), DE
8.1.1 17:00 – 17:30	Automotive V2X on Phones: Enabling Next-generation Mobile ITS Apps 858 <i>Jason H. Gao and Li-Shiuan Peh</i>
8.1.2 17:30 – 18:00	EDA for automotive cabling N/A <i>Thomas Heurung, Mentor, DE</i>
8.1.3 18:00 – 18:30	Deterministic Ethernet in Automotive Applications N/A <i>Astrit Ademaj, TTTech Computertechnik AG, AT</i>

Session Title	EU Projects Special Session: Towards Better EU-projects – Success Stories
Session Code / Room	8.2 / Konferenz 6
Date / Time	Wednesday, 16 March 2016 / 17:00 – 18:30
Organiser	Roberto Giorgi, University of Siena, IT
Chair	Cristina Silvano, Politecnico of Milan, IT
Co-Chair	Roberto Giorgi, University of Siena, IT

8.2.1 17:00 – 17:15	Collective Knowledge: Towards R&D Sustainability 864 <i>Grigori Fursin, Anton Lokhmotov and Ed Plowman</i>
8.2.2 17:15 – 17:30	Lessons Learned from the EU Project T-CREST 870 <i>Martin Schoeberl</i>
8.2.3 17:30 – 17:45	MULTI-POS: Marie Curie Network in Multi-technology Positioning 876 <i>Jari Nurmi and Elena-Simona Lohan</i>
8.2.4 17:45 – 18:00	Program Transformations in the POLCA Project 882 <i>Jan Kuper, Lutz Schubert, Kilian Kempf, Colin Glass, Daniel Rubio Bonilla and Manuel Carro</i>
8.2.5 18:00 – 18:15	Computation and Communication Challenges to Deploy Robots in Assisted Living Environments 888 <i>Georgios Keramidas, Christos Antonopoulos, Nikolaos S. Voros, Fynn Schwiegelshohn, Philipp Wehner, Jens Rettkowski, Diana Göhringer, Michael Hübner, Stasinios Konstantopoulos, Theodore Giannakopoulos, Vangelis Karkaletsis and Vaggelis Mariatos</i>
8.2.6 18:15 – 18:30	ATHENIS_3D: Automotive Tested High-voltage and Embedded Non-volatile Integrated SoC Platform with 3D Technology 894 <i>E. Wachmann, S. Saponara, C. Zambelli, P. Tisserand, J. Charbonnier, T. Erlbacher, S. Gruenler, C. Hartler, J. Siegert, P. Chassard, D. M. Ton, L. Ferrari and L. Fanucci</i>

Session Title	Hot Topic: Managing Heterogeneous Computing Resources at Runtime
Session Code / Room	8.3 / Konferenz 1
Date / Time	Wednesday, 16 March 2016 / 17:00 – 18:30
Organisers	Christian Plessl, <i>University of Paderborn, DE</i> David Andrews, <i>University of Arkansas, US</i>
Chair	Daniel Ziener, <i>Hamburg University of Technology, DE</i>
Co-Chair	José L. Ayala, <i>Complutense University of Madrid, ES</i>

- 8.3.1** Run Time Interpretation for Creating Custom Accelerators 900
17:00 – 17:30 *Sen Ma, Zeyad Aklah and David Andrews*
- 8.3.2** A Self-Adaptive Approach to Efficiently Manage Energy and Performance in
Tomorrow's Heterogeneous Computing Systems 906
17:30 – 18:00 *E. M. G. Trainiti, G. C. Durelli, A. Miele, C. Bolchini and M. D. Santambrogio*
- 8.3.3** Performance-Centric Scheduling with Task Migration for a Heterogeneous
Compute Node in the Data Center 912
18:00 – 18:30 *Achim Lösch, Tobias Beisel, Tobias Kenter, Christian Plessl and Marco Platzner*

Session Title	Advanced Methods in High-Level Design
Session Code / Room	8.4 / Konferenz 2
Date / Time	Wednesday, 16 March 2016 / 17:00 – 18:30
Chair	Fabian Oboril, <i>KIT Germany, DE</i>
Co-Chair	Luciano Lavagno, <i>Politecnico di Torino, IT</i>

- 8.4.1** Adaptive Threshold Non-Pareto Elimination: Re-thinking Machine Learning for
System Level Design Space Exploration on FPGAs 918
17:00 – 17:30 *Pingfan Meng, Alric Althoff, Quentin Gautier and Ryan Kastner*
- 8.4.2** Monitoring of MTL Specifications With IBM's Spiking-Neuron Model 924
17:30 – 18:00 *Konstantin Selyunin, Thang Nguyen, Ezio Bartocci, Dejan Nickovic and Radu Grosu*
- 8.4.3** Formal Probabilistic Analysis of Distributed Resource Management Schemes in
On-Chip Systems 930
18:00 – 18:30 *Shafaq Iqtedar, Osman Hasan, Muhammad Shafique and Jörg Henkel*

Session Title	Non-volatile Memory Design Methodologies
Session Code / Room	8.5 / Konferenz 3
Date / Time	Wednesday, 16 March 2016 / 17:00 – 18:30
Chair	Michael Huebner, RUB, DE
Co-Chair	Michael Niemier, University of Notre Dame, US
8.5.1 17:00 – 17:30	An Operating System Level Data Migration Scheme in Hybrid DRAM-NVM Memory Architecture 936 <i>Reza Salkhordeh and Hossein Asadi</i>
8.5.2 17:30 – 18:00	Unified DRAM and NVM Hybrid Buffer Cache Architecture for Reducing Journaling Overhead 942 <i>Zhiyong Zhang, Lei Ju and Zhiping Jia</i>
8.5.3 18:00 – 18:30	Fast Logic Synthesis for RRAM-based In-Memory Computing using Majority-Inverter Graphs 948 <i>Saeideh Shirinzadeh, Mathias Soeken, Pierre-Emmanuel Gaillardon and Rolf Drechsler</i>

Session Title	Dataflow Modeling and Natural Language Processing
Session Code / Room	8.6 / Konferenz 4
Date / Time	Wednesday, 16 March 2016 / 17:00 – 18:30
Chair	Dominique Borrione, Laboratoire TIMA, FR
Co-Chair	Marc Geilen, Eindhoven University of Technology, NL
8.6.1 17:00 – 17:30	Exploiting Resource-constrained Parallelism in Hard Real-Time Streaming Applications 954 <i>Jelena Spasic, Di Liu and Todor Stefanov</i>
8.6.2 17:30 – 18:00	Transaction Parameterized Dataflow: A Model for Context-Dependent Streaming Applications 960 <i>Xuan Khanh Do, Stephane Louise and Albert Cohen</i>
8.6.3 18:00 – 18:30	GLAsT: Learning Formal Grammars to Translate Natural Language Specifications into Hardware Assertions 966 <i>Christopher B. Harris and Ian G. Harris</i>

Session Title	Test Methods Handling Unknowns, 2.5D Integration and Realistic Memory Defects
Session Code / Room	8.7 / Konferenz 5
Date / Time	Wednesday, 16 March 2016 / 17:00 – 18:30
Chair	Friedrich Hapke, Mentor Graphics Hamburg, DE

8.7.1
17:00 – 17:30 Accurate CEGAR-based ATPG in Presence of Unknown Values for Large Industrial Designs 972
Karsten Scheibler, Dominik Erb and Bernd Becker

8.7.2
17:30 – 18:00 Pre-Bond Testing of the Silicon Interposer in 2.5D ICs 978
Ran Wang, Zipeng Li, Sukeshwar Kannan and Krishnendu Chakrabarty

8.7.3
18:00 – 18:30 Improving SRAM Test Quality by Leveraging Self-timed Circuits 984
Josef Kinseher, Leonardo B. Zordan, Ilia Polian and Andreas Leininger

Session Title	SPECIAL DAY Embedded Tutorial: Embedded Systems Security
Session Code / Room	9.1 / Saal 2
Date / Time	Thursday, 17 March 2016 / 08:30 – 10:00
Chair	Matthias Schunter, Intel, DE
Co-Chair	Wieland Fischer, Infineon Technologies, DE

9.1.1
08:30 – 10:00 Software Security: Vulnerabilities and Countermeasures for Two Attacker Models 990
Frank Piessens and Ingrid Verbauwhede

Session Title	Managing the Traffic Jam in NoC
Session Code / Room	9.2 / Konferenz 6
Date / Time	Thursday, 17 March 2016 / 08:30 – 10:00
Chair	Nader Bagherzadeh, University of California Irvine, US
Co-Chair	Massoud Daneshtalab, KTH, SE

9.2.1
08:30 – 09:00 OLITS: An Ohm's Law-like Traffic Splitting Model Based on Congestion Prediction 1000
Gaoming Du, Yanghao Ou, Xiangyang Li, Ping Song, Zhonghai Lu and Minglun Gao

9.2.2
09:00 – 09:30 MCAPI-compliant Hardware Buffer Manager Mechanism to Support Communication in Multi-Core Architectures 1006
Thiago Raupp da Rosa, Thomas Mesquida, Romain Lemaire and Fabien Clermidy

9.2.3 Slack-Based Resource Arbitration for Real-Time Networks-On-Chip 1012
09:30 – 10:00 *Adam Kostrzewa, Selma Saidi and Rolf Ernst*

Session Title	Industrial Experiences
Session Code / Room	9.3 / Konferenz 1
Date / Time	Thursday, 17 March 2016 / 08:30 – 10:00
Chair	Norbert Wehn, University of Kaiserslautern, DE
Co-Chair	Stephan Diestelhorst, ARM, US

- 9.3.1** Challenges of Using On-Chip Performance Monitors for Process and Environmental Variation Compensation 1018
08:30 – 08:45 *Mahroo Zandrahimi, Zaid Al-Ars, Philippe Debaudand Armand Castillejo*
- 9.3.2** Study of Workload Impact on BTI HCI Induced Aging of Digital Circuits 1020
08:45 – 09:00 *Ajith Sivadasan, Florian Cacho, Sidi Ahmed Benhassain, Vincent Huard and Lorena Anghel*
- 9.3.3** Fast Prototyping Platform for Navigation Systems with Sensors Fusion 1022
09:00 – 09:15 *Charly Bechara, Karim Ben Chehida, Mickael Guibert, Renaud Schmit, Maria Lepecq, Laurent Soulier, Thomas Dombek and Yann Leclerc*
- 9.3.4** Precision Timed Industrial Automation Systems 1024
09:15 – 09:30 *Matthew M. Y. Kuo, Sidharta Andalarn and Partha S. Roop*
- 9.3.5** AUTOSAR-based Communication Coprocessor for Automotive ECUs 1026
09:30 – 09:45 *Ahmed Hamed, Mona Safar, M. Watheq El-Kharashiand Ashraf Salem*
- 9.3.6** Mantissa-Masking for Energy-Efficient Floating-Point LTE Uplink MIMO Baseband Processing 1028
09:45 – 10:00 *D. Guenther, T. Henriksson, R. Leupers, G. Ascheid*

Session Title	Optimization for Logic and Physical Design
Session Code / Room	9.4 / Konferenz 2
Date / Time	Thursday, 17 March 2016 / 08:30 – 10:00
Chair	Valeria Bertacco, Univ. of Michigan, US
Co-Chair	Sven Peyer, IBM, DE

- 9.4.1** Optimizing Majority-Inverter Graphs With Functional Hashing 1030
08:30 – 09:00 *Mathias Soeken, Luca Gaetano Amarù, Pierre-Emmanuel Gaillardon and Giovanni De Micheli*
- 9.4.2** Resource-Aware Functional ECO Patch Generation 1036
09:00 – 09:30 *An-Che Cheng, Iris Hui-Ru Jiang and Jing-Yang Jou*

9.4.3 Simultaneous Slack Matching, Gate Sizing and Repeater Insertion for
09:30 – 10:00 Asynchronous Circuits 1042
Gang Wu and Chris Chu

Session Title	Formal Bit Precise Reasoning
Session Code / Room	9.5 / Konferenz 3
Date / Time	Thursday, 17 March 2016 / 08:30 – 10:00
Chair	Markus Wedler , <i>Synopsys GmbH, DE</i>
Co-Chair	Julien Schmaltz , <i>Eindhoven University of Technology, NL</i>

9.5.1 Formal Verification of Integer Multipliers by Combining Gröbner Basis with
08:30 – 09:00 Logic Reduction 1048
Amr Sayed-Ahmed, Daniel Große, Ulrich Kühne, Mathias Soeken and Rolf Drechsler

9.5.2 Root-Cause Analysis for Memory-Locked Errors 1054
09:00 – 09:30 *John Adler, Djordje Maksimovic and Andreas Veneris*

9.5.3 Formal Verification of Clock Domain Crossing using Gate-level Models of
09:30 – 10:00 Metastable Flip-Flops 1060
Ghaith Tarawneh, Andrey Mokhov and Alex Yakovlev

Session Title	Real-Time Scheduling
Session Code / Room	9.6 / Konferenz 4
Date / Time	Thursday, 17 March 2016 / 08:30 – 10:00
Chair	Frank Slomka , <i>Universität Ulm, DE</i>
Co-Chair	Kai Lampka , <i>Uppsala University, SE</i>

9.6.1 Response-Time Analysis of DAG Tasks under Fixed Priority Scheduling with
08:30 – 09:00 Limited Preemptions 1066
Maria A. Serrano, Alessandra Melani, Marko Bertogna and Eduardo Quinones

9.6.2 Speed Optimization for Tasks with Two Resources 1072
09:00 – 09:30 *Alessandra Melani, Renato Mancuso, Daniel Cullina, Marco Caccamo and Lothar Thiele*

9.6.3 Self-Suspension Real-Time Tasks under Fixed-Relative-Deadline Fixed-Priority
09:30 – 10:00 Scheduling 1078
Wen-Hung Huang and Jian-Jia Chen

Session Title	Temperature Awareness in Computing Systems
Session Code / Room	9.7 / Konferenz 5
Date / Time	Thursday, 17 March 2016 / 08:30 – 10:00
Chair	Muhammad Shafique, Karlsruhe Institute of Technology, DE
Co-Chair	Marina Zapater, Complutense University of Madrid, ES
9.7.1 08:30 – 09:00	Thermal-aware Dynamic Page Allocation Policy by Future Access Patterns for Hybrid Memory Cube (HMC) 1084 <i>Wei-Hen Lo, Kai-zen Liang and TingTing Hwang</i>
9.7.2 09:00 – 09:30	Minimizing Peak Temperature for Pipelined Hard Real-time Systems 1090 <i>Long Cheng, Kai Huang, Gang Chen, Biao Hu and Alois Knoll</i>
9.7.3 09:30 – 10:00	Thermal Aware Scheduling and Mapping of Multiphase Applications onto Chip Multiprocessor 1096 <i>Aryabartta Sahu</i>

Session Title	Embedded Tutorial: Analog-/Mixed-Signal Verification Methods for AMS Coverage Analysis
Session Code / Room	9.8 / Exhibition Theater
Date / Time	Thursday, 17 March 2016 / 08:30 – 10:00
Organisers	Gregor Nitsche, OFFIS, DE
Chair	Lars Hedrich, Johann Wolfgang Goethe-Universität, DE
Co-Chair	Christoph Grimm, University of Kaiserslautern, DE
9.8.0 08:30 – 10:00	Embedded Tutorial: Analog-/Mixed-Signal Verification Methods for AMS Coverage Analysis 1102 <i>Erich Barke, Andreas Fürtig, Georg Gläser, Christoph Grimm, Lars Hedrich, Stefan Heinen, Eckhard Hennig, Hyun-Sek Lukas Lee, Wolfgang Nebel, Gregor Nitsche, Markus Olbrich, Carna Radojicic and Fabian Speicher</i>
9.8.1 08:30 – 09:00	Towards More Dependable Verification Using Symbolic Simulation N/A <i>Carna Radojicic, Christoph Grimm, Fabian Speicher and Stefan Heinen</i>
9.8.2 09:00 – 09:30	Identification of Critical Scenarios in AMS Verification: Methodology for Finding the Safe Operating Area of AMS Systems N/A <i>Georg Gläser, Hyun-Sek Lukas Lee, Markus Olbrich, Erich Barke and Eckhard Hennig</i>
9.8.3 09:30 – 10:00	AMS Leaf-Component Characterization with Contracts and Satisfaction Checking vs. Electronic Circuit Schematics N/A <i>Gregor Nitsche, Andreas Fürtig, Lars Hedrich and Wolfgang Nebel</i>

Session Title	Interactive Presentations
Session Code / Room	IP4
Date / Time	Thursday, 17 March 2016 / 10:00 – 10:30
IP4-1	A q -gram Birthmarking Approach to Predicting Reusable Hardware 1112 <i>Kevin Zeng and Peter Athanas</i>
IP4-2	Captopril: Reducing the Pressure of Bit Flips on Hot Locations in Non-Volatile Main Memories 1116 <i>Majid Jalili and Hamid Sarbazi-Azad</i>
IP4-3	Handling Complex Dependencies in System Design 1120 <i>Mischa Moestl and Rolf Ernst</i>
IP4-4	A Synthesis-Agnostic Behavioral Fault Model for High Gate-Level Fault Coverage 1124 <i>Anton Karputkin and Jaan Raik</i>
IP4-6	Combining Graph-based Guidance with Error Effect Simulation for Efficient Safety Analysis 1132 <i>Jo Laufenberg, Sebastian Reiter, Alexander Viehl, Oliver Bringmann, Thomas Kropf and Wolfgang Rosenstiel</i>
IP4-7	Packet Security with Path Sensitization for NoCs 1136 <i>Travis Boraten and Avinash Karanth Kodi</i>
IP4-8	Synthesis of Approximate Coders for On-chip Interconnects Using Reversible Logic 1140 <i>Robert Wille, Oliver Keszocze, Stefan Hillmich, Marcel Walter and Alberto Garcia-Ortiz</i>
IP4-9	Design-Synthesis Co-Optimisation Using Skewed and Tapered Gates 1144 <i>Ayan Datta, James D. Warnock, Ankur Shukla, Saurabh Gupta, Yiu. H. Chan, Karthik Mohan and Charudhattan Nagarajan</i>
IP4-10	A Synthesis-Parameter Tuning System for Autonomous Design-Space Exploration 1148 <i>Matthew M. Ziegler, Hung-Yi Liu, George Gristede, Bruce Owens, Ricardo Nigaglioni and Luca P. Carloni</i>
IP4-11	Unbounded Safety Verification for Hardware Using Software Analyzers 1152 <i>Rajdeep Mukherjee, Peter Schrammel, Daniel Kroening and Tom Melham</i>
IP4-12	Verilog2SMV: A Tool for Word-level Verification 1156 <i>Ahmed Irfan, Alessandro Cimatti, Alberto Griggio, Marco Roveri and Roberto Sebastiani</i>
IP4-13	Towards Formal Verification of Real-World SystemC TLM Peripheral Models — A Case Study 1160 <i>Hoang M. Le, Vladimir Herdt, Daniel Große and Rolf Drechsler</i>

IP4-14 Frequency Scheduling For Resilient Chip Multi-Processors Operating at Near Threshold Voltage 1164
Ying Wang, Huawei Li and Xiaowei Li

IP4-15 A Low Overhead Error Confinement Method based on Application Statistical Characteristics 1168
Zheng Wang, Georgios Karakonstantis and Anupam Chattopadhyay

Session Title	SPECIAL DAY Hot Topic: Lightweight Security for Embedded Processors
Session Code / Room	10.1 / Saal 2
Date / Time	Thursday, 17 March 2016 / 11:00 – 12:30
Chair	Tilo Müller, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE
Co-Chair	Patrick Schaumont, Virginia Tech, US

10.1.1 Scaling Down: Lightweight Approaches to IoT Security N/A
11:00 – 11:30 *Patrick Koeberl*

10.1.2 SOFIA: Software and Control Flow Integrity Architecture 1172
11:30 – 12:00 *Ruan de Clercq, Ronald De Keulenaer, Bart Coppens, Bohan Yang, Pieter Maene, Koen de Bosschere, Bart Preneel, Bjorn de Sutter and Ingrid Verbauwhede*

0.1.3 Trust, But Verify: Why and How to Establish Trust in Embedded Devices 1178
12:00 – 12:30 *Aurélien Francillon*

Session Title	Does it Work or NoC?
Session Code / Room	10.2 / Konferenz 6
Date / Time	Thursday, 17 March 2016 / 11:00 – 12:30
Chair	Davide Bertozzi, University of Ferrara, IT
Co-Chair	Kees Goossens, Eindhoven University of Technology, NL

10.2.1 CrossOver: Clock Domain Crossing under Virtual-Channel Flow Control 1183
11:00 – 11:30 *Michalis Paschou, Anastasios Psarras, Chrysostomos Nicopoulos and Giorgos Dimitrakopoulos*

10.2.2 Correct Runtime Operation for NoCs through Adaptive-Region Protection 1189
11:30 – 12:00 *Rawan Abdel-Khalek and Valeria Bertacco*

10.2.3 Fault-Tolerant 3-D Network-on-Chip Design using Dynamic Link Sharing 1195
12:00 – 12:30 *Seyyed Hossein Seyyedaghaei Rezaei, Mehdi Modarressi, Reza Yazdani Aminabadi and Masoud Daneshtalab*

Session Title	Design Experiences for Multimedia and Communication Applications
Session Code / Room	10.3 / Konferenz 1
Date / Time	Thursday, 17 March 2016 / 11:00 – 12:30
Chair	Theocharis THEOCHARIDES, <i>University of Cyprus, CY</i>
Co-Chair	Steffen Paul, <i>University Bremen, DE</i>

- 10.3.1** Enabling the Heterogeneous Accelerator Model on Ultra-Low Power
11:00 – 11:30 Microcontroller Platforms 1201
Francesco Conti, Daniele Palossi, Andrea Marongiu, Davide Rossi and Luca Benini
- 10.3.2** Thermal Optimization using Adaptive Approximate Computing for Video Coding 1207
11:30 – 12:00 *Daniel Palomino, Muhammad Shafique, Altamiro Susin and Jörg Henkel*
- 10.3.3** High Performance Time-of-Flight and Color Sensor Fusion with Image-Guided
12:00 – 12:15 Depth Super Resolution 1213
Hannes Plank, Gerald Holweg, Thomas Herndl and Norbert Druml
- 10.3.4** Saturated Min-Sum Decoding: An “Afterburner” for LDPC Decoder Hardware 1219
12:15 – 12:30 *S. Scholl, P. Schläfer and N. When*

Session Title	Stochastic Methods for Circuit Analysis & Synthesis
Session Code / Room	10.4 / Konferenz 2
Date / Time	Thursday, 17 March 2016 / 11:00 – 12:30
Chair	Michal Rewiński, <i>Technical University of Gdansk, PL</i>
Co-Chair	L. Miguel Silveira, <i>INESC-ID, IST, U Lisboa, PT</i>

- 10.4.1** Utilizing Macromodels in Floating Random Walk Based Capacitance Extraction 1225
11:00 – 11:30 *Wenjian Yu, Bolong Zhang, Chao Zhang, Haiquan Wang and Luca Daniel*
- 10.4.2** Variability and Statistical Analysis Flow for Dynamic Linear Systems with Large
11:30 – 12:00 Number of Inputs 1231
A. Lucas Martins, Jorge Fernández Villena and L. Miguel Silveira
- 10.4.3** Variation-Aware Near Threshold Circuit Synthesis 1237
12:00 – 12:30 *Mohammad Saber Golanbari, Saman Kiamehr, Mojtaba Ebrahimi and Mehdi B. Tahoori*

Session Title	Enhancing Memory in Next-Generation Platforms
Session Code / Room	10.5 / Konferenz 3
Date / Time	Thursday, 17 March 2016 / 11:00 – 12:30
Chair	Fancisco Cazorla, Barcelona Supercomputing Center, ES
Co-Chair	Jeronimo Castrillon, Technische Universität Dresden, DE

10.5.1 Buffered Compares: Excavating the Hidden Parallelism Inside DRAM Architectures with Lightweight Logic 1243
11:00 – 11:30 *Jinho Lee, Jung Ho Ahn and Kiyoun Choi*

10.5.2 Large Vector Extensions Inside the HMC 1249
11:30 – 12:00 *Marco A. Z. Alves, Matthias Diener, Paulo C. Santos and Luigi Carro*

10.5.3 minFlash: A Minimalistic Clustered Flash Array 1255
12:00 – 12:30 *Ming Liu, Sang-Woo Jun, Sungjin Lee, Jamey Hicks and Arvind*

Session Title	Compilers and Tools for GPUs and MPSoCs
Session Code / Room	10.6 / Konferenz 4
Date / Time	Thursday, 17 March 2016 / 11:00 – 12:30
Chair	Frank Hannig, University of Erlangen-Nürnberg, DE
Co-Chair	Lars Bauer, Karlsruhe Institute of Technology, DE

10.6.1 An Optimized Task-Based Runtime System for Resource-Constrained Parallel Accelerators 1261
11:00 – 11:30 *Daniele Cesarini, Andrea Marongiu and Luca Benini*

10.6.2 A Fine-grained Performance Model for GPU Architectures 1267
11:30 – 12:00 *Nicola Bombieri, Federico Busato and Franco Fummi*

10.6.3 Critical Points Based Register-Concurrency Autotuning for GPUs 1273
12:00 – 12:15 *Ang Li, Shuaiwen Leon Song, Akash Kumar, Eddy Z. Zhang, Daniel Chavarria-Miranda and Henk Corporaal*

10.6.4 GRATER: An Approximation Workflow for Exploiting Data-Level Parallelism in FPGA Acceleration 1279
12:15 – 12:30 *Atieh Lotfi, Abbas Rahimi, Amir Yazdanbakhsh, Hadi Esmaeilzadeh and Rajesh K. Gupta*

Session Title	Reliable System Design
Session Code / Room	10.7 / Konferenz 5
Date / Time	Thursday, 17 March 2016 / 11:00 – 12:30
Chair	Mohamed Sabry Aly, Stanford University, US
Co-Chair	Semeen Rehman, Karlsruhe Institute of Technology, DE

- 10.7.1** A Holistic Tri-region MLC STT-RAM Design with Combined Performance, Energy, and Reliability Optimizations 1285
11:00 – 11:30 *Wujie Wen, Mengjie Mao, Hai Li, Yiran Chen, Yukui Pei and Ning Ge*
- 10.7.2** Thermal-aware TSV Repair for Electromigration in 3D ICs 1291
11:30 – 12:00 *Shengcheng Wang, Mehdi B. Tahoori and Krishnendu Chakrabarty*
- 10.7.3** Electrothermal Simulation of Bonding Wire Degradation under Uncertain Geometries 1297
12:00 – 12:30 *Thorben Casper, Herbert De Gerssem, Renaud Gillon, Tomas Gotthans, Tomas Kratochvil, Peter Meuris, Sebastian Schöps*

Session Title	Lunch Time Keynote Session
Session Code / Room	11.0
Date / Time	Thursday, 17 March 2016 / 13:30 – 14:00
Chair	Luca Fanucci, University of Pisa, IT
Co-Chair	Matthias Schunter, Intel Corporation, DE

- 11.0.1** [Keynote] Secure Silicon: Enabler for the Internet of Things xxxi
13:30 – 14:00 *Walden C. Rhines*

Session Title	SPECIAL DAY Hot Topic: Embedded Security Applications
Session Code / Room	11.1 / Saal 2
Date / Time	Thursday, 17 March 2016 / 14:00 – 15:30
Chair	Tim Güneysu, University of Bremen, DE
Co-Chair	X. Sharon Hu, University of Notre Dame, US

- 11.1.1** Smart Grid Security
14:00 – 14:30 *Klaus Kursawe*
- 11.1.2** Security In Industrie 4.0 — Challenges and Solutions for the Fourth Industrial Revolution 1303
14:30 – 15:00 *Michael Waidner and Michael Kasper*

11.1.3 Security for Automotive and the Internet of Things N/A
15:00 – 15:30 *Paul Duplys, Hans Löhr, Herve Seudie and Robert Szerwinski*

Session Title	Beating New Technology Paths for NoC
Session Code / Room	11.2 / Konferenz 6
Date / Time	Thursday, 17 March 2016 / 14:00 – 15:30
Chair	Partha Pande, WSU, US
Co-Chair	Sébastien Le Beux, Le Beux, FR

11.2.1 Cross-layer Floorplan Optimization For Silicon Photonic NoCs In Many-core Systems 1309
14:00 – 14:30 *Ayse K. Coskun, Anjun Gu, Warren Jin, Ajay Joshi, Andrew B. Kahng, Jonathan Klamkin, Yenai Ma, John Recchio, Vaishnav Srinivas and Tiansheng Zhang*

11.2.2 Adaptive Multi-Voltage Scaling in Wireless NoC for High Performance Low Power Applications 1315
14:30 – 15:00 *Hemanta Kumar Mondal, Sri Harsha Gade, Raghav Kishore and Sujay Deb*

11.2.3 Energy Efficient Transceiver in Wireless Network on Chip Architectures 1321
15:00 – 15:30 *Vincenzo Catania, Andrea Mineo, Salvatore Monteleone, Maurizio Palesi and Davide Patti*

Session Title	Microarchitectures and Workload Allocation for Energy Efficiency
Session Code / Room	11.3 / Konferenz 1
Date / Time	Thursday, 17 March 2016 / 14:00 – 15:30
Chair	Andrea Bartolini, Univ. of Bologna, IT
Co-Chair	Andreas Burg, EPFL, CH

11.3.1 Resistive Configurable Associative Memory for Approximate Computing 1327
14:00 – 14:30 *Mohsen Imani, Abbas Rahimi and Tajana S. Rosing*

11.3.2 Exploiting CPU-Load and Data Correlations in Multi-Objective VM Placement for Geo-Distributed Data Centers 1333
14:30 – 15:00 *Ali Pahlevan, Pablo Garcia del Valle and David Aienza*

11.3.3 Energy Efficiency in Cloud-Based MapReduce Applications through Better Performance Estimation 1339
15:00 – 15:15 *Seyed Morteza Nabavinejad and Maziar Goudarzi*

11.3.4 Unsupervised Power Modeling of Co-Allocated Workloads for Energy Efficiency in Data Centers 1345
15:15 – 15:30 *Juan C. Salinas-Hilburg, Marina Zapater, José L. Risco-Martín, José M. Moya and José L. Ayala*

Session Title	Automating Test Generation, Assertions and Diagnosis
Session Code / Room	11.4 / Konferenz 2
Date / Time	Thursday, 17 March 2016 / 14:00 – 15:30
Chair	Pablo Sanchez, <i>University of Cantabria, ES</i>
Co-Chair	Ronny Morad, <i>IBM, IL</i>
11.4.1 14:00 – 14:30	Automated Test Generation for Debugging Arithmetic Circuits 1351 <i>Farimah Farahmandi and Prabhat Mishra</i>
11.4.2 14:30 – 15:00	MCXplore: An Automated Framework for Validating Memory Controller Designs 1357 <i>Mohamed Hassan and Hiren Patel</i>
11.4.3 15:00 – 15:15	EAST: Efficient Assertion Simulation Techniques 1363 <i>Debjyoti Bhattacharjee, Soumi Chattopadhyay and Ansuman Banerjee</i>
11.4.4 15:15 – 15:30	Combinational Trace Signal Selection with Improved State Restoration for Post-Silicon Debug 1369 <i>Siamack BeigMohammadi and Bijan Alizadeh</i>

Session Title	Design of Efficient Microarchitectures
Session Code / Room	11.5 / Konferenz 3
Date / Time	Thursday, 17 March 2016 / 14:00 – 15:30
Chair	Dionisios Pnevmatikatos, <i>Technical University of Crete, GR</i>
Co-Chair	Todd Austin, <i>University of Michigan, US</i>
11.5.1 14:00 – 14:30	Practical Way Halting by Speculatively Accessing Halt Tags 1375 <i>Daniel Moreau, Alen Bardizbanyan, Magnus Sjölander, David Whalley and Per Larsson-Edefors</i>
11.5.2 14:30 – 15:00	Lazy Pipelines: Enhancing Quality in Approximate Computing 1381 <i>G. Tziantzioulis, A. M. Gok, S. M. Faisal, N. Hardavellas, S. Ogrenci-Memik and S. Parthasarathy</i>
11.5.3 15:00 – 15:30	High-Efficiency Logarithmic Number Unit Design based on an Improved Cotransformation Scheme 1387 <i>Youri Popoff, Florian Scheidegger, Michael Schaffner, Michael Gautschi, Frank K. Gürkaynak and Luca Benini</i>

Session Title	Applications of Reconfigurable Computing
Session Code / Room	11.6 / Konferenz 4
Date / Time	Thursday, 17 March 2016 / 14:00 – 15:30
Chair	Alessandro Cilardo, University of Naples Federico II, IT
Co-Chair	Koen Bertels, Delft University of Technology, NL

- 11.6.1** Efficient FPGA Acceleration of Convolutional Neural Networks Using Logical-3D Compute Array 1393
14:00 – 14:30 *Atul Rahman, Jongeun Lee and Kiyoun Choi*
- 11.6.2** Energy Efficient Video Fusion with Heterogeneous CPU-FPGA Devices 1399
14:30 – 15:00 *Peng Sun, Alin Achim, Ian Hasler, Paul Hill and Jose Nunez-Yanez*
- 11.6.3** Highly Efficient Reconfigurable Parallel Graph Cuts for Embedded Vision 1405
15:00 – 15:30 *Antonis Nikitakis and Ioannis Papaefstathiou*

Session Title	Naked Analog Synthesis
Session Code / Room	11.7 / Konferenz 5
Date / Time	Thursday, 17 March 2016 / 14:00 – 15:30
Chair	Árpád Árpád Bürmen, University of Ljubljana, SI
Co-Chair	Francisco Fernandez, IMSE-CNM, ES

- 11.7.1** Pareto Front Analog Layout Placement using Satisfiability Modulo Theories 1411
14:00 – 14:30 *Sherif M. Saif, Mohamed Dessouky, M. Watheq El-Kharashi, Hazem Abbas and Salwa Nassar*
- 11.7.2** Efficient Multiple Starting Point Optimization for Automated Analog Circuit Optimization via Recycling Simulation Data 1417
14:30 – 15:00 *Bo Peng, Fan Yang, Changhao Yan, Xuan Zeng and Dian Zhou*
- 11.7.3** PolyGP: Improving GP-Based Analog Optimization through Accurate High-Order Monomials and Semidefinite Relaxation 1423
15:00 – 15:30 *Ye Wang, Constantine Caramanis and Michael Orshansky*

Session Title	Interactive Presentations
Session Code / Room	IP5
Date / Time	Thursday, 17 March 2016 / 15:30 – 16:00

- IP5-1** Reliability and Performance Trade-offs for 3D NoC-Enabled Multicore Chips 1429
Sourav Das, Janardhan Rao Doppa, Partha Pratim Pande and Krishnendu Chakrabarty

- IP5-2** Memory-Access Aware DVFS for Network-on-Chip in CMPs 1433
Yuan Yao and Zhonghai Lu
- IP5-3** A Dynamically Reconfigurable ECC Decoder Architecture 1437
Awais Sani, Philippe Coussy and Cyrille Chavet
- IP5-4** Resistive Bloom Filters: From Approximate Membership to Approximate Computing with Bounded Errors 1441
Vahideh Akhlaghi, Abbas Rahimi and Rajesh K. Gupta
- IP5-5** Real-Time System-Level Implementation of a Telepresence Robot Using an Embedded GPU Platform 1445
Muhammad Teguh Satria, Swathi Gurumani, Wang Zheng, Keng Peng Tee, Augustine Koh, Pan Yu, Kyle Rupnow and Deming Chen
- IP5-6** Exploring Specialized Near-Memory Processing for Data Intensive Operations 1449
Salessawi Ferede Yitbarek, Tao Yang, Reetuparna Das and Todd Austin
- IP5-7** Matlab to C Compilation Targeting Application Specific Instruction Set Processors 1453
Ioannis Latifis, Karthick Parashar, Grigoris Dimitroulakos, Hans Cappelle, Christakis Lezos, Konstantinos Masselos and Francky Catthoor
- IP5-8** Sampling-based Buffer Insertion for Post-Silicon Yield Improvement under Process Variability 1457
Grace Li Zhang, Bing Li and Ulf Schlichtmann
- IP5-9** PRADA: Combating Voltage Noise in the NoC Power Supply Through Flow-Control and Routing Algorithms 1461
Prabal Basu, Rajesh Jayashankara Shridevi, Koushik Chakraborty and Sanghamitra Roy
- IP5-10** A Power-Efficient 3-D On-Chip Interconnect for Multi-Core Accelerators with Stacked L2 Cache 1465
Kyungsu Kang, Sangho Park, Jong-Bae Lee, Luca Benini and Giovanni De Micheli
- IP5-11** Power-Efficient Load-Balancing on Heterogeneous Computing Platforms 1469
Muhammad Usman Karim Khan, Muhammad Shafique, Apratim Gupta, Thomas Schumann and Jörg Henkel
- IP5-12** Topaz: Mining High-Level Safety Properties from Logic Simulation Traces 1473
Ahmed Nassar, Fadi J. Kurdahi and Salam R. Zantout
- IP5-13** Exploiting Transaction Level Models for Observability-aware Post-silicon Test Generation 1477
Farimah Farahmandi, Prabhat Mishra and Sandip Ray
- IP5-14** SEERAD: A High Speed yet Energy-Efficient Rounding-based Approximate Divider 1481
Reza Zendegani, Mehdi Kamal, Arash Fayyazi, Ali Afzali-Kusha, Saeed Safari and Massoud Pedram
- IP5-15** Improving Performance Guarantees in Wormhole Mesh NoC Designs 1485
Miloš Panić, Carles Hernandez, Jaume Abella, Antoni Roca, Eduardo Quiñonesy and Francisco J. Cazorla

- IP5-16** A Data Layout Transformation (DLT) Accelerator: Architectural Support for Data Movement Optimization in Accelerated-centric Heterogeneous Systems 1489
Tung Thanh-Hoang, Amirali Shambayati and Andrew A. Chien
- IP5-17** Ouessant: Flexible Integration of Dedicated Coprocessors in Systems On Chip 1493
Pierre-Henri Horrein, Philip-Dylan Gleonec, Erwan Libessart, André Lalevée and Matthieu Arzel
- IP5-18** A novel Background Subtraction Scheme for in-Camera Acceleration in Thermal Imagery 1497
Antonis Nikitakis, Ioannis Papaefstathiou, Konstantinos Makantasis and Anastasios Doulamis
- IP5-19** Radiation-Hardened DSP Configurations for Implementing Arithmetic Functions on FPGA 1501
Marcos Sanchez-Elez, Inmaculada Pardines, Felipe Serrano and Hortensia Mecha
- IP5-20** Configuration Prefetching and Reuse for Preemptive Hardware Multitasking on Partially Reconfigurable FPGAs 1505
Aurelio Morales-Villanueva, Rohit Kumar and Ann Gordon-Ross
- IP5-21** Analog Circuit Topological Feature Extraction with Unsupervised Learning of New Sub-Structures 1509
Hao Li, Fanshu Jiao and Alex Daboli
- IP5-22** Design Automation Tasks Scheduling for Enhanced Parallel Execution of a State-of-the-Art Layout-Aware Sizing Approach 1513
David Neves, Ricardo Martins, Nuno Lourenço and Nuno Horta

Session Title	SPECIAL DAY Hot Topic: Design Methods for Security and Trust
Session Code / Room	12.1 / Saal 2
Date / Time	Thursday, 17 March 2016 / 16:00 – 17:30
Chair	Jean-Luc Danger, Télécom ParisTech, FR
Co-Chair	Ilia Polian, Universität Passau, DE

- 12.1.1** A Design Method for Remote Integrity Checking of Complex PCBs 1517
16:00 – 16:30
Aydin Aysu, Shravya Gaddam, Harsha Mandadi, Carol Pinto, Luke Wegryn and Patrick Schaumont
- 12.1.2** Quantifying Hardware Security Using Joint Information Flow Analysis 1523
16:30 – 17:00
Ryan Kastner, Wei Hu and Alric Althoff
- 12.1.3** Instruction Set Extensions for Secure Applications 1529
17:00 – 17:30
Francesco Regazzoni and Paolo Ienne

Session Title	Hot Topic: Exploiting New Transistor Technologies to Enhance Hardware Security (without PUFs!)
Session Code / Room	12.2 / Konferenz 6
Date / Time	Thursday, 17 March 2016 / 16:00 – 17:30
Organisers	Michael Niemier, <i>University of Notre Dame, South Bend, US</i>
Chair	Sri Parameswaran, <i>The University of New South Wales, AU</i>

- 12.2.1** Hardware Security Through Chain Assurance 1535
16:00 – 16:30 *Yaw Obeng, Colm Nolan and David Brown*
- 12.2.2** Leverage Emerging Technologies For DPA-Resilient Block Cipher Design 1538
16:30 – 17:00 *Yu Bi, Kaveh Shamsi, Jiann-Shiun Yuan, Francois-Xavier Standaer and Yier Jin*
- 12.2.3** Using Emerging Technologies for Hardware Security Beyond PUFs 1544
17:00 – 17:30 *An Chen, X. Sharon Hu, Yier Jin, Michael Niemier and Xunzhao Yin*

Session Title	System Support for Resilience and Robustness
Session Code / Room	12.3 / Konferenz 1
Date / Time	Thursday, 17 March 2016 / 16:00 – 17:30
Chair	Oliver Bringmann, <i>University of Tuebingen, DE</i>
Co-Chair	Dirk Stroobandt, <i>Ghent University, BE</i>

- 12.3.1** Effect of LFSR Seeding, Scrambling and Feedback Polynomial on Stochastic Computing Accuracy 1550
16:00 – 16:30 *Jason H. Anderson, Yuko Hara-Azumi and Shigeru Yamashita*
- 12.3.2** Efficient Program Tracing and Monitoring Through Power Consumption — With a Little Help from the Compiler 1556
16:30 – 17:00 *Carlos Moreno, Sean Kauffman and Sebastian Fischmeister*
- 12.3.3** FLIC: Fast, Lightweight Checkpointing for Mobile Virtualization using NVRAM 1562
17:00 – 17:15 *Kan Zhong, Duo Liu, Liang Liang, Linbo Long, Yi Lin and Zili Shao*
- 12.3.4** PAIS: Parallelization Aware Instruction Scheduling for Improving Soft-error Reliability of GPU-based Systems 1568
17:15 – 17:30 *Haeseung Lee, Hsinchung Chen and Mohammad Abdullah Al Faruque*

Session Title	Simulating Everything: From Timing to Instructions
Session Code / Room	12.4 / Konferenz 2
Date / Time	Thursday, 17 March 2016 / 16:00 – 17:30
Chair	Elena Ioana Vatajelu, Politecnico di Torino, IT
Co-Chair	Valeria Bertacco, University of Michigan, US

- 12.4.1** Accelerating Source-Level Timing Simulation 1574
16:00 – 16:30 *Simon Schulz and Oliver Bringmann*
- 12.4.2** Sparsity-Oriented Sparse Solver Design for Circuit Simulation 1580
16:30 – 17:00 *Xiaoming Chen, Lixue Xia, Yu Wang and Huazhong Yang*
- 12.4.3** Integration of Mixed-signal Components into Virtual Platforms for Holistic Simulation of Smart Systems 1586
17:00 – 17:15 *Enrico Fraccaroli, Michele Lora, Sara Vinco, Davide Quaglia and Franco Fummi*
- 12.4.4** Decision Tree Generation for Decoding Irregular Instructions 1592
17:15 – 17:30 *Katsumi Okuda and Haruhiko Takeyama*

Session Title	Accelerator Design and Heterogeneous Architectures
Session Code / Room	12.5 / Konferenz 3
Date / Time	Thursday, 17 March 2016 / 16:00 – 17:30
Chair	Cristina Silvano, Politecnico di Milano, IT
Co-Chair	Todd Austin, University of Michigan, US

- 12.5.1** A Reconfigurable Heterogeneous Multicore with a Homogeneous ISA 1598
16:00 – 16:30 *Jeckson Dellagostin Souza, Luigi Carro, Mateus Beck Rutzig and Antonio Carlos Schneider Beck*
- 12.5.2** The Neuro Vector Engine: Flexibility to Improve Convolutional Net Efficiency for Wearable Vision 1604
16:30 – 17:00 *Maurice Peemen, Runbin Shi, Sohan Lal, Ben Juurlink, Bart Mesman and Henk Corporaal*
- 12.5.3** Improving Scalability of CMPs with Dense ACCs Coverage 1610
17:00 – 17:15 *Nasibeh Teimouri, Hamed Tabkhi and Gunar Schirner*
- 12.5.4** Hardware Accelerator for Analytics of Sparse Data 1616
17:15 – 17:30 *Eriko Nurvitadhi, Asit Mishra, Yu Wang, Ganesh Venkatesh and Debbie Marr*

Session Title	Reconfigurable Computing Platforms and Architectures
Session Code / Room	12.6 / Konferenz 4
Date / Time	Thursday, 17 March 2016 / 16:00 – 17:30
Chair	Dirk Stroobandt, Ghent University, BE
Co-Chair	Jürgen Becker, Karlsruhe Institute of Technology, DE
12.6.1 16:00 – 16:30	Securing the Cloud with Reconfigurable Computing: An FPGA Accelerator for Homomorphic Encryption 1622 <i>Alessandro Cilardo and Domenico Argenziano</i>
12.6.2 16:30 – 17:00	Throughput Oriented FPGA Overlays Using DSP Blocks 1628 <i>Abhishek Kumar Jain, Douglas L. Maskell and Suhaib A. Fahmy</i>
12.6.3 17:00 – 17:30	Run-time Phase Prediction for a Reconfigurable VLIW Processor 1634 <i>Qi Guo, Anderson Sartor, Anthony Brandon, Antonio C. S. Beck, Xuehai Zhou and Stephan Wong</i>

Session Title	Formal System Level Verification
Session Code / Room	12.7 / Konferenz 5
Date / Time	Thursday, 17 March 2016 / 16:00 – 17:30
Chair	Mathias Soeken, EPFL, CH
Co-Chair	Gianpiero Cabodi, Politecnio di Torino, IT
12.7.1 16:00 – 16:30	ADVOCAT: Automated Deadlock Verification for On-chip Cache Coherence and Interconnects 1640 <i>Freek Verbeek, Pooria M. Yaghini, Ashkan Eghbal and Nader Bagherzadeh</i>
12.7.2 16:30 – 17:00	Guarantees for Runnable Entities with Heterogeneous Real-Time Requirements 1646 <i>Leonie Ahrendts, Zain A. H. Hammadeh and Rolf Ernst</i>
12.7.3 17:00 – 17:30	Validating Scheduling Transformation for Behavioral Synthesis 1652 <i>Zhenkun Yang, Kecheng Hao, Kai Cong, Li Lei, Sandip Ray and Fei Xie</i>

Additional Papers:

HPAZ: A High-Throughput Pipeline Architecture of ZUC in Hardware 269
Zongbin Liu, Qinglong Zhang, Cunjing Ma, Changline, Jiwu Jing

Recursive Hierarchical DFT Methodology with Multi-Level Clock Control and Scan Pattern Retargeting 1128
Dan Trock, Rick Fisette