

2016 International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS 2016)

**Istanbul, Turkey
12-14 April 2016**



**IEEE Catalog Number: CFP1693A-POD
ISBN: 978-1-5090-0337-2**

**Copyright © 2016 by the Institute of Electrical and Electronics Engineers, Inc
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

******This publication is a representation of what appears in the IEEE Digital Libraries. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP1693A-POD
ISBN (Print-On-Demand):	978-1-5090-0337-2
ISBN (Online):	978-1-5090-0336-5

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

TABLE OF CONTENTS

DO YOU TRUST YOUR CHIP?	1
<i>Ozgur Sinanoglu</i>	
A GENETIC ALGORITHM BASED REMAINING LIFETIME PREDICTION FOR A VLIW PROCESSOR EMPLOYING PATH DELAY AND IDDX TESTING	2
<i>Yong Zhao ; Hans G. Kerkhoff</i>	
IMPLEMENTATION OF A SECURED DIGITAL ULTRALIGHT 14443-TYPE A RFID TAG WITH AN FPGA PLATFORM	6
<i>Yassine Najja ; Vincent Berouille ; David Hely ; Mohsen Machhout</i>	
RESIDUE NUMBER SYSTEM AS A SIDE CHANNEL AND FAULT INJECTION ATTACK COUNTERMEASURE IN ELLIPTIC CURVE CRYPTOGRAPHY	9
<i>Apostolos P. Fournaris ; Louiza Papachristodoulou ; Lejla Batina ; Nicolas Sklavos</i>	
AN EFFICIENT MAPPING ALGORITHM ON 2-D MESH NETWORK-ON-CHIP WITH RECONFIGURABLE SWITCHES	13
<i>Salih Bayar ; Arda Yurdakul</i>	
IDENTIFICATION OF DELAY DEFECTS ON EMBEDDED PATHS USING ONE CURRENT SENSOR	17
<i>Wisam Aljubouri ; Spyros Tragoudas ; Themistoklis Haniotakis</i>	
SECUBE™: AN OPEN-SOURCE SECURITY PLATFORM IN A SINGLE SOC	21
<i>Antonio Varriale ; Elena Ioana Vatajelu ; Giorgio Di Natale ; Paolo Prinetto ; Pascal Trotta ; Tiziana Margarita</i>	
SIMPLE TRI-STATE LOGIC TROJANS ABLE TO UPSET PROPERTIES OF RING OSCILLATORS	27
<i>Leonel Acunha Guimaraes ; Rodrigo Possamai Bastos ; Thiago Ferreira De Paiva Leite ; Laurent Fesquet</i>	
QUALITATIVE TECHNIQUES FOR SYSTEM-ON-CHIP TEST WITH LOW-ENERGY PROTONS	33
<i>Stefano Di Mascio ; Marco Ottavi ; Gianluca Furano ; Tomasz Szewczyk ; Alessandra Menicucci ; Luigi Campajola ; Francesco Di Capua</i>	
EFFICIENT SELECTION OF CRITICAL PATHS FOR DELAY DEFECTS IN THE PRESENCE OF PROCESS VARIATIONS	39
<i>Phaninder Alladi ; Spyros Tragoudas</i>	
DYNAMICALLY RECONFIGURABLE FFT PROCESSOR FOR FLEXIBLE OFDM BASEBAND PROCESSING	45
<i>Mario Lopes Ferreira ; Amin Barahimi ; Joao Canas Ferreira</i>	
FUSED MODULO $2^N + 1$ ADD-MULTIPLY UNIT FOR WEIGHTED OPERANDS	51
<i>Kiamal Pekmestzi ; Kostas Tsoumanis ; Constantinos Efstathiou</i>	
FPGA IMPLEMENTATION OF A FAULT-TOLERANT APPLICATION-SPECIFIC NOC DESIGN	57
<i>Serif Yesil ; Suleyman Tosun ; Ozcan Ozturk</i>	
EVOLVABLE HARDWARE IN FPGAS: EMBEDDED TUTORIAL	63
<i>Ruben Salvador</i>	
APPROXIMATE COMPUTING FOR UNRELIABLE SILICON	69
<i>Andreas Peter Burg</i>	
ANALYTICAL OPTIMIZATION OF INTERDIGITATED STRUCTURE FOR BIOLOGICAL MEDIUM CHARACTERIZATION	70
<i>M. Dekmous ; A. Lakhdari ; H. Mouhadjer ; N. Mekkakia-Maaza</i>	
LOWPASS FILTER DESIGN TECHNIQUE FOR HYBRID AND MONOLITHIC IMPLEMENTATION	74
<i>Faycal Amrani ; Mohamed Trabelsi ; Abdelhalim A. Saadi ; Rachida Touhami</i>	
MAC UNIT FOR RECONFIGURABLE SYSTEMS USING MULTI-OPERAND ADDERS WITH DOUBLE CARRY-SAVE ENCODING	78
<i>Ugur Cini ; Olcay Kurt</i>	
REGISTER FILE RELIABILITY ENHANCEMENT THROUGH ADJACENT NARROW-WIDTH EXPLOITATION	82
<i>Hamzeh Ahangari ; Ihsen Alouani ; Ozcan Ozturk ; Smail Niar ; Atika Rivencq</i>	
FPGA IMPLEMENTATIONS OF HEVC SUB-PIXEL INTERPOLATION USING HIGH-LEVEL SYNTHESIS	86
<i>Firas Abdul Ghani ; Ercan Kalali ; Ilker Hamzaoglu</i>	

A HIGH PERFORMANCE HARDWARE FOR EARLY TERMINATED C-1BT BASED MOTION ESTIMATION	90
<i>Abdulkadir Akin ; Ilker Hamzaoglu</i>	
AUTOMATIC DESIGN OF APPROXIMATE CIRCUITS BY MEANS OF MULTI-OBJECTIVE EVOLUTIONARY ALGORITHMS.....	94
<i>Radek Hrbacek ; Vojtech Mrazek ; Zdenek Vasicek</i>	
AUTO-ADAPTIVE ULTRA-LOW POWER IC	100
<i>A. Bosio ; P. Debaud ; P. Girard ; S. Guilhot ; M. Valka ; A. Virazel</i>	
VOLTAGE OVER-SCALING IN SEQUENTIAL CIRCUITS FOR APPROXIMATE COMPUTING.....	106
<i>David May ; Walter Stechele</i>	
AN EXTENDIBLE DESIGN EXPLORATION TOOL FOR SUPPORTING APPROXIMATE COMPUTING TECHNIQUES.....	112
<i>Mario Barbareschi ; Federico Iannucci ; Antonino Mazzeo</i>	
BOOLEAN LOGIC GATE EXPLORATION FOR MEMRISTOR CROSSBAR	118
<i>Lei Xie ; Hoang Anh Du Nguyen ; Mottaqiallah Taouil ; Said Hamdioui ; Koen Bertels</i>	
A NOVEL HETEROGENEOUS FPGA ARCHITECTURE BASED ON MEMRISTOR-TRANSISTOR HYBRID APPROACH	124
<i>Umer Farooq ; M. Khurram Bhatti ; M. Hassan Aslam</i>	
LETS MOVE POLYMORPHISM DOWNWARDS: ON THE MULTIFUNCTIONAL LOGIC BASED ON AMBIPOLAR BEHAVIOUR OF SEMICONDUCTOR DEVICES	130
<i>Richard Ruzika ; Radek Tesar</i>	
MULTILEVEL OPERATION IN OXIDE BASED RESISTIVE RAM WITH SET VOLTAGE MODULATION	135
<i>H. Aziza ; H. Ayari ; S. Onkaraiah ; M. Moreau ; J-M. Portal ; M. Bocquet</i>	
LOW POWER DIGITAL VIDEO COMPRESSION HARDWARE DESIGN	140
<i>Ilker Hamzaoglu</i>	
OPTIMIZING CMOS ANALOG VARIABLE GAIN AMPLIFIER CELL FOR WIMAX RECEIVER	141
<i>Sawssen Lahiani ; Samir Ben Salem ; Houda Daoud ; Mourad Loulou</i>	
THICKNESS DEPENDENCE INVESTIGATION OF THE MUTUAL INDUCTANCE LINK IN CONCENTRIC PLANAR TRANSFORMERS	147
<i>Hala Ghadhab ; Mohamed Hadj Said ; Fares Tounsi ; Brahim Mezghani ; Sandeep G. Surya ; V. Rangopal Rao</i>	
A DISCRETE IMPLEMENTATION OF A BIDIRECTIONAL CIRCUIT FOR ACTUATION AND READ-OUT OF RESONATING SENSORS	152
<i>Luca Marchetti ; Amar Romi ; Yngvar Berg ; Omid Mirmotahari ; Mehdi Azadmehr</i>	
HIGH SPEED CONTENT ADDRESSABLE MEMORY WITH REDUCED SIZE AND LESS POWER CONSUMPTION	157
<i>Hammad Riaz ; Abdul Aziz Bhatti ; Muhammad Ashraf Tahir ; Muhammad Sarwar</i>	
HIGH-SPEED DYNAMIC DUAL-RAIL ULTRA LOW VOLTAGE STATIC CMOS LOGIC OPERATING AT 300 MV	163
<i>Omid Mirmotahari ; Ali Dadashi Nanoelectronics ; Mehdi Azadmehr ; Yngvar Berg</i>	
INVESTIGATION OF TRANSFER-FREE CATALYTIC CVD GRAPHENE ON SiO₂ BY MEANS OF CONDUCTIVE ATOMIC FORCE MICROSCOPY	167
<i>D. Noll ; U. Schwalke</i>	
TIP-ENHANCED RAMAN SCATTERING OF 4H-SiC FILMS	171
<i>Ru Han ; Danghui Wang</i>	
Author Index	