

2016 IEEE 24th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM 2016)

**Washington, DC, USA
1 – 3 May 2016**



**IEEE Catalog Number: CFP16054-POD
ISBN: 978-1-5090-2357-8**

**Copyright © 2016 by the Institute of Electrical and Electronics Engineers, Inc
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

******This publication is a representation of what appears in the IEEE Digital Libraries. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP16054-POD
ISBN (Print-On-Demand):	978-1-5090-2357-8
ISBN (Online):	978-1-5090-2356-1

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

2016 IEEE 24th Annual International Symposium on Field-Programmable Custom Computing Machines

FCCM 2016

Table of Contents

Message from General Chairxi
Organizing Committeexiii
Program Committeexiv
Additional Reviewersxvi
Sponsorsxvii

Session 1: Overlays

DeCO: A DSP Block Based FPGA Accelerator Overlay with Low Overhead Interconnect	1
<i>Abhishek Kumar Jain, Xiangwei Li, Pranjul Singhai, Douglas L. Maskell, and Suhaib A. Fahmy</i>	
High Performance Instruction Scheduling Circuits for Out-of-Order Soft Processors	9
<i>Henry Wong, Vaughn Betz, and Jonathan Rose</i>	
GRVI Phalanx: A Massively Parallel RISC-V FPGA Accelerator Accelerator	17
<i>Jan Gray</i>	
Tinker: Generating Custom Memory Architectures for Altera's OpenCL Compiler	21
<i>Dustin Richmond, Jeremy Blackstone, Matthew Hogains, Kevin Thai, and Ryan Kastner</i>	

Posters 1

Evaluating Embedded FPGA Accelerators for Deep Learning Applications	25
<i>Gopalakrishna Hegde, Siddhartha, Nachiappan Ramasamy, Vamsi Buddha, and Nachiket Kapre</i>	
Communication Optimization for the 16-Core Epiphany Floating-Point Processor Array	26
<i>Nachiket Kapre and Siddhartha</i>	
A LUT-Based Approximate Adder	27
<i>Andreas Becher, Jorge Echavarria, Daniel Ziener, Stefan Wildermann, and Jürgen Teich</i>	
Power-Efficient Accelerated Genomic Short Read Mapping on Heterogeneous Computing Platforms	28
<i>Ernst Joachim Houtgast, Vlad-Mihai Sima, Giacomo Marchiori, Koen Bertels, and Zaid Al-Ars</i>	
When Spark Meets FPGAs: A Case Study for Next-Generation DNA Sequencing Acceleration	29
<i>Yu-Ting Chen, Jason Cong, Zhenman Fang, Jie Lei, and Peng Wei</i>	
Parallelism for High-Performance Tsunami Simulation with FPGA: Spatial or Temporal?	30
<i>Kohei Nagasu, Kentaro Sano, Fumiya Kono, Naohito Nakasato, Alexander Vazhenin, and Stanislav Sedukhin</i>	
RP-Ring: A Heterogeneous Multi-FPGA Accelerating Solution for N-Body Simulations	31
<i>Tianqi Wang, Xi Jin, Bo Peng, Chuanjun Wang, and Linlin Zheng</i>	

Session 2: Applications 1 (Artificial Neural Networks and Computational Biology)

The SMEM Seeding Acceleration for DNA Sequence Alignment	32
<i>Mau-Chung Frank Chang, Yu-Ting Chen, Jason Cong, Po-Tsang Huang, Chun-Liang Kuo, and Cody Hao Yu</i>	
fpgaConvNet: A Framework for Mapping Convolutional Neural Networks on FPGAs	40
<i>Stylianos I. Venieris and Christos-Savvas Bouganis</i>	
Increasing Network Size and Training Throughput of FPGA Restricted Boltzmann Machines Using Dropout	48
<i>Jiang Su, David B. Thomas, and Peter Y.K. Cheung</i>	
Two-Hit Filter Synthesis for Genomic Database Search	52
<i>Jordan A. Bradshaw, Rasha Karakchi, and Jason D. Bakos</i>	

Session 3: CAD, Synthesis, and Compilers 1

KAPow: A System Identification Approach to Online Per-Module Power Estimation in FPGA Designs	56
<i>Eddie Hung, James J. Davis, Joshua M. Levine, Edward A. Stott, Peter Y.K. Cheung, and George A. Constantinides</i>	
SynADT: Dynamic Data Structures in High Level Synthesis	64
<i>Zeping Xue and David B. Thomas</i>	
Loop Splitting for Efficient Pipelining in High-Level Synthesis	72
<i>Junyi Liu, John Wickerson, and George A. Constantinides</i>	
Improving Classification Accuracy of a Machine Learning Approach for FPGA Timing Closure	80
<i>Que Yanghua, Nachiket Kapre, Harnhua Ng, and Kirvy Teo</i>	
Knowledge Transfer in Automatic Optimisation of Reconfigurable Designs	84
<i>Maciej Kurek, Marc Peter Deisenroth, Wayne Luk, and Timothy Todman</i>	
Reconfiguration Control Networks for TMR Systems with Module-Based Recovery	88
<i>Dimitris Agiakatsikas, Nguyen T.H. Nguyen, Zhuoran Zhao, Tong Wu, Ediz Cetin, Oliver Diessel, and Lingkan Gong</i>	

Posters 2

Vertex-Centric Graph Processing on FPGA	92
<i>Nina Engelhardt and Hayden Kwok-Hay So</i>	
High-Speed RTL Implementations and FPGA Benchmarking of Three Authenticated Ciphers Competing in CAESAR Round Two	93
<i>William Diehl and Kris Gaj</i>	
Accelerating Apache Spark Big Data Analysis with FPGAs	94
<i>Ehsan Ghasemi and Paul Chow</i>	

Session 4: Applications 2 (Data-centric Energy Efficiency)

Parallel Hardware Merge Sorter	95
<i>Wei Song, Dirk Koch, Mikel Luján, and Jim Garside</i>	
High-Throughput and Energy-Efficient Graph Processing on FPGA	103
<i>Shijie Zhou, Charalampos Chelmiss, and Viktor K. Prasanna</i>	

Session 5: Hardware Debug

Continuous Online Self-Monitoring Introspection Circuitry for Timing Repair by Incremental Partial-Reconfiguration (COSMIC TRIP)	111
<i>Hans Giesen, Benjamin Gojman, Raphael Rubin, Ji Kim, and André DeHon</i>	
Sectors: Divide & Conquer and Softwarization in the Design and Validation of the Stratix® 10 FPGA	119
<i>Dana L. How and Sean Atsatt</i>	
AutoSLIDE: Automatic Source-Level Instrumentation and Debugging for HLS	127
<i>Liwei Yang, Swathi Gurumani, Deming Chen, and Kyle Rupnow</i>	
Cost Effective Partial Scan for Hardware Emulation	131
<i>Tao Li and Qiang Liu</i>	

Posters 3

Initiation Interval Aware Resource Sharing for FPGA DSP Blocks	135
<i>Ronak Bajaj and Suhaib A. Fahmy</i>	
A Dynamically Scheduled Architecture for the Synthesis of Graph Database Queries	136
<i>Marco Minutoli, Vito Giovanni Castellana, Antonino Tumeo, Fabrizio Ferrandi, and Marco Lattuada</i>	
Acceleration of the Pair-HMM Algorithm for DNA Variant Calling	137
<i>Gowthami Jayashri Manikandan, Sitao Huang, Kyle Rupnow, Wen-Mei W. Hwu, and Deming Chen</i>	
An Empirical Analysis of the Fidelity of VPR Area Models	138
<i>Farheen Fatima Khan and Andy Ye</i>	
Heterogeneous Implementation of ECG Encryption and Identification on the Zynq SoC	139
<i>Amine Ait Si Ali, Xiaojun Zhai, Abbas Amira, Faycal Bensaali, and Naeem Ramzan</i>	

Session 6: CAD, Synthesis, and Compilers 2

A Multi-ported Memory Compiler Utilizing True Dual-Port BRAMs	140
<i>Ameer M. S. Abdelhadi and Guy G. F. Lemieux</i>	
P4-to-VHDL: Automatic Generation of 100 Gbps Packet Parsers	148
<i>Pavel Benáček, Viktor Puš, and Hana Kubátová</i>	
Marathon: Statically-Scheduled Conflict-Free Routing on FPGA Overlay NoCs	156
<i>Nachiket Kapre</i>	
Parallelizing FPGA Technology Mapping through Partitioning	164
<i>Chuyu Shen, Zili Lin, Ping Fan, Xianglong Meng, and Weikang Qian</i>	

Online Bandwidth Reduction Using Dynamic Partial Reconfiguration	168
<i>Seyyed Mahdi Najmabadi, Zhe Wang, Yousef Baroud, and Sven Simon</i>	
Energy Efficiency of Full Pipelining: A Case Study for Matrix Multiplication	172
<i>Peipei Zhou, Hyunseok Park, Zhenman Fang, Jason Cong, and André DeHon</i>	

Session 7: Applications 3 (Computational Physics and Geography)

Spatial Predicates Evaluation in the Geohash Domain Using Reconfigurable Hardware	176
<i>Dajung Lee, Roger Moussalli, Sameh Asaad, and Mudhakar Srivatsa</i>	
A Content Adapted FPGA Memory Architecture with Pattern Recognition Capability for L1 Track Triggering in the LHC Environment	184
<i>Tanja Harbaum, Mahmoud Seboui, Matthias Balzer, Jürgen Becker, and Marc Weber</i>	
FPGA-Accelerated Particle-Grid Mapping	192
<i>Ahmed Sanullah, Arash Khoshparvar, and Martin C. Herbordt</i>	

Posters 4

Finding Space-Time Stream Permutations for Minimum Memory and Latency	196
<i>Thaddeus Koehn and Peter Athanas</i>	
Application-Aware Collective Communication (Extended Abstract)	197
<i>Jiayi Sheng, Qingqing Xiong, Chen Yang, and Martin C. Herbordt</i>	
Bridging the Performance-Programmability Gap for FPGAs via OpenCL: A Case Study with OpenDwarfs	198
<i>Konstantinos Krommydas, Ahmed E. Helal, Anshuman Verma, and Wu-Chun Feng</i>	
ECO Based Placement and Routing Framework for 3D FPGAs with Micro-fluidic Cooling	199
<i>Zhiyuan Yang, Caleb Serafy, and Ankur Srivastava</i>	
FPGA-Based Reduction Techniques for Efficient Deep Neural Network Deployment	200
<i>Adam Page and Tinoosh Mohsenin</i>	
CS-Based Secured Big Data Processing on FPGA	201
<i>Amey Kulkarni, Ali Jafari, Colin Shea, and Tinoosh Mohsenin</i>	
High Level Synthesis Based E-Nose System for Gas Applications	202
<i>Amine Ait Si Ali, Abbes Amira, Faycal Bensaali, Mohieddine Benammar, Muhammad Hassan, and Amine Bermak</i>	

Session 8: Applications 4 ("Big Data")

Runtime Parameterizable Regular Expression Operators for Databases	204
<i>Zsolt István, David Sidler, and Gustavo Alonso</i>	
Accelerating Equi-Join on a CPU-FPGA Heterogeneous Platform	212
<i>Ren Chen and Viktor K. Prasanna</i>	
Author Index	220