

# **2016 IEEE Symposium on VLSI Technology (VLSI Technology 2016)**

**Honolulu, Hawaii, USA  
14-16 June 2016**



**IEEE Catalog Number: CFP16VTS-POD  
ISBN: 978-1-5090-0639-7**

**Copyright © 2016 by the Institute of Electrical and Electronics Engineers, Inc  
All Rights Reserved**

*Copyright and Reprint Permissions:* Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

***\*\*\*This publication is a representation of what appears in the IEEE Digital Libraries. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP16VTS-POD
ISBN (Print-On-Demand):	978-1-5090-0639-7
ISBN (Online):	978-1-5090-0638-0
ISSN:	0743-1562

**Additional Copies of This Publication Are Available From:**

Curran Associates, Inc  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: (845) 758-0400  
Fax: (845) 758-2633  
E-mail: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

CURRAN ASSOCIATES INC.  
**proceedings**  
.com

## TABLE OF CONTENTS

<b>1.1 The Age of Sensors – How MEMS Sensors Will Enable the Next Wave of New Products.....</b>	<b>1</b>
<i>S. Lloyd, M. Lim</i>	
<b>1.2 Intelligent Mobility Realized through VLSI.....</b>	<b>5</b>
<i>T. Asami</i>	
<b>2.1 Si FinFET Based 10nm Technology with Multi Vt Gate Stack for Low Power and High Performance Applications.....</b>	<b>9</b>
<i>H.-J. Cho, H. S. Oh, K. J. Nam, Y. H. Kim, K. H. Yeo, W. D. Kim, Y. S. Chung, Y. S. Nam, S. M. Kim, W. H. Kwon, M. J. Kang, I. R. Kim, H. Fukutome, C. W. Jeong, H. J. Shin, Y. S. Kim, D. W. Kim, S. H. Park, H. S. Oh, J. H. Jeong, S. B. Kim, D. W. Ha, J. H. Park, H. S. Rhee, S. J. Hyun, D. S. Shin, D. H. Kim, H. Y. Kim, S. Maeda, K. H. Lee, Y. H. Kim, M. C. Kim, Y. S. Koh, B. Yoon, K. Shin, N. I. Lee, S. B. Kang, K. H. Hwang, J. H. Lee, J.-H. Ku, S. W. Nam, S. M. Jung, H. K. Kang, J. S. Yoon, E. S. Jung</i>	
<b>2.2 FINFET Technology Featuring High Mobility SiGe Channel for 10nm and Beyond.....</b>	<b>11</b>
<i>D. Guo, G. Karve, G. Tsutsui, K.-Y. Lim, R. Robison, T. Hook, R. Vega, D. Liu, S. Bedell, S. Mochizuki, F. Lie, K. Akarvardar, M. Wang, R. Bao, S. Burns, V. Chan, K. Cheng, J. Demarest, J. Fronheiser, P. Hashemi, J. Kelly, J. Li, N. Loubet, P. Montanini, B. Sahu, M. Sankarapandian, S. Sieg, J. Sporre, J. Strange, R. Southwick, N. Tripathi, R. Venigalla, J. Wang, K. Watanabe, C. W. Yeung, D. Gupta, B. Doris, N. Felix, A. Jacob, H. Jagannathan, S. Kanakasabapathy, R. Mo, V. Narayanan, D. Sadana, P. Oldiges, J. Stathis, T. Yamashita, V. Paruchuri, M. Colburn, A. Knorr, R. Divakaruni, H. Bu, M. Khare</i>	
<b>2.3 High Performance In<sub>0.53</sub>Ga<sub>0.47</sub>As FinFETs Fabricated on 300 mm Si Substrate.....</b>	<b>13</b>
<i>M. L. Huang, S. W. Chang, M. K. Chen, Y. Oniki, H. C. Chen, C. H. Lin, W. C. Lee, C. H. Lin, M. A. Khaderbad, K. Y. Lee, Z. C. Chen, P. Y. Tsai, L. T. Lin, M. H. Tsai, C. L. Hung, T. C. Huang, Y. C. Lin, Y.-C. Yeo, S. M. Jang, H. Y. Hwang, H. C.-H. Wang, C. H. Diaz</i>	
<b>2.4 Achieving Sub-ns switching of STT-MRAM for Future Embedded LLC Applications through Improvement of Nucleation and Propagation Switching Mechanisms .....</b>	<b>15</b>
<i>G. Jan, L. Thomas, S. Le, Y.-J. Lee, H. Liu, J. Zhu, J. Iwata-Harms, S. Patel, R.-Y. Tong, S. Serrano-Guisan, D. Shen, R. He, J. Haq, J. Teng, V. Lam, R. Annapragna, Y.-J. Wang, T. Zhong, T. Tornq, P.-K. Wang</i>	
<b>3.1 Memory in the Era of Innovative Architectures .....</b>	<b>17</b>
<i>D. Klein</i>	
<b>3.2 High-Density User-Programmable Logic Array Based on Adjacent Integration of Pure-CMOS Crossbar Antifuse into Logic CMOS Circuits.....</b>	<b>19</b>
<i>S. Yasuda, M. Oda, M. Matsumoto, K. Tatsumura, K. Zaitsu, Y.-H. Ho, M. Ono</i>	
<b>3.3 Advanced Non-Volatile Embedded Memory for a Wide Range of Applications.....</b>	<b>21</b>
<i>S. Kimura</i>	
<b>3.4 Random Soft Error Suppression by Stoichiometric Engineering: CMOS Compatible and Reliable 1Mb HfO<sub>2</sub>-ReRAM with 2 Extra Masks for Embedded IoT Systems .....</b>	<b>23</b>
<i>C. Ho, T. Y. Shen, P. Y. Hsu, S. C. Chang, S. Y. Wen, M. H. Lin, P. K. Wang, S. C. Liao, C. S. Chou, K. M. Peng, C. M. Wu, W. H. Chang, Y. H. Chen, F. Chen, L. W. Lin, T. H. Tsai, S. F. Lim, C. J. Yang, M. H. Shieh, H. H. Liao, C. H. Lin, P. L. Pai, T. Y. Chan, Y. C. Chiao</i>	
<b>4.1 Understanding Charge Traps for Optimizing Si-Passivated Ge nMOSFETs .....</b>	<b>25</b>
<i>P. Ren, R. Gao, Z. Ji, H. Arimura, J. F. Zhang, R. Wang, M. Duan, W. Zhang, J. Franco, S. Sioncke, D. Cott, J. Mitard, L. Witters, H. Mertens, B. Kaczer, A. Mocuta, N. Collaert, D. Linten, R. Huang, A. V.-Y. Thean, G. Groeseneken</i>	
<b>4.2 A 2nd Generation of 14/16nm-Node Compatible Strained-Ge pFINFET with Improved Performance with Respect to Advanced Si-Channel FinFETs .....</b>	<b>27</b>
<i>J. Mitard, L. Witters, Y. Sasaki, H. Arimura, A. Schulze, R. Loo, L.-å. Ragnarsson, A. Hikavyy, D. Cott, T. Chiarella, S. Kubicek, H. Mertens, R. Ritzenthaler, C. Vrancken, P. Favia, H. Bender, N. Horiguchi, K. Barla, D. Mocuta, A. Mocuta, N. Collaert, A. V.-Y. Thean</i>	
<b>4.3 Selective GeO<sub>x</sub>-Scavenging from Interfacial Layer on Si<sub>1-x</sub>Ge<sub>x</sub> Channel for High Mobility Si/Si<sub>1-x</sub>Ge<sub>x</sub> CMOS Application.....</b>	<b>29</b>
<i>C. H. Lee, H. Kim, P. Jamison, R. G. Southwick III, S. Mochizuki, K. Watanabe, R. Bao, R. Galatage, S. Guillaumet, T. Ando, R. Pandey, A. Konar, B. Lherron, J. Fronheiser, S. Siddiqui, H. Jagannathan, V. Paruchuri</i>	
<b>4.4 Demonstration of Record SiGe Transconductance and Short-Channel Current Drive in High-Ge-Content SiGe PMOS FinFETs with Improved Junction and Scaled EOT .....</b>	<b>31</b>
<i>P. Hashemi, K.-L. Lee, T. Ando, K. Balakrishnan, J. A. Ott, S. Koswatta, S. U. Engelmann, D.-G. Park, V. Narayanan, R. T. Mo, E. Leobandung</i>	

<b>5.1 Demonstration of an InGaAs Gate Stack with Sufficient PBTI Reliability by Thermal Budget Optimization, Nitridation, High-k Material Choice, and Interface Dipole.....</b>	33
J. Franco, A. Vais, S. Sioncke, V. Putcha, B. Kaczer, B.-S. Shie, X. Shi, R. Mahlouji, L. Nyns, D. Zhou, N. Waldron, J. W. Maes, Q. Xie, M. Givens, F. Tang, X. Jiang, H. Arimura, T. Schram, L.-å. Ragnarsson, A. S. Hernandez, G. Hellings, N. Horiguchi, M. Heyns, G. Groeseneken, D. Linten, N. Collaert, A. Thean	
<b>5.2 Application of CVS and VRS Method for Correlation of Logic CMOS Wear Out to Discrete Device Degradation Based on Ring Oscillator Circuits.....</b>	35
A. Kerber, T. Nigam	
<b>5.3 Deep Insight into Process-Induced Pre-Existing Traps and PBTI Stress-Induced Trap Generations in High-k Gate Dielectrics through Systematic RTN Characterizations and <i>Ab initio</i> Calculations .....</b>	37
J. Chen, Y. Nakasaki, Y. Mitani	
<b>5.4 Hot Carrier Degradation in Nanowire Transistors: Physical Mechanisms, Width Dependence and Impact of Self-Heating .....</b>	39
A. Laurent, X. Garros, S. Barraud, G. Marinello, G. Reimbold, D. Roy, E. Vincent, G. Ghibaudo	
<b>6.1 MoS<sub>2</sub> U-Shape MOSFET with 10 nm Channel Length and Poly-Si Source/Drain Serving as Seed for Full Wafer CVD MoS<sub>2</sub> Availability .....</b>	41
K.-S. Li, B.-W. Wu, L.-J. Li, M.-Y. Li, C.-C. K. Cheng, C.-L. Hsu, C.-H. Lin, Y.-J. Chen, C.-C. Chen, C.-T. Wu, M.-C. Chen, J.-M. Shieh, W.-K. Yeh, Y.-L. Chueh, F.-L. Yang, C. Hu	
<b>6.2 Serially Connected Monolayer MoS<sub>2</sub> FETs with Channel Patterned by a 7.5 nm Resolution Directed Self-Assembly Lithography .....</b>	43
A. Nourbakhsh, A. Zubair, A. Tavakkoli, R. Sajjad, X. Ling, M. Dresselhaus, J. Kong, K. K. Berggren, D. Antoniadis, T. Palacios	
<b>6.3 GDOT: A Graphene-Based Nanofunction for Dot-Product Computation .....</b>	45
N. C. Wang, S. K. Gonugondla, I. Nahlus, N. R. Shanbhag, E. Pop	
<b>6.4 Extremely Low Power C-Axis Aligned Crystalline In-Ga-Zn-O 60 nm Transistor Integrated with Industry 65 nm Si MOSFET for IoT Normally-Off CPU Application.....</b>	47
S. H. Wu, X. Y. Jia, M. Kui, C. C. Shuai, T. Y. Hsieh, H. C. Lin, D. Chen, C. B. Lin, J. Y. Wu, T. R. Yew, Y. Endo, K. Kato, S. Yamazaki	
<b>6.5 A Sub-ns Three-Terminal Spin-Orbit Torque Induced Switching Device.....</b>	49
S. Fukami, T. Anekawa, A. Ohkawara, C. Zhang, H. Ohno	
<b>6.6 Si CMOS Platform for Quantum Information Processing .....</b>	51
L. Hutin, R. Maurand, D. Kotekar-Patil, A. Corna, H. Bohuslavskyi, X. Jehl, S. Barraud, S. De Franceschi, M. Sanquer, M. Vinet	
<b>7.1 Ultralow-Resistivity CMOS Contact Scheme with Pre-Contact Amorphization Plus Ti (Germano-)Silicidation .....</b>	53
H. Yu, M. Schaekers, A. Hikavyy, E. Rosseel, A. Peter, K. Hollar, F. A. Khaja, W. Aderhold, L. Date, A. J. Mayur, J.-G. Lee, K. M. Shin, B. Douhard, S. A. Chew, S. Demuynick, S. Kubicek, D. Kim, A. Mocuta, K. Barla, N. Horiguchi, N. Collaert, A. V.-Y. Thean, K. De Meyer	
<b>7.2 Ti and NiPt/Ti Liner Silicide Contacts for Advanced Technologies .....</b>	55
P. Adusumilli, E. Alptekin, M. Raymond, N. Breil, F. Chafik, C. Lavoie, D. Ferrer, S. Jain, V. Kamineni, A. Ozcan, S. Allen, J. J. An, V. Basker, R. Bolam, H. Bu, J. Cai, J. Demarest, B. Doris, E. Engbrecht, S. Fan, J. Fronheiser, O. Gluschenkov, D. Guo, B. Haran, D. Hilscher, H. Jagannathan, D. Kang, Y. Ke, J. Kim, S. Koswatta, A. Kumar, A. Labonte, R. Lallement, W. Lee, Y. Lee, J. Li, C.-H. Lin, B. Liu, Z. Liu, N. Loubet, N. Makela, S. Mochizuki, B. Morgenfeld, S. Narasimha, T. Nesheiwat, H. Niimi, C. Niu, M. Oh, C. Park, R. Ramachandran, J. Rice, V. Sardesai, J. Shearer, C. Sheraw, C. Tran, G. Tsutsui, H. Utomo, K. Wong, R. Xie, T. Yamashita, Y. Yan, C. Yeh, M. Yu, N. Zamdmer, N. Zhan, B. Zhang, V. Paruchuri, C. Goldberg, W. Kleemeier, S. Stiffler, R. Divakaruni, W. Henson	
<b>7.3 Ultra-Low NMOS Contact Resistivity Using a Novel Plasma-Based DSS Implant and Laser Anneal for Post 7 nm Nodes.....</b>	57
C.-N. Ni, K. V. Rao, F. Khaja, S. Sharma, S. Tang, J. J. Chen, K. E. Hollar, N. Breil, X. Li, M. Jin, C. Lazik, J. Lee, H. Maynard, N. Variam, A. J. Mayur, S. Kim, H. Chung, M. Chudzik, R. Hung, N. Yoshida, N. Kim	
<b>7.5 Ultra Low p-Type SiGe Contact Resistance FinFETs with Ti Silicide Liner Using Cryogenic Contact Implantation Amorphization and Solid-Phase Epitaxial Regrowth (SPER) .....</b>	59
Y. R. Yang, N. Breil, C. Y. Yang, J. Hsieh, F. Chiang, B. Colombeau, B. N. Guo, K. H. Shim, N. Variam, G. Leung, J. Hebb, S. Sharma, C. N. Ni, J. Ren, J. Wen, J. H. Park, H. Chen, S. Chen, M. Hou, D. Tsai, J. Kuo, D. Liao, M. Chudzik, S. H. Lin, H. F. Huang, N. H. Yang, J. F. Lin, C. T. Tsai, G. C. Hung, S. C. Hsu, O. Cheng, J. Y. Wu, T. R. Yew	
<b>8.1 Comprehensive Evaluation of Early Retention (Fast Charge Loss within a Few Seconds) Characteristics in Tube-Type 3-D NAND Flash Memory .....</b>	61
B. Choi, S. H. Jang, J. Yoon, J. Lee, M. Jeon, Y. Lee, J. Han, J. Lee, D. M. Kim, D. H. Kim, C. Lim, S. Park, S.-J. Choi	
<b>8.2 A Monte Carlo Simulation Method to Predict Large-Density NAND Product Memory Window from Small-Array Test Element Group (TEG) Verified on a 3D NAND Flash Test Chip .....</b>	63
C.-C. Hsieh, H.-T. Lue, T.-H. Hsu, P.-Y. Du, K.-H. Chiang, C.-Y. Lu	

<b>8.3 Advanced a-VMCO Resistive Switching Memory through Inner Interface Engineering with Wide (<math>&gt;10^2</math>) on/off window, Tunable <math>\mu</math>A-Range Switching Current and Excellent Variability .....</b>	65
<i>B. Govoreanu, L. Di Piazza, J. Ma, T. Conard, A. Vanleenhove, A. Belmonte, D. Radisic, M. Popovici, A. Velea, A. Redolfi, O. Richard, S. Clima, C. Adelmann, H. Bender, M. Jurczak</i>	
<b>8.4 Fully CMOS Compatible 3D Vertical RRAM with Self-Aligned Self-Selective Cell Enabling Sub-5nm Scaling .....</b>	67
<i>X. Xu, Q. Luo, T. Gong, H. Lv, S. Long, Q. Liu, S. S. Chung, J. Li, M. Liu</i>	
<b>8.5 Te-Based Amorphous Binary OTS Device with Excellent Selector Characteristics for X-Point Memory Applications .....</b>	69
<i>Y. Koo, K. Baek, H. Hwang</i>	
<b>9.1 Demonstration of a Sub-0.03 <math>\mu</math>m<sup>2</sup> High Density 6-T SRAM with Scaled Bulk FinFETs for Mobile SOC Applications Beyond 10nm Node.....</b>	71
<i>S.-Y. Wu, C. Y. Lin, M. C. Chiang, J. J. Liaw, J. Y. Cheng, C. H. Chang, V. S. Chang, K. H. Pan, C. H. Tsai, C. H. Yao, T. Miyashita, Y. K. Wu, K. C. Ting, C. H. Hsieh, R. F. Tsui, R. Chen, C. L. Yang, H. C. Chang, C. Y. Lee, K. S. Chen, Y. Ku, S. M. Jang</i>	
<b>9.2 First Demonstration of InGaAs/SiGe CMOS Inverters and Dense SRAM Arrays on Si Using Selective Epitaxy and Standard FEOL Processes .....</b>	73
<i>L. Czornomaz, V. Djara, V. Deshpande, E. O'Connor, M. Sousa, D. Caimi, K. Cheng, J. Fompeyrine</i>	
<b>9.3 Replacement High-K/Metal-Gate High-Ge-Content Strained SiGe FinFETs with High Hole Mobility and Excellent SS and Reliability at Aggressive EOT ~7Å and Scaled Dimensions Down to Sub-4nm Fin Widths.....</b>	75
<i>P. Hashemi, T. Ando, K. Balakrishnan, E. Cartier, M. Lofaro, J. A. Ott, J. Bruley, K.-L. Lee, S. Koswatta, S. Dawes, J. Rozen, A. Pyzyna, K. Chan, S. U. Engelmann, D.-G. Park, V. Narayanan, R. T. Mo, E. Leobandung</i>	
<b>9.4 Zero-Thickness Multi Work Function Solutions for N7 Bulk FinFETs.....</b>	77
<i>L.-å. Ragnarsson, H. Dekkers, P. Matagne, T. Schram, T. Conard, N. Horiguchi, A. V.-Y. Thean</i>	
<b>10.1 Smart Power Technologies Enabling Power SOC and SIP (Invited) .....</b>	79
<i>S. Pendharkar</i>	
<b>10.2 A Dynamic/Static SRAM Power Management Scheme for DVFS and AVS in Advanced Automotive Infotainment SoCs (Invited).....</b>	81
<i>K. Nii, M. Yabuuchi, Y. Ishii, M. Tanaka, M. Igarashi, K. Fukuoka, S. Tanaka</i>	
<b>10.3 A Multiple-String Hybrid LED Driver with 97% Power Efficiency and 0.996 Power Factor .....</b>	83
<i>L. Li, Y. Gao, P. K. T. Mok</i>	
<b>10.4 A Sine-Reference Band (SRB)-Controlled Average Current Technique for a Phase-Cut Dimmable AC-DC Buck LED Driver without an Electrolytic Capacitor .....</b>	85
<i>C. Shin, W. Lee, S.-W. Lee, B. Jeong, J. Lee, U. Jang, Y.-G. Kim, S.-H. Lee, J.-S. Bang, G.-H. Cho</i>	
<b>11.1 Overcoming Scaling Barriers through Design Technology CoOptimization (Invited) .....</b>	87
<i>L. Liebmann, J. Zeng, X. Zhu, L. Yuan, G. Bouche, J. Kye</i>	
<b>11.2 Analog/RF Wonderland: Circuit and Technology Co-Optimization in Advanced FinFET Technology (Invited).....</b>	89
<i>F.-L. Hsueh, Y.-C. Peng, C.-H. Chen, T.-J. Yeh, H.-H. Hsieh, C.-H. Chang, S.-L. Liu, M.-C. Chuang, M. Chen</i>	
<b>11.3 200-280GHz CMOS RF Front-End of Transmitter for Rotational Spectroscopy.....</b>	91
<i>N. Sharma, Q. Zhong, Z. Chen, W. Choi, J. P. McMillan, C. F. Neese, R. Schueler, I. Medvedev, F. De Lucia, K. O</i>	
<b>11.4 Broadband THz Spectroscopic Imaging Based on a Fully-Integrated 4x2 Digital-to-Impulse Radiating Array with a Full-Spectrum of 0.03-1.03THz in Silicon .....</b>	93
<i>M. M. Assefzadeh, A. Babakhani</i>	
<b>12.1 RTN-Based Defect Tracking Technique: Experimentally Probing the Spatial and Energy Profile of the Critical Filament Region and its Correlation with HfO<sub>2</sub> RRAM Switching Operation and Failure Mechanism .....</b>	95
<i>Z. Chai, J. Ma, W. Zhang, B. Govoreanu, E. Simoen, J. F. Zhang, Z. Ji, R. Gao, G. Groeseneken, M. Jurczak</i>	
<b>12.2 Robust Cu Atom Switch with over-400°C Thermally Tolerant Polymer-Solid Electrolyte (TT-PSE) for Nonvolatile Programmable Logic .....</b>	97
<i>K. Okamoto, M. Tada, N. Banno, N. Iguchi, H. Hada, T. Sakamoto, M. Miyamura, Y. Tsuji, R. Nebashi, A. Morioka, X. Bai, T. Sugibayashi</i>	
<b>12.3 Retention, Disturb and Variability Improvements Enabled by Local Chemical-Potential Tuning and Controlled Hour-Glass Filament Shape in a Novel W WO<sub>3</sub> Al<sub>2</sub>O<sub>3</sub> Cu CBRAM .....</b>	99
<i>L. Goux, A. Belmonte, U. Celano, J. Woo, S. Folkersma, C. Y. Chen, A. Redolfi, A. Fantini, R. Degraeve, S. Clima, W. Vandervorst, M. Jurczak</i>	
<b>12.4 A Novel Low Power Phase Change Memory Using Inter-Granular Switching .....</b>	101
<i>H. L. Lung, Y. H. Ho, Y. Zhu, W. C. Chien, S. Kim, W. Kim, H. Y. Cheng, A. Ray, M. Brightsky, R. Bruce, C. W. Yeh, C. Lam</i>	

<b>13.1 Smart Solutions for Efficient Dual Strain Integration for Future FDSOI Generations .....</b>	103
A. Bonneville, C. Le Royer, Y. Morand, S. Reboh, C. Plantier, N. Rambal, J.-P. Pédini, S. Kerdiles, P. Besson, J.-M. Hartmann, D. Marseilhan, B. Mathieu, R. Berthelon, M. Cassé, F. Andrieu, D. Rouchon, O. Weber, F. Boeuf, M. Haond, A. Claverie, M. Vinet	
<b>13.2 High Performance CMOS FDSOI Devices Activated at Low Temperature.....</b>	105
L. Pasini, P. Batude, J. Lacord, M. Casse, B. Mathieu, B. Sklenard, F. P. Luce, J. Micout, A. Payet, F. Mazen, P. Besson, E. Gheglin, J. Borrel, R. Daubriac, L. Hulin, D. Blachier, D. Barge, S. Chhun, V. Mazzocchi, A. Cros, J.-P. Barnes, Z. Saghi, V. Delaye, N. Rambal, V. Lapras, J. Mazurier, O. Weber, F. Andrieu, L. Brunet, C. Fenouillet-Beranger, Q. Rafhay, G. Ghibaudo, F. Cristiano, M. Haond, F. Boeuf, M. Vinet	
<b>13.3 High Aspect Ratio InGaAs FinFETs with Sub-20 nm Fin Width.....</b>	107
A. Vardi, J. Lin, W. Lu, X. Zhao, J. A. Del Alamo	
<b>13.4 Junctionless Gate-All-Around Lateral and Vertical Nanowire FETs with Simplified Processing for Advanced Logic and Analog/RF Applications and Scaled SRAM Cells .....</b>	109
A. Veloso, B. Parvais, P. Matagne, E. Simoen, T. Huynh-Bao, V. Paraschiv, E. Vecchio, K. Devriendt, E. Rosseel, M. Ercken, B. T. Chan, C. Delvaux, E. Altamirano-Sánchez, J. J. Versluijs, Z. Tao, S. Suhard, S. Brus, A. Sibaja-Hernandez, N. Waldron, P. Lagrain, O. Richard, H. Bender, A. Chasin, B. Kaczer, T. Ivanov, S. Ramesh, K. De Meyer, J. Ryckaert, N. Collaert, A. Thean	
<b>13.5 Record Mobility (<math>\mu_{eff}</math> ~3100 cm<sup>2</sup>/V·s) and Reliability Performance (V<sub>ov</sub>~0.5V for 10yr Operation) of In<sub>0.53</sub>Ga<sub>0.47</sub>As MOS Devices Using Improved Surface Preparation and a Novel Interfacial Layer .....</b>	111
A. Vais, A. Alian, L. Nyns, J. Franco, S. Sioncke, V. Putcha, H. Yu, Y. Mols, R. Rooyackers, D. Lin, J. W. Maes, Q. Xie, M. Givens, F. Tang, X. Jiang, A. Mocuta, N. Collaert, K. De Meyer, A. Thean	
<b>14.1 Reliability Study of Perpendicular STT-MRAM As Emerging Embedded Memory Qualified for Reflow Soldering at 260°C .....</b>	113
M.-C. Shih, C.-Y. Wang, Y.-H. Lee, W. Wang, L. Thomas, H. Liu, J. Zhu, Y.-J. Lee, G. Jan, Y.-J. Wang, T. Zhong, T. Tornig, P.-K. Wang, D. Lin, T.-W. Chiang, K.-H. Shen, H. Chuang, W. J. Gallagher	
<b>14.2 Sub-3 ns Pulse with sub-100 μA Switching of 1x-2x nm Perpendicular MTJ for High-Performance Embedded STT-MRAM Towards Sub-20 nm CMOS .....</b>	115
D. Saida, S. Kashiwada, M. Yakabe, T. Daibou, N. Hase, M. Fukumoto, S. Miwa, Y. Suzuki, H. Noguchi, S. Fujita, J. Ito	
<b>14.3 First Demonstration and Performance Improvement of Ferroelectric HfO<sub>2</sub>-Based Resistive Switch with Low Operation Current and Intrinsic Diode Property.....</b>	117
S. Fujii, Y. Kamimuta, T. Ino, Y. Nakasaki, R. Takaishi, M. Saitoh	
<b>14.4 One-Transistor Ferroelectric Versatile Memory: Strained-Gate Engineering for Realizing Energy-Efficient Switching and Fast Negative-Capacitance Operation .....</b>	119
Y.-C. Chiu, C.-H. Cheng, C.-Y. Chang, Y.-T. Tang, M.-C. Chen	
<b>14.5 Study of Wake-Up and Fatigue Properties in Doped and Undoped Ferroelectric HfO<sub>2</sub> in Conjunction with Piezo-Response Force Microscopy Analysis.....</b>	121
S. Shibayama, L. Xu, S. Migita, A. Toriumi	
<b>15.1 Gate-All-Around MOSFETs Based on Vertically Stacked Horizontal Si Nanowires in a Replacement Metal Gate Process on Bulk Si Substrates.....</b>	123
H. Mertens, R. Ritzenhaller, A. Hikavyy, M. S. Kim, Z. Tao, K. Wostyn, S. A. Chew, A. De Keersgieter, G. Mannaert, E. Rosseel, T. Schram, K. Devriendt, D. Tsvetanova, H. Dekkers, S. Demuyncck, A. Chasin, E. Van Besien, A. Dangol, S. Godny, B. Douhard, N. Bosman, O. Richard, J. Geypen, H. Bender, K. Barla, D. Mocuta, N. Horiguchi, A. V.-Y. Thean	
<b>15.2 InAs Nanowire GAA n-MOSFETs with 12-15 nm Diameter .....</b>	125
T. Vasen, P. Ramvall, A. Afzalian, C. Thelander, K. A. Dick, M. Holland, G. Doornbos, S. W. Wang, R. Oxland, G. Vellianitis, M. J. H. Van Dal, B. Duriez, J.-R. Ramirez, R. Droopad, L.-E. Wernersson, L. Samuelson, T.-K. Chen, Y.-C. Yeo, M. Passlack	
<b>15.3 InGaAs Nanowire MOSFETs with ION = 555 μA/μm at IOFF = 100 nA/μm and V<sub>DD</sub> = 0.5 V .....</b>	127
C. B. Zota, F. Lindelöw, L.-E. Wernersson, E. Lind	
<b>15.4 Top-Down InGaAs Nanowire and Fin Vertical FETs with Record Performance .....</b>	129
S. Ramesh, T. Ivanov, E. Camerotto, N. Sun, J. Franco, A. Sibaja-Hernandez, R. Rooyackers, A. Alian, J. Loo, A. Veloso, A. Milenin, D. Lin, P. Favia, H. Bender, N. Collaert, A. V.-Y. Thean, K. De Meyer	
<b>15.5 Scalability of InGaAs Gate-All-Around FET Integrated on 300mm Si platform: Demonstration of Channel Width Down to 7nm and L<sub>g</sub> Down to 36nm .....</b>	131
X. Zhou, N. Waldron, G. Boccardi, F. Sebaai, C. Merckling, G. Eneman, S. Sioncke, L. Nyns, A. Opdebeeck, J. W. Maes, Q. Xie, M. Givens, F. Tang, X. Jiang, W. Guo, B. Kunert, L. Teugels, K. Devriendt, A. S. Hernandez, J. Franco, D. Van Dorp, K. Barla, N. Collaert, A. V.-Y. Thean	
<b>16.1 RTN and Low Frequency Noise on Ultra-Scaled Near-Ballistic Ge Nanowire nMOSFETs .....</b>	133
W. Wu, H. Wu, M. Si, N. Conrad, Y. Zhao, P. D. Ye	
<b>16.2 Statistical Limits of Contact Resistivity Due to Atomistic Variation in Nanoscale Contacts .....</b>	135
G. Shine, C. E. Weber, K. C. Saraswat	

<b>16.3 Variability-Aware TCAD Based Design-Technology Co-Optimization Platform for 7nm Node Nanowire and Beyond .....</b>	137
Y. Wang, B. Cheng, X. Wang, E. Towie, C. Riddet, A. R. Brown, S. M. Amoroso, L. Wang, D. Reid, X. Liu, J. Kang, A. Asenov	
<b>16.4 Random Telegraph Noise (RTN) in 14nm Logic Technology: High Volume Data Extraction and Analysis.....</b>	139
S. Dongaonkar, M. D. Giles, A. Kornfeld, B. Grossnickle, J. Yoon	
<b>16.5 Design / Technology Co-Optimization of Strain-Induced Layout Effects in 14nm UTBB-FDSOI CMOS: Enablement and Assessment of Continuous-RX Designs .....</b>	141
R. Berthelon, F. Andrieu, E. Josse, R. Bingert, O. Weber, E. Serret, A. Aurand, S. Delmedico, V. Farys, C. Bernicot, E. Bechet, E. Bernard, T. Poiroux, D. Rideau, P. Scheer, E. Baylac, P. Perreau, M. A. Jaud, J. Lacord, E. Petitprez, A. Pofelski, S. Ortolland, P. Sardin, D. Dutartre, A. Claverie, M. Vinet, J. C. Marin, M. Haond	
<b>17.1 On-Chip Interconnect Trends, Challenges and Solutions: How to Keep RC and Reliability Under Control (Invited) .....</b>	143
Z. Tokei, I. Ciofi, P. Roussel, P. Debacker, P. Raghavan, M. H. Van Der Veen, N. Jourdan, C. J. Wilson, V. V. Gonzalez, C. Adelmann, L. Wen, K. Croes, O. V. P. K. Moors, M. Krishtab, S. Armini, J. Bömmels	
<b>17.2 Production-Worthy WOW 3D Integration Technology Using Bumpless Interconnects and Ultra-Thinning Processes (Invited).....</b>	145
T. Ohba	
<b>17.3 First Demonstration of a CMOS over CMOS 3D VLSI CoolCube<sup>TM</sup> Integration on 300mm Wafers.....</b>	147
L. Brunet, P. Batude, C. Fenouillet-Beranger, P. Besombes, L. Hortemel, F. Ponthenier, B. Previtali, C. Tabone, A. Royer, C. Agrafieil, C. Euvrard-Colnat, A. Seignard, C. Morales, F. Fournel, L. Benissa, T. Signamarcheix, P. Besson, M. Jourdan, R. Kachtouli, V. Benevent, J.-M. Hartmann, C. Comboroure, N. Allouti, N. Posseme, C. Vizioz, C. Arvet, S. Barnola, S. Kerdiles, L. Baud, L. Pasini, C.-M. V. Lu, F. Deprat, A. Toffoli, G. Romano, C. Guedj, V. Delaye, F. Boeuf, O. Faynot, M. Vinet	
<b>17.4 A Highly Scalable Poly-Si Junctionless FETs Featuring a Novel Multi-Stacking Hybrid P/N Layer and Vertical Gate with Very High Ion/Ioff for 3D Stacked ICs.....</b>	149
Y.-C. Cheng, H.-B. Chen, C.-Y. Chang, C.-H. Cheng, Y.-J. Shih, Y.-C. Wu	
<b>18.1 Direct Three-Dimensional Observation of the Conduction in Poly-Si and In<sub>1-x</sub>Ga<sub>x</sub>As 3D NAND Vertical Channels .....</b>	151
U. Celano, E. Capogreco, J. G. Lisoni, A. Arreghini, B. Kunert, W. Guo, G. Van Den Bosch, J. Van Houdt, K. De Meyer, A. Furnemont, W. Vandervorst	
<b>18.2 Four-Layer 3D Vertical RRAM Integrated with FinFET as a Versatile Computing Unit for Brain-Inspired Cognitive Information Processing.....</b>	153
H. Li, K.-S. Li, C.-H. Lin, J.-L. Hsu, W.-C. Chiu, M.-C. Chen, T.-T. Wu, J. Sohn, S. B. Eryilmaz, J.-M. Shieh, W.-K. Yeh, H.-S. P. Wong	
<b>18.3 Novel RRAM-Enabled 1T1R Synapse Capable of Low-Power STDP via Burst-Mode Communication and Real-Time Unsupervised Machine Learning .....</b>	155
S. Ambrogio, S. Balatti, V. Milo, R. Carboni, Z. Wang, A. Calderoni, N. Ramaswamy, D. Ielmini	
<b>18.4 A ReRAM-Based Physically Unclonable Function with Bit Error Rate &lt; 0.5% after 10 Years at 125°C for 40nm Embedded Application .....</b>	157
Y. Yoshimoto, Y. Katoh, S. Ogasahara, Z. Wei, K. Kouno	
<b>19.1 Gate Stack Solutions in Gate-First FDSOI Technology to meet High Performance, Low Leakage, VT Centering and Reliability Criteria .....</b>	159
O. Weber, E. Josse, X. Garros, M. Rafik, X. Federspiel, C. Diouf, A. Toffoli, S. Zoll, O. Gourhant, V. Joseph, C. Suarez-Segovia, F. Domengie, V. Beugin, B. Saidi, M. Gros-Jean, P. Perreau, J. Mazurier, E. Richard, M. Haond	
<b>19.2 A New Variation Plot to Examine the Interfacial-Dipole Induced Work-Function Variation in Advanced High-k Metal-Gate CMOS Devices .....</b>	161
E. R. Hsieh, Y. D. Wang, S. S. Chung, J. C. Ke, C. W. Yang, S. Hsu	
<b>19.3 Novel N/PFET Vt Control by TiN Plasma Nitridation for Aggressive Gate Scaling.....</b>	163
M. Togo, W. H. Tong, X. Zhang, D. H. Triyoso, J. Lian, Y. M. Randriamihja, S. Uppal, S. Dag, E. C. Silva, M. Kota, T. Shimizu, S. Patil, M. Eller, S. Samavedam	
<b>19.4 Complete Extraction of Defect Bands Responsible for Instabilities in n and pFinFETs .....</b>	165
G. Rzepa, M. Waltl, W. Goes, B. Kaczer, J. Franco, T. Chiarella, N. Horiguchi, T. Grasser	
<b>20.1 Low-Power, High-Performance S-NDR Oscillators for Stereo (3D) Vision Using Directly-Coupled Oscillator Networks.....</b>	167
A. A. Sharma, Y. Kesim, M. Shulaker, C. Kuo, C. Augustine, H. S.-P. Wong, S. Mitra, M. Skowronski, J. A. Bain, J. A. Weldon	
<b>20.2 Ultra Low Power Coupled Oscillator Arrays for Computer Vision Applications.....</b>	169
N. Shukla, W.-Y. Tsai, M. Jerry, M. Barth, V. Narayanan, S. Datta	
<b>20.3 A 512×576 65-nm CMOS ISFET Sensor for Food Safety Screening with 123.8 mV/pH Sensitivity and 0.01 pH Resolution .....</b>	171
Y. Jiang, X. Liu, T. C. Dang, M. Yan, H. Yu, J.-C. Huang, C.-H. Hsieh, T.-T. Chen	

<b>20.4 Integration of Neural Sensing Microsystem with TSV-Embedded Dissolvable μ-Needles Array, Biocompatible Flexible Interposer, and Neural Recording Circuits .....</b>	173
<i>Y.-C. Huang, Y.-C. Hu, P.-T. Huang, S.-L. Wu, Y.-H. You, J.-M. Chen, Y.-Y. Huang, H.-C. Chang, Y.-H. Lin, J.-R. Duann, T.-W. Chiu, W. Hwang, C.-T. Chuang, J.-C. Chiou, K.-N. Chen</i>	
<b>21.1 Enabling High-Performance Heterogeneous TFET/CMOS Logic with Novel Circuits Using TFET Unidirectionality and Low-VDD Operation .....</b>	175
<i>D. H. Morris, K. Vaidyanathan, U. E. Avci, H. Liu, T. Karnik, I. A. Young</i>	
<b>21.2 Performance Improvement of In<sub>x</sub>Ga<sub>1-x</sub>As Tunnel FETs with Quantum Well and EOT Scaling .....</b>	177
<i>D. H. Ahn, S. M. Ji, M. Takenaka, S. Takagi</i>	
<b>21.3 Complementary III-V Heterojunction Lateral NW Tunnel FET Technology on Si .....</b>	179
<i>D. Cutaia, K. E. Moselund, H. Schmid, M. Borg, A. Olziersky, H. Riel</i>	
<b>21.4 Phase-Transition-FET Exhibiting Steep Switching Slope of 8mV/Decade and 36% Enhanced ON Current .....</b>	181
<i>J. Frougier, N. Shukla, D. Deng, M. Jerry, A. Aziz, L. Liu, G. Lavallee, T. S. Mayer, S. Gupta, S. Datta</i>	
<b>21.5 Circuit Performance Analysis of Negative Capacitance FinFETs .....</b>	183
<i>S. Khandelwal, A. I. Khan, J. P. Duarte, A. B. Sachid, S. Salahuddin, C. Hu</i>	
<b>22.1 White Spots Reduction by Ultimate Proximity Metal Gettering at Carbon Complexes Formed underneath Contact Area in CMOS Image Sensors .....</b>	185
<i>T. Yamaguchi, T. Yamashita, T. Kamino, Y. Goto, T. Kuroi, M. Matsuura</i>	
<b>22.2 Enabling Monolithic 3D Image Sensor Using Large-Area Monolayer Transition Metal Dichalcogenide and Logic/Memory Hybrid 3D<sup>+</sup>IC .....</b>	187
<i>C.-C. Yang, K.-C. Chiu, C.-T. Chou, C.-N. Liao, M.-H. Chuang, T.-Y. Hsieh, W.-H. Huang, C.-H. Shen, J.-M. Shieh, W.-K. Yeh, Y.-H. Chen, M.-C. Wu, Y.-H. Lee</i>	
<b>22.3 Germanium-Tin Heterojunction Phototransistor: Towards High-Efficiency Low-Power Photodetection in Short-Wave Infrared Range .....</b>	189
<i>W. Wang, Y. Dong, S. Y. Lee, W. K. Loke, X. Gong, S.-F. Yoon, G. Liang, Y.-C. Yeo</i>	
<b>22.4 Novel Pixel Structure with Stacked Deep Photodiode to Achieve High NIR Sensitivity and High MTF .....</b>	191
<i>H. Takahashi, H. Tanaka, M. Oda, M. Ando, N. Niisoe, S. Kawai, T. Asano, M. Sudo, M. Yoshita, T. Yamada</i>	
<b>22.5 Back-Illuminated Voltage-Domain Global Shutter CMOS Image Sensor with 3.75μm Pixels and Dual in-Pixel Storage Nodes .....</b>	193
<i>L. Stark, J. M. Raynor, F. Lalanne, R. K. Henderson</i>	
<b>Author Index</b>	