

2016 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2016)

**Storrs, Connecticut, USA
19 – 20 September 2016**



**IEEE Catalog Number: CFP16078-POD
ISBN: 978-1-5090-3624-0**

**Copyright © 2016 by the Institute of Electrical and Electronics Engineers, Inc
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

******This publication is a representation of what appears in the IEEE Digital Libraries. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP16078-POD
ISBN (Print-On-Demand):	978-1-5090-3624-0
ISBN (Online):	978-1-5090-3623-3
ISSN:	1550-5774

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

Table of Contents

Session 1: Aging

BTI Aware Thermal Management for Reliable DVFS Designs	1
<i>Hardeep Chahal, Vasileios Tenentes, Daniele Rossi, and Bashir M. Al-Hashimi</i>	
Prognosis of NBTI Aging Using a Machine Learning Scheme	7
<i>Naghmeh Karimi and Ke Huang</i>	
Experimental Study and Analysis of Soft and Permanent Errors in Digital Cameras	11
<i>Glenn H. Chapman, Rahul Thomas, Rohan Thomas, Israel Koren, and Zahava Koren</i>	

Session 2: Fault Tolerance in Latches & Approximate Computing

A Highly Robust Double Node Upset Tolerant Latch	15
<i>Adam Watkins and Spyros Tragouodas</i>	
Applying Efficient Fault Tolerance to Enable the Preconditioned Conjugate Gradient Solver on Approximate Computing Hardware.....	21
<i>Alexander Scholl, Claus Braun, and Hans-Joachim Wunderlich</i>	
Construction of a Soft Error (SEU) Hardened Latch with High Critical Charge	27
<i>Hiroki Ueno and Kazuteru Namba</i>	
Design and Analysis of an Approximate 2D Convolver	31
<i>Ke Chen, Fabrizio Lombardi, and Jie Han</i>	

Session 3: System-level Approaches

Combined On-line Lifetime-Energy Optimization for Asymmetric Multicores	35
<i>Cristiana Bolchini, Matteo Carminati, Tulika Mitra, and Thannirmalai Somu Muthukaruppan</i>	
Effects of Online Fault Detection Mechanisms on Probabilistic Timing Analysis.....	41
<i>Chao Chen, Jacopo Panerati, and Giovanni Beltrame</i>	
Bounding Error Detection Latency in Safety Critical Systems with Enhanced Execution Fingerprinting	47
<i>Mojing Liu and Brett H. Meyer</i>	

Guiding Genetic Algorithms Using Importance Measures for Reliable Design of Embedded Systems	53
<i>Hananeh Aliee, Stefan Vitzethum, Michael Glab, Jurgen Teich, and Emanuele Borgonovo</i>	
Session 4: Special Session on Fault-tolerant Realtime Systems	
Fault-Tolerant Scheduling of Multicore Mixed-Criticality Systems under Permanent Failures.....	57
<i>Zaid Al-bayati, Brett H. Meyer, and Haibo Zeng</i>	
Cross-Layer Fault-Tolerant Design of Real-Time Systems	63
<i>Siva Satyendra Sahoo, Bharadwaj Veeravalli, and Akash Kumar</i>	
Fault-Aware Sensitivity Analysis for Probabilistic Real-Time Systems.....	69
<i>Luca Santinelli, Zhishan Guo, and Laurent George</i>	
Session 5: FPGA & CMOS Technologies	
Low Cost Resilient Regular Expression Matching on FPGAs.....	75
<i>Marcos T. Leipnitz, Eduardo Nunes de Souza, and Gabriel L. Nazar</i>	
In-Place LUT Polarity Inversion to Mitigate Soft Errors for FPGAs	81
<i>Juexiao Su, Ju-Yueh Lee, Chang Wu, and Lei He</i>	
Detecting Intermittent Resistive Faults in Digital CMOS Circuits.....	87
<i>Hassan Ebrahimi, Alireza Rohani, and Hans G. Kerkhoff</i>	
Soft Error Vulnerability Assessment of the Real-Time Safety-Related ARM Cortex-R5 CPU.....	91
<i>Xabier Iturbe, Balaji Venu, and Emre Ozer</i>	
Session 6: Architecture-level Techniques	
Efficient Utilization of Hierarchical iJTAG Networks for Interrupts Management	97
<i>Ahmed Ibrahim and Hans G. Kerkhoff</i>	
Error Recovery through Partial Value Similarity	103
<i>Abdulaziz Eker and Oguz Ergin</i>	
In-Field Functional Test Programs Development Flow for Embedded FPUs.....	107
<i>R. Cantoro, D. Piumatti, P. Bernardi, S. De Luca, and A. Sansonetti</i>	

Design and Characterization of a High-Safety Hardware/Software Module for the Acquisition of Eurobalise Telegrams.....	111
<i>Filippo Giuliani , Marco Ottavi , Gian Carlo Cardarilli, Marco Re, Luca Di Nunzio, Rocco Fazzolari, Antimo Bruno, and Francesco Zuliani</i>	
Session 7: Fault Tolerance in NoC & SoC	
CoBRA: Low Cost Compensation of TSV Failures in 3D-NoC	115
<i>Ronak Salamat, Masoumeh Ebrahimi, Nader Bagherzadeh, and Freek Verbeek</i>	
A New Approach to Deadlock-Free Fully Adaptive Routing for High-Performance Fault-Tolerant NoCs	121
<i>Amir Charif, Nacer-Eddine Zergainoh, and Michael Nicolaidis</i>	
An Adaptive Routing Algorithm to Improve Lifetime Reliability in NoCs Architecture	127
<i>Juman Alshraiedeh and Avinash Kodi</i>	
A Novel Method for SEE Validation of Complex SoCs Using Low-Energy Proton Beams	131
<i>Gianluca Furano, Stefano Di Mascio, Tomasz Szewczyk, Alessandra Menicucci, Luigi Campajola, Francesco Di Capua, Andrea Fabbri, and Marco Ottavi</i>	
Session 8: Special Session on the use of VLSI Techniques for Securing ICs against Attacks	
Reliable PUF Design Using Failure Patterns from Time-Controlled Power Gating	135
<i>Xiaolin Xu and Daniel E. Holcomb</i>	
Side Channel Attacks on STTRAM and Low- Overhead Countermeasures	141
<i>Anirudh Iyengar, Swaroop Ghosh, Nitin Rathi, and Helia Naeimi</i>	
On Meta-Obfuscation of Physical Layouts to Conceal Design Characteristics	147
<i>Vinay C. Patil, Arunkumar Vijayakumar, and Sandip Kundu</i>	
Can Flexible, Domain Specific Programmable Logic Prevent IP Theft?	153
<i>Xiaotong Cui, Kaijie Wu, Siddharth Garg, and Ramesh Karri</i>	
Author Index	158