

# **2016 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2016)**

**Jeju, South Korea  
25-28 October 2016**



**IEEE Catalog Number: CFP16APC-POD  
ISBN: 978-1-5090-1571-9**

**Copyright © 2016 by the Institute of Electrical and Electronics Engineers, Inc  
All Rights Reserved**

*Copyright and Reprint Permissions:* Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

***\*\*\*This publication is a representation of what appears in the IEEE Digital Libraries. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP16APC-POD
ISBN (Print-On-Demand):	978-1-5090-1571-9
ISBN (Online):	978-1-5090-1570-2

**Additional Copies of This Publication Are Available From:**

Curran Associates, Inc  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: (845) 758-0400  
Fax: (845) 758-2633  
E-mail: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

CURRAN ASSOCIATES INC.  
**proceedings**  
.com

# TABLE OF CONTENTS

<b>IMAGE ENHANCEMENT USING DCT-BASED MATRIX HOMOMORPHIC FILTERING METHOD</b> .....	1
<i>Su-Ling Lee ; Chien-Cheng Tseng</i>	
<b>OPTIMIZED THREE SCORES COMBINATION FOR IMAGE QUALITY ASSESSMENT</b> .....	5
<i>Kei Ishiyama ; Yosuke Sugiura ; Tetsuya Shimamura</i>	
<b>ACCELERATING RESIDUE-TO-BINARY CONVERSION OF VERY HIGH CARDINALITY MODULI SET FOR FULLY HOMOMORPHIC ENCRYPTION</b> .....	9
<i>Truong Phu Truan Ho ; Chip-Hong Chang</i>	
<b>AN ULTRA-LOW-POWER VARIABLE-ACCURACY BIT-SERIAL FFT BUTTERFLY PROCESSING ELEMENT FOR IOT SENSORS</b> .....	13
<i>Yue Lu ; Tom J Kazmierski</i>	
<b>LOWER-NORM CRITERION BASED BACKGROUND NOISE ESTIMATION FOR SIMPLE OBSERVATION MODEL</b> .....	17
<i>Akitoshi Itai ; Yuta Hara</i>	
<b>BINAURAL-CUE-BASED NOISE REDUCTION USING MULTIRATE QUASI-ANSI FILTER BANK FOR HEARING AIDS</b> .....	21
<i>Huei-Shiuan Tang ; Cheng-Yen Yang ; Chih Wei Liu ; Chia-Cheng Chien</i>	
<b>A DIGITAL LDO WITH TRANSIENT ENHANCEMENT AND LIMIT CYCLE OSCILLATION REDUCTION</b> .....	25
<i>Mo Huang ; Yan Lu ; U. Seng-Pan ; Rui P. Martins</i>	
<b>A SUB-1V LOW DROPOUT REGULATOR WITH IMPROVED TRANSIENT PERFORMANCE FOR LOW POWER DIGITAL SYSTEMS</b> .....	29
<i>Y. S. Jiang ; D. Wang ; P. K. Chan</i>	
<b>DIGITALLY ASSISTED LOW DROPOUT REGULATOR DESIGN FOR LOW DUTY CYCLE IOT APPLICATIONS</b> .....	33
<i>Yan Lu</i>	
<b>A DIGITAL LOW-DROPOUT-REGULATOR WITH STEADY-STATE LOAD CURRENT (SLC) ESTIMATOR AND DYNAMIC GAIN SCALING (DGS) CONTROL</b> .....	37
<i>Jian-He Lin ; Wen-Jie Tsou ; Ke-Horng Chen ; Chin-Long Wey ; Ying-Hsi Lin ; Jian-Ru Lin ; Lsung-Yen Lsai</i>	
<b>A COMPARATIVE ANALYSIS ON BINARY AND MULTIPLE-UNARY WEIGHTED POWER STAGE DESIGN FOR DIGITAL LDO</b> .....	41
<i>Fan Yang ; Yasu Lu ; Philip K. T. Mok</i>	
<b>EMBEDDED HYBRID LDO TOPOLOGIES FOR DIGITAL LOAD CIRCUITS</b> .....	43
<i>Saad Bin Nasir ; Arijit Raychowdhury</i>	
<b>A LOW-POWER LDO CIRCUIT WITH A FAST LOAD REGULATION</b> .....	47
<i>Young-Jae Jang ; Seong-Eun Cho ; Byungsub Kim ; Jae-Yoon Sim ; Hong-June Park</i>	
<b>MOBILITY PATTERNS OF HUMAN POPULATION AMONG UNIVERSITY CAMPUSES</b> .....	50
<i>Shu-Min Zhang ; Xiang Li</i>	
<b>IMPROVING ROBUSTNESS OF POWER SYSTEMS VIA OPTIMAL LINK SWITCH-OFF</b> .....	54
<i>Haicheng Tu ; Yongxiang Xia ; Herbert H. C. Iu ; Chi K. Tse</i>	
<b>AN EFFECTIVE REWIRING STRATEGY FOR OPTIMIZING TRAFFIC PERFORMANCE OF COMMUNICATION NETWORKS</b> .....	57
<i>Zhenhao Chen ; Jiajing Wu ; Zibin Zheng</i>	
<b>EFFECT OF TRAFFIC GENERATION PATTERNS ON TRAFFIC PERFORMANCE OF COMPLEX NETWORKS</b> .....	61
<i>Junwen Zeng ; Jiajing Wu ; Zhenhao Chen ; Zibin Zheng</i>	
<b>CHAOS PROPAGATION IN COUPLED CHAOTIC CIRCUITS WITH MULTI-RING COMBINATION</b> .....	65
<i>Takahiro Chikazawa ; Yoko Uwate ; Yoshifumi Nishio</i>	
<b>SYNCHRONIZATION IN COMPLEX NETWORKS BY COUPLED PARAMETRICALLY EXCITED OSCILLATORS WITH PARAMETER MISMATCH</b> .....	69
<i>Kosuke Oi ; Yoko Uwate ; Yoshifumi Nishio</i>	
<b>A 1V LOW-POWER CMOS RESISTANCE-TO-FREQUENCY CONVERTER USING HYBRID TRANSDUCITOR FOR IOT</b> .....	73
<i>Kuan Chuang Koay ; P. K. Chan</i>	

<b>A HIGH OUTPUT-SWING CURRENT MIRROR WITH NEURON MOSFETS IN STANDARD CMOS TECHNOLOGY .....</b>	<b>77</b>
<i>Akio Shimizu ; Yohei Ishikawa ; Sumio Fukai</i>	
<b>SINGLE-STAGE OFFSET-CANCELLED LATCHED COMPARATOR SCHEDULED BY MULTI-LEVEL CONTROL ON RESET SWITCH .....</b>	<b>79</b>
<i>Sarang Kazemini ; Arefeh Soltani</i>	
<b>ANALOG INTEGRATED AUDIO FREQUENCY SYNTHESIZER.....</b>	<b>83</b>
<i>Douglas Andersson Hägglund ; Girish Aramanekoppa Subbarao ; Mohammed Abdulaziz ; Markus Törmänen</i>	
<b>A SELF BIASED FULL RANGE CURRENT SENSOR FOR BUCK REGULATOR .....</b>	<b>87</b>
<i>Chundong Wu ; Wang Ling Goh ; Wei Mao ; Lei Wang ; Yat Hei Lam ; Alan Chang ; Yong Lian</i>	
<b>A CMOS SINUSOIDAL SIGNAL GENERATOR BASED ON MIXED-TIME PROCESSING FOR ELECTRICAL BIOIMPEDANCE SPECTROSCOPY SUPPORTING BETA DISPERSION RANGE .....</b>	<b>91</b>
<i>Soon-Jae Kweon ; Sung-Hun Jo ; Jeong-Ho Park ; Hyung-Joun Yoo</i>	
<b>A SINGLE ON/OFF REFERENCE TRACKING BUCK CONVERTER USING TURNING POINT PREDICTION FOR DVFS APPLICATION .....</b>	<b>95</b>
<i>Sijie Pan ; Philip K. T. Mok</i>	
<b>A FAST TRANSIENT LDO BASED ON DUAL LOOP FVF WITH HIGH PSRR .....</b>	<b>99</b>
<i>Lei Wang ; Wei Mao ; Chundong Wu ; Alan Chang ; Yong Lian</i>	
<b>A 0.6-V POWER EFFICIENT DIGITAL LDO WITH 99.7% CURRENT EFFICIENCY UTILIZING LOAD CURRENT AWARE CLOCK MODULATION FOR FAST TRANSIENT RESPONSE .....</b>	<b>103</b>
<i>Karthik Gopal Jayaraman ; Karim Rawy ; Tony T. Kim</i>	
<b>RF ENERGY HARVESTER WITH PEAK POWER CONVERSION EFFICIENCY TRACKING .....</b>	<b>107</b>
<i>Menghan Sun ; Damith Ranasinghe ; Said F. Al-Sarawi</i>	
<b>A COMPACT, RESOURCE SHARING ON-CHIP SOFT-START TECHNIQUE FOR AUTOMOTIVE DC-DC CONVERTERS .....</b>	<b>111</b>
<i>K T Hafeez ; Ashudeb Dutta ; S G Singh ; Krishna Kanth Gowri Avalur</i>	
<b>SUCCESS RATE MODEL FOR FULLY AES-128 IN CORRELATION POWER ANALYSIS.....</b>	<b>115</b>
<i>Ali Akbar Pammu ; Kwen-Siong Chong ; Ne Kyaw Zwa Lwin ; Weng-Geng Ho ; Nan Liu ; Bah-Hwee Gwee</i>	
<b>COMPACT SPIN TRANSFER TORQUE NON-VOLATILE FLIP FLOP DESIGN FOR POWER-GATING ARCHITECTURE.....</b>	<b>119</b>
<i>Karim Ali ; Fei Li ; Sunny Y. H. Lua ; Chun-Huat Heng</i>	
<b>A LOW POWER AND COMPACT PHYSICAL UNCLONABLE FUNCTION BASED ON THE CASCODE CURRENT MIRRORS .....</b>	<b>127</b>
<i>Shibang Lin ; Dejian Liang ; Yuan Cao ; Xiaofang Pan ; Xiaojin Zhao</i>	
<b>CMOS-MEMRISTOR DENDRITE THRESHOLD CIRCUITS .....</b>	<b>131</b>
<i>Askhat Zhanbossinov ; Kamilya Smagulova ; Alex Pappachen James</i>	
<b>LATERAL SILICON NANOWIRE BASED STANDARD CELL DESIGN FOR HIGHER PERFORMANCE.....</b>	<b>135</b>
<i>Om. Prakash ; M. Sharma ; A. Bulusu ; A. K. Saxena ; S. K. Manhas ; S. Maheshwaram</i>	
<b>AN FPGA-BASED QUALITY FILTER FOR DE NOVO SEQUENCE ASSEMBLY PIPELINE .....</b>	<b>139</b>
<i>Chun-Shen Liu ; Nae-Chyun Chen ; Yu-Cheng Li ; Yi-Chang Lu</i>	
<b>MVDR BASED ADAPTIVE BEAMFORMER DESIGN AND ITS FPGA IMPLEMENTATION FOR ULTRASONIC IMAGING .....</b>	<b>143</b>
<i>Shin-Shiang Wang ; Yi-Chi Tien ; Yin-Tsung Hwang ; Jin-Fa Lin ; Guo-Zua Wu</i>	
<b>IMPLEMENTATION OF INTELLIGENT HOME APPLIANCES BASED ON IOT .....</b>	<b>146</b>
<i>Tsung-Han Tsai ; Kung-Long Zhang</i>	
<b>A PROCESSOR SHIELD FOR SOFTWARE-BASED ON-LINE SELF-TEST .....</b>	<b>149</b>
<i>Ching-Wen Lin ; Chung-Ho Chen</i>	
<b>EDGE-BASED MOVING OBJECT TRACKING ALGORITHM FOR AN EMBEDDED SYSTEM .....</b>	<b>153</b>
<i>Kai Xiang Yang ; Ming Hwa Sheu</i>	
<b>EFFECTIVE MODEL CONSTRUCTION FOR ENHANCED PREDICTION IN EXAMPLE-BASED SUPER-RESOLUTION .....</b>	<b>156</b>
<i>Chun-Wei Chen ; Fang-Kai Hsu ; Der-Wei Yang ; Jonas Wang ; Ming-Der Shieh</i>	
<b>LOW-COST PROTOTYPE DESIGN OF A PORTABLE ECG SIGNAL RECORDER .....</b>	<b>160</b>
<i>Shin-Chi Lai ; Te-Hsuan Hung ; Wen-Chih Li ; Yu-Syuan Jhang ; Kuan-Ying Chang ; Wen-Ho Juang ; Ching-Hsing Luo</i>	
<b>ARCHITECTURAL MODELING OF A MULTI-TONE/SINGLE-SIDEBAND SERIAL LINK TRANSCEIVER FOR LOSSY WIRELINE DATA LINKS .....</b>	<b>164</b>
<i>Gain Kim ; Yusuf Leblebici</i>	
<b>FULLY COHERENT SHAPED OFFSET QPSK DEMODULATOR ARCHITECTURE WITH SUPERIOR HARDWARE EFFICIENCY .....</b>	<b>168</b>
<i>Dominik Rieth ; Christoph Heller ; Gerd Ascheid</i>	

<b>NARROWBAND INTERFERENCE SUPPRESSION WITH SYMBOL INTERLEAVING FOR UWB COMMUNICATION SYSTEMS.....</b>	172
<i>Eisaku Ogawa ; Yosuke Sugiura ; Tetsuya Shimamura</i>	
<b>THE RESEARCH OF BROADBAND MIMO MILLIMETER WAVE TRANSCEIVER SYSTEM: DESIGN AND TEST .....</b>	176
<i>Fei Huang ; Jianyi Zhou ; Zhiqiang Yu ; Binqi Yang ; Ji Lan ; Weichen Huang</i>	
<b>A COMPACT MULTI-MODE CORDIC WITH GLOBAL-SHIFTING-SUM (GSS) METHOD.....</b>	180
<i>Gihoon Jung ; Kyungrak Choi ; Jongsun Park</i>	
<b>HIGH-EFFICIENCY AND COST-SHARING ARCHITECTURE DESIGN OF FAST ALGORITHM BASED MULTIPLE 4×4 AND 8×8 FORWARD TRANSFORMS FOR MULTI-STANDARD VIDEO ENCODER.....</b>	184
<i>Hao-Fan Hsu ; Chia-Wei Chang ; Chih-Peng Fan</i>	
<b>A DESIGN OF A COST-EFFECTIVE LOOK-UP TABLE FOR RGB-TO-RGBW CONVERSION.....</b>	188
<i>Sunwoong Kim ; Hyuk-Jae Lee</i>	
<b>EFFICIENT HOLE FILLING AND DEPTH ENHANCEMENT BASED ON TEXTURE IMAGE AND DEPTH MAP CONSISTENCY .....</b>	192
<i>Ting-An Chang ; Jung-Ping Kuo ; Jar-Ferr Yang</i>	
<b>WEIGHTED PEAK RATIO FOR ESTIMATING STEREO CONFIDENCE LEVEL USING COLOR SIMILARITY .....</b>	196
<i>Sanghun Kim ; Chan Young Jang ; Young Hwan Kim</i>	
<b>DEPTH EXTRACTION USING ADAPTIVE BLUR CHANNEL SELECTION FOR DUAL APERTURE CAMERA .....</b>	198
<i>Kyungho Kim ; Yeongmin Lee ; Hyun Sang Park ; Chong-Min Kyung</i>	
<b>STEP SHIFT: A FAST IMAGE SEGMENTATION ALGORITHM AND ITS HARDWARE IMPLEMENTATION FOR NEXT-GENERATION SEQUENCING FLUORESCENCE DATA .....</b>	202
<i>Xiao-Xuan Huang ; Chun-Hsien Ho ; Yu-Cheng Li ; Nae-Chyun Chen ; Yi-Chang Lu</i>	
<b>IMPLEMENTATION OF A RESOURCE-CONSTRAINED ECC PROCESSOR WITH POWER ANALYSIS COUNTERMEASURE .....</b>	206
<i>Zilong Liu ; Dongsheng Liu ; Xiangcheng Sun ; Xuecheng Zou ; Hui Lin</i>	
<b>CORRELATION-GRAPH-BASED TEMPERATURE SENSOR ALLOCATION FOR THERMAL-AWARE NETWORK-ON-CHIP SYSTEMS.....</b>	210
<i>Kun-Chih Jimmy Chen ; Yen-Po Lin ; Kai-Yu Chiang ; Yu-Hsien Chen</i>	
<b>OPTIMIZATION OF AREA AND POWER IN MULTI-MODE POWER GATING SCHEME FOR STATIC MEMORY ELEMENTS .....</b>	214
<i>Xing Su ; Shinji Kimura</i>	
<b>FPGA-BASED REAL-TIME LANE DETECTION FOR ADVANCED DRIVER ASSISTANCE SYSTEMS .....</b>	218
<i>Seokha Hwang ; Youngjoo Lee</i>	
<b>IMPLEMENTATION EVALUATION OF SCAN-BASED ATTACK AGAINST A TRIVIUM CIPHER CIRCUIT .....</b>	220
<i>Daisuke Oku ; Masao Yanagisawa ; Nozomu Togawa</i>	
<b>A SIMPLE METHOD FOR FINDING ALL CHARACTERISTIC CURVES OF PIECEWISE-LINEAR RESISTIVE CIRCUITS USING AN INTEGER PROGRAMMING SOLVER.....</b>	224
<i>Kiyotaka Yamamura ; Ryota Watanabe</i>	
<b>FINDING ALL SOLUTIONS OF PIECEWISE-LINEAR RESISTIVE CIRCUITS USING EXCEL.....</b>	228
<i>Kiyotaka Yamamura ; Daiki Koyama</i>	
<b>A NEW DECENTRALIZED DISCRETE-TIME ALGORITHM FOR ESTIMATING ALGEBRAIC CONNECTIVITY OF MULTIAGENT NETWORKS.....</b>	232
<i>Kento Endo ; Norikazu Takahashi</i>	
<b>RIGOROUS ANALYSIS OF ARNOLD TONGUES IN A MANIFOLD PIECEWISE-LINEAR CIRCUIT.....</b>	236
<i>Viet Duc Le ; Tadashi Tsubone ; Naohiko Inaba</i>	
<b>WIDE CURRENT RANGE AND HIGH COMPLIANCE-VOLTAGE BULK-DRIVEN CURRENT MIRRORS: SIMPLE AND CASCODE .....</b>	240
<i>Kriangkrai Sooksood</i>	
<b>AN ULTRA-LOW POWER AND OFFSET-INSENSITIVE CMOS SUBTHRESHOLD VOLTAGE REFERENCE .....</b>	243
<i>Lidan Wang ; Chenahang Zhan ; Guofeng Li</i>	
<b>METHODS FOR MEASURING LOOP-GAIN FUNCTION OF HIGH-FREQUENCY DC-DC CONVERTERS .....</b>	247
<i>Xun Liu ; Junmin Jiang ; Philip K. T. Mok ; Wing-Hung Ki</i>	

<b>AN ILLUMINATION AWARE SINGLE SOLAR-CELL VCO CCO BASED CHARGE-PUMP ENERGY HARVESTING SYSTEM FOR SOC INTEGRATION .....</b>	<b>250</b>
<i>R P Kartheek ; Akash Gupta ; Murali K. Rajendran ; Ashudeb Dutta</i>	
<b>0.6-V, SUB-NW, SECOND-ORDER LOWPASS FILTERS USING FLIPPED VOLTAGE FOLLOWERS .....</b>	<b>254</b>
<i>Chutham Sawigun ; Prajuab Pawarangkoon</i>	
<b>ON-CHIP ESD PROTECTION DESIGN FOR RADIO-FREQUENCY POWER AMPLIFIER WITH LARGE-SWING-TOLERANCE CONSIDERATION.....</b>	<b>258</b>
<i>Guan-Yi Li ; Chun-Yu Lin</i>	
<b>DESIGN OF 5.5GHZ LC OSCILLATOR USING DISTRIBUTED GRID OF N-WELL IN P-SUBSTRATE INDUCTOR.....</b>	<b>262</b>
<i>S. A Enche Ab Rahim ; Adel Barakat ; Ramesh K. Pokharel</i>	
<b>WIDE-BAND INJECTION-LOCKED FREQUENCY DOUBLER.....</b>	<b>265</b>
<i>Wen-Cheng Lai ; Jheng-Wei Jhuang ; Sheng-Lyang Jang ; Guan-Yu Lin ; Ching-Wen Hsue</i>	
<b>A TUNABLE POWER AMPLIFIER EMPLOYING DIGITALLY CONTROLLED ACCUMULATION-MODE VARACTOR ARRAY FOR 2.4-GHZ SHORT-RANGE WIRELESS COMMUNICATION .....</b>	<b>269</b>
<i>Sanggil Kim ; Donggu Im</i>	
<b>INTERFERENCE MEASUREMENT AND ANALYSIS OF FULL-DUPLEX WIRELESS SYSTEM IN 60 GHZ BAND.....</b>	<b>273</b>
<i>Hung-Wei Yang ; Yongyu He ; Chih-Wei Jen ; Chun-Yi Liu ; Shyh-Jye Jou ; Xuefeng Yin ; Meng Ma ; Bingli Jiao</i>	
<b>DESIGN AND IMPLEMENTATION OF A LOW-LATENCY, HIGH-THROUGHPUT SORTED QR DECOMPOSITION CIRCUIT FOR MIMO COMMUNICATIONS .....</b>	<b>277</b>
<i>Wei-Yang Chen ; Daniel Guenther ; Chung-An Shen ; Gerd Ascheid</i>	
<b>A GENERALIZED EIGENVALUE DECOMPOSITION PROCESSOR FOR MULTI-USER MIMO PRECODING.....</b>	<b>281</b>
<i>Chun-An Chen ; Yang Zao-Fu ; Chiao-En Chen ; Yuan-Hao Huang</i>	
<b>DESIGN OF A LOW-COMPLEXITY O-QPSK TRANSCEIVER WITH SPATIAL MODULATION FOR INTERNET-OF-THINGS APPLICATIONS.....</b>	<b>285</b>
<i>Ching-Hao Yang ; Pei-Yun Tsai</i>	
<b>AN IDD RECEIVER OF LDPC CODED MODULATION SCHEME FOR FLASH MEMORY APPLICATIONS .....</b>	<b>289</b>
<i>Mao-Ruei Li ; Ting-Yu Kuan ; Huang-Chang Lee ; Yeong-Luh Ueng</i>	
<b>EFFICIENT HARDWARE ARCHITECTURE OF DETERMINISTIC MPA DECODER FOR SCMA .....</b>	<b>293</b>
<i>Chao Yang ; Chuan Zhang ; Shunqing Zhang ; Xiaohu You</i>	
<b>A 2-CLOCK-CYCLE NAÏVE BAYES CLASSIFIER FOR DYNAMIC BRANCH PREDICTION IN PIPELINED RISC MICROPROCESSORS.....</b>	<b>297</b>
<i>Iitaru Hida ; Masayuki Ikebe ; Tetsuya Asai ; Masato Motomura</i>	
<b>POWER-FLOW SIMULATION WITH VISUALIZATION FUNCTION BASED ON IEEE COMMON DATA FORMAT .....</b>	<b>301</b>
<i>Shohei Sugino ; Kazuhiro Okabe ; Nobuyoshi Komuro ; Hiroo Sekiya</i>	
<b>NEW CLASS-E RECTIFIER WITH LOW VOLTAGE STRESS.....</b>	<b>305</b>
<i>Xiuqin Wei ; Hiroo Sekiya ; Tadashi Suetsugu</i>	
<b>PARTICLE SWARM OPTIMIZATION FOR MATRIX CONVERTER OF SWITCHING PATTERN DESIGN.....</b>	<b>309</b>
<i>Takuya Shindo ; Kenya Jin'No</i>	
<b>FIREFLY ALGORITHM EXISTING LEADER FIREFLIES.....</b>	<b>313</b>
<i>Masaki Takeuchi ; Haruna Matsushita ; Yoko Uwate ; Yoshifumi Nishio</i>	
<b>EQUIDISTANT MIXER-BASED FREQUENCY GENERATION FOR 60 GHZ FBMC TRANSMITTER TOPOLOGIES .....</b>	<b>317</b>
<i>Oner Hanay ; Erkan Bayram ; David Bierbuesse ; Renato Negra</i>	
<b>DESIGN OF A 8-TAPS, 10GBPS TRANSMITTER FOR AUTOMOTIVE MICRO-CONTROLLERS.....</b>	<b>321</b>
<i>Andrea Bandiziol ; Werner Grollitsch ; Francesco Brandonisio ; Roberto Nonis ; Pierpaolo Palestri</i>	
<b>DIGITAL CLOCK DATA RECOVERY CIRCUIT FOT S/PDIF .....</b>	<b>325</b>
<i>Jonghoon Kang ; Chanho Lee</i>	
<b>A 3.5/7.0/14-GB/S MULTI-RATE CLOCK AND DATA RECOVERY CIRCUIT WITH A MULTI-MODE ROTATIONAL BINARY PHASE DETECTOR.....</b>	<b>327</b>
<i>Ki-Hyun Pyun ; Dae-Hyun Kwon ; Woo-Young Choi</i>	
<b>A MULTI-TAP INDUCTOR BASED 2.0-4.1 GHZ WIDEBAND LC-OSCILLATOR.....</b>	<b>330</b>
<i>Zaira Zahir ; Gaurab Banerjee</i>	

<b>A 5-B 1-GS/S BINARY-SEARCH ADC IN 90NM CMOS</b> .....	334
<i>Yung-Hui Chung ; Cheng-Hsun Tsai ; Hsuan-Chih Yeh</i>	
<b>DYNAMIC MAPPING METHOD FOR STATIC AND DYNAMIC PERFORMANCE IMPROVEMENT ON CURRENT-STEERING DIGITAL-TO-ANALOG CONVERTER</b> .....	336
<i>Wei Mao ; Yongfu Li ; Chun-Huat Heng ; Yong Lian</i>	
<b>A FRONT-END CIRCUIT WITH 16-CHANNEL 12-BIT 100-KSPS RC-HYBRID SAR ADC FOR INDUSTRIAL MONITORING APPLICATION</b> .....	340
<i>Zhelu Li ; Jianxiong Xi ; Lenian He ; Kexu Sun</i>	
<b>A LOW JITTER BURST-MODE CLOCK AND DATA RECOVERY CIRCUIT WITH TWO SYMMETRIC VCO'S</b> .....	344
<i>Bum-Hee Choi ; Kyung-Sub Son ; Jin-Ku Kang</i>	
<b>A 9-BIT, 1.08PS RESOLUTION TWO-STEP TIME-TO-DIGITAL CONVERTER IN 65 NM CMOS FOR TIME-MODE ADC</b> .....	348
<i>Junjie Kong ; Stephan Henzler ; Doris Schmitt-Landsiedel ; Litter Siek</i>	
<b>A SYSTEMATIC METHODOLOGY FOR DESIGN AND ANALYSIS OF APPROXIMATE ARRAY MULTIPLIERS</b> .....	352
<i>Takahiro Yamamoto ; Ittetsu Taniguchi ; Hiroyuki Tomiyama ; Shigeru Yamashita ; Yuko Hara-Azumi</i>	
<b>ENERGY-EFFICIENT HYBRID ADDER DESIGN BY USING INEXACT LOWER BITS ADDER</b> .....	355
<i>Sunghyun Kim ; Youngmin Kim</i>	
<b>COOPERATIVE VIRTUAL CHANNEL ROUTER FOR ADAPTIVE HARDWIRED FPGA NETWORK-ON-CHIP</b> .....	358
<i>F. F Zakaria ; Naa Latif ; Shaiful Jahari Hashim ; P. Ehkan ; F. Z. Rokhani</i>	
<b>MIXED ERROR CORRECTION SCHEME AND ITS DESIGN OPTIMIZATION FOR SOFT-ERROR TOLERANT DATAPATHS</b> .....	362
<i>Junghoon Oh ; Mineo Kaneko</i>	
<b>YIELD AND POWER IMPROVEMENT METHOD BY POST-SILICON DELAY TUNING AND TECHNOLOGY MAPPING</b> .....	366
<i>Hayato Mashiko ; Yukihide Kohira</i>	
<b>A NEW ONLINE TEST AND DEBUG METHODOLOGY FOR AUTOMOTIVE CAMERA IMAGE PROCESSING SYSTEM</b> .....	370
<i>Hyunggoy Oh ; Inhyuk Choi ; Sungho Kang</i>	
<b>A MODIFIED PREDICTOR-CORRECTOR METHOD FOR TRACING SOLUTION CURVES</b> .....	372
<i>Kiyotaka Yamamura ; Kiyoshi Adachi</i>	
<b>VOLTAGE CONTROLLED MEMRISTOR THRESHOLD LOGIC GATES</b> .....	376
<i>Akshay Kumar Maan ; Alex Pappachen James</i>	
<b>PHASE-CONTROLLED SYSTEM DESIGN VIA MIXED H8 SYNTHESIS AND NONLINEAR METHOD</b> .....	380
<i>N. S. Ahmad ; S. J. Abu Bakar</i>	
<b>SWITCHING SYNCHRONIZATION STATES OF A RING OF COUPLED CHAOTIC CIRCUITS WITH ONE-DIRECTION DELAY EFFECTS</b> .....	384
<i>Seiya Kita ; Yoko Uwate ; Yoshifumi Nishio</i>	
<b>TOWARDS IMPROVING ACCURACY OF NONLINEAR TIME INVARIANT VLSI CIRCUITS USING VOLTERRA SERIES BASED PARAMETRIC ANALYSIS</b> .....	388
<i>J. Ravindra ; Sai Satyanarayana Re</i>	
<b>EFFICIENT HARDWARE ARCHITECTURE OF DETERMINISTIC MPA DECODER FOR SCMA</b> .....	392
<i>Chao Yang ; Chuan Zhang ; Shunqing Zhang ; Xiaohu You</i>	
<b>ASIC DESIGN OF A LOW-COMPLEXITY K-BEST VITERBI DECODER FOR IOT APPLICATIONS</b> .....	396
<i>Hiromasa Kato ; Thi Hong Tran ; Yasuhiko Nakashima</i>	
<b>LOW LATENCY CHECK NODE UNIT ARCHITECTURE FOR NONBINARY LDPC DECODING</b> .....	400
<i>Huyen Pham Thi ; Hanho Lee</i>	
<b>EFFICIENT SOR-BASED DETECTION AND ARCHITECTURE FOR LARGE-SCALE MIMO UPLINK</b> .....	402
<i>Anlan Yu ; Chuan Zhang ; Shunqing Zhang ; Xiaohu You</i>	
<b>A LOW-POWER SINGLE-ENDED 11-BIT SA-ADC WITH 1 V SUPPLY VOLTAGE AND 2 V INPUT VOLTAGE RANGE FOR CMOS IMAGE SENSORS</b> .....	410
<i>Junbo Shim ; Min-Kyu Kim ; Seong-Kwan Hong ; Oh-Kyong Kwon</i>	
<b>A LOW-COMPLEXITY FAST-LOCKING DIGITAL PLL WITH MULTI-OUTPUT BANG-BANG PHASE DETECTOR</b> .....	418
<i>Qiwei Huang ; Chenchang Zhan ; Jinwook Burm</i>	

<b>A 76NW, 4KS/S 10-BIT SAR ADC WITH OFFSET CANCELLATION FOR BIOMEDICAL APPLICATIONS</b> .....	421
<i>Manuel Delgado-Restituto ; Manuel Carrasco-Robles ; Rafaella Fiorelli ; Antonio J. Ginés-Arteaga ; Ángel Rodríguez-Vázquez</i>	
<b>AN EFFICIENT, WIDE RANGE TIME-TO-DIGITAL CONVERTER USING CASCADED TIME-INTERPOLATION STAGES FOR ELECTRICAL IMPEDANCE SPECTROSCOPY</b> .....	425
<i>Seongheon Shin ; Soon-Jae Kweon ; Jeong-Ho Park ; Yong-Chang Choi ; Hyung-Joun Yoo</i>	
<b>NEAR-INFRARED-RAY AND SIDE-VIEW VIDEO BASED DROWSY DRIVER DETECTION SYSTEM: WHETHER OR NOT WEARING GLASSES</b> .....	429
<i>Wei-Cheng Li ; Wei-Liang Ou ; Chih-Peng Fan ; Chien-Hsiu Huang ; Yi-Shian Shie</i>	
<b>HARDWARE DESIGN OF HISTOGRAMS OF ORIENTED GRADIENTS BASED ON LOCAL BINARY PATTERN AND BINARIZATION</b> .....	433
<i>Shen-Fu Hsiao ; Jun-Mao Chan ; Ching-Hui Wang</i>	
<b>FAST-GAUSSIAN SIFT AND ITS HARDWARE ARCHITECTURE FOR KEYPOINT DETECTION</b> .....	436
<i>Liu Ke ; Jun Wang ; Xijun Zhao ; Fan Liang</i>	
<b>DEPTH REFINEMENT ON SPARSE-DEPTH IMAGES USING VISUAL PERCEPTION CUES</b> .....	440
<i>Muhammad Umar Karim Khan ; Asim Khan ; Chong-Min Kyung</i>	
<b>DISTRIBUTED VIDEO TRANSCODING ON A HETEROGENEOUS COMPUTING PLATFORM</b> .....	444
<i>Zhi Hao Chang ; Bih Fei Jong ; Wei Jing Wong ; M. L. Dennis Wong</i>	
<b>OL-SVR BASED SOFT-SENSOR FOR REAL-TIME ESTIMATION OF SOLAR IRRADIANCE</b> .....	448
<i>Jieming Ma ; Ziqiang Bi ; Yu Shi ; Ka Lok Man ; Xinyu Pan ; Jian Wang</i>	
<b>THE PNP WEB TAG: A PLUG-AND-PLAY PROGRAMMING MODEL FOR CONNECTING IOT DEVICES TO THE WEB OF THINGS</b> .....	452
<i>Fan Yang ; Danny Hughes ; Nelson Matthys ; Ka Lok Man</i>	
<b>RECTANNA DESIGN FOR ENERGY HARVESTING</b> .....	456
<i>Jing Chen Wang ; Mark Leach ; Zhao Wang ; Ka Lok Man ; Eng Gee Lim</i>	
<b>AN EXPLORATION OF USABLE AUTHENTICATION MECHANISMS FOR VIRTUAL REALITY SYSTEMS</b> .....	458
<i>Zhen Yu ; Hai-Ning Liang ; Charles Fleming ; Ka Lok Man</i>	
<b>MEMORY ACCESS ALGORITHM FOR LOW ENERGY CPU/GPU HETEROGENEOUS SYSTEMS WITH HYBRID DRAM/NVM MEMORY ARCHITECTURE</b> .....	461
<i>Tsai-Kan Chien ; Lih-Yih Chiou ; Chieh-Wen Cheng ; Shyh-Shyuan Sheu ; Pei-Hua Wang ; Ming-Jinn Tsai ; Chih-I Wu</i>	
<b>A POST-PROCESSING ALGORITHM FOR REDUCING STRONG ERROR EFFECTS IN NAND FLASH MEMORY</b> .....	465
<i>Sung-Rae Kim ; Kijun Lee ; Gyuyeol Kong ; Myung-Kyu Lee ; Dongmin Shin ; Geunyeong Yu ; Beomkyu Shin ; Pilsang Yoon ; Hongrak Son ; Jun-Jin Kong</i>	
<b>LOW LEAKAGE MASK VERTICAL CONTROL TCAM FOR NETWORK ROUTER</b> .....	469
<i>Yu-Cheng Cheng ; Jin-Hao Chen ; Tung-Chi Wu ; Yen-Jen Chang</i>	
<b>READ MARGIN ANALYSIS IN AN RRAM CROSSBAR ARRAY</b> .....	473
<i>Jaehyun Seo ; Byungsub Kim</i>	
<b>SLICED POLAR CODES</b> .....	476
<i>Eran Hof</i>	
<b>A BIRA USING FAULT-FREE MEMORY REGION FOR AREA REDUCTION</b> .....	480
<i>Chang-Hyun Oh ; Sae-Eun Kim ; Joon-Sung Yang</i>	
<b>LOW-FREQUENCY NOISE REDUCTION TECHNIQUE FOR ACCELEROMETER READOUT CIRCUIT</b> .....	483
<i>Po-Chang Wu ; Chih-Yuan Yeh ; Hann-Huei Tsai ; Ying-Zong Juang</i>	
<b>A HIGH BACKGROUND LIGHT SUBTRACTION CIRCUIT FOR LONG RANGE TIME-OF-FLIGHT CAMERAS</b> .....	487
<i>Chandani Anand ; Kapil Jainwal ; Mukul Sarkar</i>	
<b>MODELLING AND ANALYSIS OF SIGNAL FLOW PLATFORM IMPLEMENTATION INTO RETINAL CELL PATHWAY</b> .....	491
<i>Jason K. Eshraghian ; Seungbum Baek ; Kyoungrok Cho ; Nicolangelo Iannella ; Jun-Ho Kim ; Yong Sook Goo ; Herbert H. C. Iu ; Tyrone Fernando ; Kamran Eshraghian</i>	
<b>INTERFACE IC FOR BREATH ANALYZER WITH FOUR THREE-ELECTRODE METAL-OXIDE GAS SENSORS AND A HUMIDITY SENSOR</b> .....	495
<i>Jeong-Ho Park ; Han-Won Cho ; Soon-Jae Kweon ; Hyung-Joun Yoo</i>	
<b>DARK CURRENT ANALYSIS OF P-TYPE AND N-TYPE PIXELS UNDER TOTAL IONIZING DOSE RADIATION EFFECTS</b> .....	499
<i>Ran Zheng ; Jia Wang</i>	



<b>SIMULTANEOUS LAYER-AWARE AND REGION-AWARE PARTITIONING FOR 3D IC</b> .....	502
<i>Yung-Hao Lai ; Yang Lang Chang ; Jyh-Perng Fang ; Jie Lee</i>	
<b>A UNIFIED GDB-BASED SOURCE-TRANSACTION LEVEL SW/HW CO-DEBUGGING</b> .....	506
<i>Tsun-Hsin Chang ; Shao-Chieh Hou ; Ing-Jer Huang</i>	
<b>PROFILING-BASED TASK GRAPH EXTRACTION ON MULTIPROCESSOR SYSTEM-ON-CHIP</b> .....	510
<i>Sodam Han ; Yonghee Yun ; Young Hwan Kim</i>	
<b>CALCULATING THE PROBABILITY OF TIMING VIOLATION OF F/F-CONTROLLED PATHS WITH TIMING VARIATIONS</b> .....	514
<i>Hyun-jeong Kwon ; Young Hwan Kim</i>	
<b>UNIFIED HW/SW FRAMEWORK FOR EFFICIENT SYSTEM LEVEL SIMULATION</b> .....	518
<i>N. Sutisna ; L. Lanante ; Y. Nagao ; M. Kurosaki ; H. Ochi</i>	
<b>TEST ACCESS MECHAISM FOR STACK TEST TIME REDUCTION OF 3-DIMENSIONAL INTEGRATED CIRCUIT</b> .....	522
<i>Inhyuk Choi ; Hyunggoy Oh ; Sungho Kang</i>	
<b>DESIGN OPTIMIZATION CONSIDERING GUIDING TEMPLATE FEASIBILITY AND REDUNDANT VIA INSERTION FOR DIRECTED SELF-ASSEMBLY</b> .....	526
<i>Shao-Yun Fang ; Yun-Xiang Hong</i>	
<b>MACHINE LEARNING (ML)-BASED LITHOGRAPHY OPTIMIZATIONS</b> .....	530
<i>Seongbo Shim ; Suhyeong Choi ; Youngsoo Shin</i>	
<b>MULTIPLE-PATTERNING LITHOGRAPHY-AWARE ROUTING FOR STANDARD CELL LAYOUT SYNTHESIS</b> .....	534
<i>Kuen-Wey Lin ; Yih-Lang Li ; Rung-Bin Lin</i>	
<b>MANUFACTURABILITY-AWARE MASK ASSIGNMENT IN MULTIPLE PATTERNING LITHOGRAPHY</b> .....	538
<i>Yukihide Kohira ; Atsushi Takahashi ; Tomomi Matsui ; Chikaaki Kodama ; Shigeki Nojima ; Satoshi Tanaka</i>	
<b>VLSI LAYOUT HOTSPOT DETECTION BASED ON DISCRIMINATIVE FEATURE EXTRACTION</b> .....	542
<i>Hang Zhang ; Haoyu Yang ; Bei Yu ; Evangeline F. Y. Young</i>	
<b>DESIGN OF LOW-DROPOUT REGULATOR USING A-INGAZNO THIN-FILM TRANSISTORS</b> .....	546
<i>Yongchan Kim ; Hojin Lee</i>	
<b>A LOW-AREA 10B COLUMN DRIVER WITH RESISTOR-RESISTOR-STRING DAC FOR MOBILE ACTIVE-MATRIX LCDS</b> .....	548
<i>Jong-Seok Kim ; Jin-O Yoon ; Byong-Deok Choi</i>	
<b>ON-GLASS OPERATIONAL AMPLIFIER USING SOLUTION-PROCESSED A-IGZO TFTS</b> .....	551
<i>Daejung Kim ; Keun-Yeong Choi ; Hojin Lee</i>	
<b>LOW-POWER COUNTER FOR COLUMN-PARALLEL CMOS IMAGE SENSORS</b> .....	554
<i>Jong-Seok Kim ; Jin-O Yoon ; Byong-Deok Choi</i>	
<b>FINGERPRINT PIXEL SENSOR ARRAY ON A DISPLAY</b> .....	557
<i>In Hye Kang ; Jun Young Hwang ; Byung Seong Bae</i>	
<b>DESIGN OF A STANDING WAVE OSCILLATOR BASED PLL</b> .....	559
<i>Wei Zhang ; Youde Hu ; Keji Cui ; Lebo Wang ; Lirong Zheng</i>	
<b>AN ACCURATE DESIGN APPROACH FOR TWO-STAGE CMOS OPERATIONAL AMPLIFIERS</b> .....	563
<i>Yushun Guo</i>	
<b>DESIGN OF A HYBRID RING OSCILLATOR AT 1.5/3.0 GHZ WITH LOW POWER SUPPLY SENSITIVITY</b> .....	567
<i>Vivek Sharma ; Kapil Jainwal ; Abhishek Tripathi</i>	
<b>HIGH FRAME RATE VGA CMOS IMAGE SENSOR USING TWO-STEP SINGLE SLOPE ADCS</b> .....	571
<i>Himchan Park ; Junan Lee ; Jinwoo Kim ; Yongsik Shin ; Jinwook Burm</i>	
<b>LIMITED SEARCH SPHERE DECODER AND ADAPTIVE DETECTOR FOR NOMA WITH SU-MIMO</b> .....	573
<i>I-Min Kuo ; Wen-Ching Hu ; Tzi-Dar Chiueh</i>	
<b>LEGO-BASED VLSI DESIGN AND IMPLEMENTATION OF POLAR CODES ENCODER ARCHITECTURE WITH RADIX-2 PROCESSING ENGINES</b> .....	577
<i>Xin-Yu Shih ; Po-Chun Huang ; Yu-Chun Chen</i>	
<b>ANALOG FILTERS DESIGN IN VLC ANALOG FRONT-END RECEIVER FOR REDUCING INDOOR AMBIENT LIGHT NOISE</b> .....	581
<i>Trio Adiono ; Angga Pradana ; Rachmad Vidya Wicaksana Putra ; Syifaul Fuada</i>	
<b>EFFICIENT SUCCESSIVE CANCELLATION DECODER FOR POLAR CODES BASED ON FROZEN BITS</b> .....	585
<i>Zheyang Piao ; Yeon-Jin Kim ; Jin-Gyun Chung</i>	

<b>ARCHITECTURE OF WLAN CHANNEL ESTIMATORS</b> .....	588
<i>My-Kieu Nguyen-Thi ; Ik-Joon Chang ; Jinsang Kim</i>	
<b>CLOSED-FORM DESIGN OF FIR FREQUENCY SELECTIVE FILTER USING DISCRETE SINE TRANSFORM</b> .....	591
<i>Chien-Cheng Tseng ; Su-Ling Lee</i>	
<b>DISCRETE FRACTIONAL HÉNON MAP BASED ON DIGITAL FRACTIONAL ORDER INTEGRATOR</b> .....	595
<i>Chien-Cheng Tseng ; Su-Ling Lee</i>	
<b>NORMAL-FORM STATE-SPACE REALIZATION OF SINGLE FREQUENCY IIR NOTCH FILTERS AND ITS APPLICATION TO ADAPTIVE NOTCH FILTERS</b> .....	599
<i>Yoichi Hinamoto ; Shotaro Nishimura</i>	
<b>LOW COMPLEXITY AND QUASI-LINEAR PHASE IIR FILTERS DESIGN BASED ON ITERATIVE CONVEX OPTIMIZATION</b> .....	603
<i>Jinghong Tan ; Jiajia Chen</i>	
<b>MULTIPLIERLESS TWO-STAGE COMB STRUCTURE WITH AN IMPROVED MAGNITUDE CHARACTERISTIC</b> .....	607
<i>Gordana Jovanovic Dolecek ; Alfonso Fernandez-Vazquez</i>	
<b>PIXEL-BASED PIPELINE HARDWARE ARCHITECTURE FOR HIGH-PERFORMANCE HAAR-LIKE FEATURE EXTRACTION</b> .....	611
<i>Yuki Fujita ; Fengwei An ; Aiwen Luo ; Xiangyu Zhang ; Lei Chen ; Hans Jürgen Mattausch</i>	
<b>A DUALBAND IMPEDANCE TRANSFORMER REALIZED BY FRACTIONAL-ORDER INDUCTOR AND CAPACITOR</b> .....	613
<i>Peng Chen ; Kai Yang ; Tianliang Zhang</i>	
<b>NONLINEAR INERTER IN THE LIGHT OF CHUA'S TABLE OF HIGHER-ORDER ELECTRICAL ELEMENTS</b> .....	617
<i>Dalibor Biolek ; Zdenek Biolek ; Viera Biolkova ; Zdenek Kolka</i>	
<b>CHARGING THE CAPACITOR VIA A (MEMORY) RESISTOR</b> .....	621
<i>Zdenek Biolek ; Dalibor Biolek ; Viera Biolkova</i>	
<b>ON USING THE CYCLICALLY-COUPLED QC-LDPC CODES IN FUTURE SSDS</b> .....	625
<i>Qing Lu ; Chiu-Wing Sham ; Francis C. M. Lau</i>	
<b>SYNCHRONIZATION PHENOMENA IN STAR-COUPLED VAN DER POL OSCILLATORS BY ADDING DIFFERENT FREQUENCY OSCILLATORS</b> .....	629
<i>Minh Hai Tran ; Kosuke Oi ; Yoko Uwate ; Yoshifumi Nishio</i>	
<b>TCAM-PUF WITH IMPROVED RELIABILITY AND UNIQUENESS FOR SECURITY IMPROVEMENT</b> .....	633
<i>T. Nagakarthik ; Jeong O Kim ; Tae Yang Kim ; Joon Ho Kong ; Jun Rim Choi</i>	
<b>PIM ARCHITECTURE EXPLORATION FOR HMC</b> .....	635
<i>Sangwoo Han ; Hyeokjun Seo ; ByoungJin Kim ; Eui-Young Chung</i>	
<b>ELECTROCHROMIC DISPLAY DRIVING SCHEME FOR HIGH DYNAMIC RANGE IMAGE CAPTURE</b> .....	637
<i>Seok-Jeong Song ; Dowon Kim ; Jeongrim Seo ; Ki-Hyuk Seol ; Hyoungsik Nam</i>	
<b>SELF-CONTAINED BUILT-IN-SELF-TEST/REPAIR TRANSCEIVERS FOR INTERCONNECTS IN 3DICS</b> .....	640
<i>Myat Thu Linn Aung ; Tony T. Kim</i>	
<b>A LOW POWER AND LOW NOISE CMOS CHOPPER AMPLIFIER FOR USE IN CAPACITIVE TYPE ACCELEROMETER</b> .....	642
<i>Chih-Yuan Yeh ; Jung-Tang Huang ; Po-Chang Wu ; Hann-Huei Tsai ; Ying-Zong Juang</i>	
<b>LOW-POWER, LIGHTWEIGHT AND RELIABILITY-ENHANCED CURRENT STARVED INVERTER BASED RO PUFs</b> .....	646
<i>Chao Qun Liu ; Yuan Cao ; Chip-Hong Chang</i>	
<b>INTERCEPTIVE SIDE CHANNEL ATTACK ON AES-128 WIRELESS COMMUNICATIONS FOR IOT APPLICATIONS</b> .....	650
<i>Ali Akbar Pammu ; Kwen-Siong Chong ; Weng-Geng Ho ; Bah-Hwee Gwee</i>	
<b>AN ADVANCED 3D FORMAT GENERATION ARCHITECTURE FOR VIDEO AND DEPTH</b> .....	654
<i>Pin-Chen Kuo ; Kuan-Ting Lee ; Ching-Lun Chou ; Chun-Wei Chang ; Bin-Da Liu ; Jar-Ferr Yang</i>	
<b>DEAR: A FRAMEWORK FOR POWER-EFFICIENT AND FLEXIBLE EMBEDDED DIGITAL SIGNAL PROCESSOR DESIGN</b> .....	658
<i>Chi-Ming Lee ; Yong-Jyun Huang ; Chih-Wei Liu ; Yarsun Hsu</i>	
<b>ANALYSIS OF A RECONFIGURABLE TEG ARRAY FOR HIGH EFFICIENCY THERMOELECTRIC ENERGY HARVESTING</b> .....	662
<i>Qiping Wan ; Ying-Khai Teh ; Philip K. T. Mok</i>	

<b>COMPARISON OF TWO SIGE 2-STAGE E-BAND POWER AMPLIFIER ARCHITECTURES</b> .....	666
<i>Tobias Tired ; Henrik Sjöland ; Göran Jönsson ; Johan Wernehag</i>	
<b>ANALYSIS OF NON-IDEAL EFFECTS AND ELECTROCHEMICAL IMPEDANCE SPECTROSCOPY OF ARRAYED FLEXIBLE NIO-BASED PH SENSOR</b> .....	670
<i>Siao-Jie Yan ; Jung-Chuan Chou ; Yi-Hung Liao ; Chih-Hsien Lai ; Jian-Syun Chen ; Bo-Yang Zhuang ; Hsiang-Yi Chen ; Ting-Wei Tseng</i>	
<b>SYSTEM-LEVEL FAILURE SIMULATION AND MEMORY ALLOCATION SCHEME IN 3D MEMORY</b> .....	674
<i>Jung-Jin Lee ; Joon-Sung Yang</i>	
<b>RANDOM TESTING OF C COMPILERS BASED ON TEST PROGRAM GENERATION BY EQUIVALENCE TRANSFORMATION</b> .....	676
<i>Kazuhiro Nakamura ; Nagisa Ishiura</i>	
<b>DIGITALLY-ASSISTED GAIN CALIBRATION STRATEGY FOR OPEN-LOOP RESIDUE AMPLIFIERS IN PIPELINE ADCS</b> .....	680
<i>Sarang Kazemina ; Arefeh Soltani</i>	
<b>FPGA IMPLEMENTATION OF HAMMING CODE FOR INCREASING THE FRAME RATE OF CAN COMMUNICATION</b> .....	684
<i>Ronnie O. Serfa Juan ; Min Woo Jeong ; Hyeong Woo Cha ; Hi Seok Kim</i>	
<b>AN ULTRA-LOW POWER CMOS SUBTHRESHOLD VOLTAGE REFERENCE WITHOUT REQUIRING RESISTORS OR BJTS</b> .....	688
<i>Yang Liu ; Chenchang Zhan ; Lidan Wang</i>	
<b>WIDE REAR VEHICLE RECOGNITION USING A FISHEYE LENS CAMERA IMAGE</b> .....	691
<i>Jin-Seong Jeong ; Hyun-Tae Kim ; Bruce Kim ; Sang-Bock Cho</i>	
<b>A LOW POWER RELAXATION OSCILLATOR WITH PROCESS INSENSITIVE AUTO-CALIBRATION SCHEME</b> .....	694
<i>Xin Lu ; Bo Wang ; Zhihuang Wen ; Xiaojin Zhao ; Yuan Cao ; Amine Bermak</i>	
<b>CLOSED-LOOP TRANSFER FUNCTIONS AND FREQUENCY-POINT SPECTRUM SIMULATION OF CCM BUCK CONVERTERS</b> .....	698
<i>Wing-Hung Ki ; Lin Cheng ; Chenchang Zhan</i>	
<b>TEXTURE-BASED FAST CU SIZE DECISION ALGORITHM FOR HEVC INTRA CODING</b> .....	702
<i>Jae Myung Ha ; Jong Hyun Bae ; Myung Hoon Sunwoo</i>	
<b>DC-20 GHZ DIFFERENTIAL TRANSMIT/RECEIVE DP4T SWITCHING MATRIX FOR RADAR-BASED TARGET DETECTION</b> .....	706
<i>A. Azhari ; T. Kikkawa</i>	
<b>LOW-POWER DUAL-PRECISION TABLE-BASED FUNCTION EVALUATION SUPPORTING DYNAMIC PRECISION CHANGES</b> .....	710
<i>Shen-Fu Hsiao ; Kuei-Chun Huang</i>	
<b>TSV-AWARE 3-D IC STRUCTURAL PLANNING WITH IRREGULAR DIE-SIZE</b> .....	713
<i>Arko Dutt ; Pranab Roy ; Hafizur Rahaman</i>	
<b>KKT-CONDITION BASED STUDY ON DVFS FOR HETEROGENEOUS TASK SET</b> .....	717
<i>Mineo Kaneko</i>	
<b>A -34DBM SENSITIVITY BATTERY-LESS WAKE-UP RECEIVER WITH DIGITAL DECODER</b> .....	721
<i>Nagaveni Vamsi ; Sesha Sai Ram Ragulagadda ; Ashudeb Dutta ; Shiv Govind Singh</i>	
<b>CONTRAST ENHANCEMENT USING MULTIPLE MAPPING FUNCTIONS FOR POWER REDUCTION IN OLED DISPLAY</b> .....	725
<i>Chan Young Jang ; Sanghun Kim ; Young Hwan Kim</i>	
<b>TEXT INFORMATION ACQUISITION METHOD OF TRAFFIC SIGNS FOR AUTONOMOUS NAVIGATION</b> .....	727
<i>Hyun-Tae Kim ; Jin-Seong Jeong ; Bruce Kim ; Sang-Bock Cho</i>	
<b>A 0.9V, 3.1–10.6 GHZ CMOS LNA WITH HIGH GAIN AND WIDEBAND INPUT MATCH IN 90 NM CMOS PROCESS</b> .....	730
<i>Sunil Pandey ; P N Kondekar ; Kaushal Nigam ; Dheeraj Sharma</i>	
<b>LIVE DEMONSTRATION: A 128-CHANNEL SPIKE SORTING PROCESSOR FEATURING 0.175 <math>\mu</math>W AND 0.0033 MM<sup>2</sup> PER CHANNEL IN 65-NM CMOS</b> .....	734
<i>Seyed Mohammad Ali Zeinolabedin ; Anh Tuan Do ; Dongsuk Jeon ; Dennis Sylvester ; Tony Tae-Hyoung Kim</i>	
<b>LIVE DEMONSTRATION: MINDS — MESHED AND INTERNET NETWORKED DEVICES SYSTEM FOR SMART HOME: TRACK SELECTION: EMBEDDED SYSTEMS</b> .....	736
<i>Trio Adiono ; Maulana Yusuf Fathany ; Rachmad Vidya Wicaksana Putra ; Khilda Afifah ; Muhammad Husni Santrijaji ; Braham Lawas Lawu ; Syifaul Fuada</i>	
<b>LIVE DEMONSTRATION: MORFPGA DUO PLATFORM WITH DUAL-CAMERA SUPPORT</b> .....	738
<i>Chun-Ming Huang ; Chih-Chyau Yang ; Chien-Ming Wu ; Chun-Wen Cheng ; Chun-Yu Chen ; Yi-Jun Liu</i>	

<b>LIVE DEMONSTRATION: SIGNAL FLOW PLATFORM IMPLEMENTATION INTO RETINAL CELL PATHWAY .....</b>	<b>740</b>
<i>Seunghum Baek ; Jason K. Eshraghian ; Kyoungrok Cho ; Nicolangelo Iannella ; Jun-Ho Kim ; Herbert H. C. Iu ; Tyrone Fernando ; Kamran Eshraghian</i>	
<b>LIVE DEMONSTRATION: MEMRISTOR SYNAPTIC ARRAY WITH FPGA-IMPLEMENTED NEURONS FOR NEUROMORPHIC PATTERN RECOGNITION.....</b>	<b>742</b>
<i>Son Ngoc Truong ; Khoa Van Pham ; Wonsun Yang ; Kyeong-Sik Min ; Yawar Abbas ; Chi Jung Kang</i>	
<b>LIVE DEMONSTRATION: AN FPGA BASED HARDWARE COMPRESSION ACCELERATOR FOR HADOOP SYSTEM.....</b>	<b>744</b>
<i>Sang Muk Lee ; Jung Hwan Oh ; Ji Hoon Jang ; Seong Mo Lee ; Ji Kwang Kim ; Seung Eun Lee</i>	
<b>LIVE DEMONSTRATION: AHB BASED DIGITAL FILTER FOR LOW POWER MOBILE HEALTHCARE SYSTEM.....</b>	<b>746</b>
<i>Oh Seong Gwon ; Ji Kwang Kim ; Jung Woo Shin ; Seung Eun Lee</i>	
<b>LIVE DEMONSTRATION: CAN FD CONTROLLER FOR IN-VEHICLE NETWORK.....</b>	<b>748</b>
<i>Jung Woo Shin ; Jung Hwan Oh ; Sang Muk Lee ; Seung Eun Lee</i>	
<b>Author Index</b>	