

2016 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS 2016)

**Gwalior, India
19-21 December 2016**



**IEEE Catalog Number: CFP16C48-POD
ISBN: 978-1-5090-6171-6**

**Copyright © 2016 by the Institute of Electrical and Electronics Engineers, Inc
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP16C48-POD
ISBN (Print-On-Demand):	978-1-5090-6171-6
ISBN (Online):	978-1-5090-6170-9

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

2016 IEEE International Symposium on Nanoelectronic and Information Systems

iNIS 2016

Table of Contents

Message from the General Chairs	xi
Message from the Technical Program Chairs	xiii
Steering Committee	xv
Organizing Committee	xvi
Technical Program Committee	xviii
Additional Reviewers	xxiv
Keynotes	xxv

Session 01: Graphene Nanoribbon Devices

Modeling of Graphene Nanoribbon Tunnel Field Effect Transistor in Verilog-A for Digital Circuit Design	1
<i>Md. Fahad, Zhou Zhao, Ashok Srivastava, and Lu Peng</i>	
Width-Dependent Characteristics of Graphene Nanoribbon Field Effect Transistor for High Frequency Applications	6
<i>Yaser M. Banadaki and Ashok Srivastava</i>	
Performance Analysis of Top-Contact MLG NR Based Interconnects	11
<i>Ramesh Kumar, Rohit Dhiman, and Rajeevan Chandel</i>	

Session 02: Special Session: Smart and Connected Health

Exploring Human Body Communications for IoT Enabled Ambulatory Health Monitoring Systems	17
<i>Prabha Sundaravadivel, Saraju P. Mohanty, Elias Kougiannos, Venkata P. Yanambaka, and Himanshu Thapliyal</i>	
IoT-Based Fall Detection for Smart Home Environments	23
<i>Shalom Greene, Himanshu Thapliyal, and David Carpenter</i>	

Session 03: Sensor Systems

Ni-CNT as Isopropanol Sensor: Ab-Initio Analysis	29
<i>Sushmita Dandeliya, Md Shahzad Khan, and Anurag Srivastava</i>	
CMOS-Memristor Hybrid Integrated Pixel Sensors	34
<i>Kamilya Smagulova, Aigerim Tankimanova, and Alex Pappachen James</i>	
A Reply Cache Mechanism to Reduce Query Latency of WSN in IoT Sensory Environment	38
<i>Yeduri Sreenivasa Reddy and K. K. Pattanaik</i>	

Session 04: Hardware/Software for Internet of Things and Smart, Connected World

Design and Implementation of Tunable Bandpass Filter for Biomedical Applications	43
<i>B. K. Saurabh, Y. B. Nithin Kumar, Shivnarayan Patidar, and M. H. Vasantha</i>	
A 4X1 High-Definition Transcranial Direct Current Stimulation Device for Targeting Cerebral Micro Vessels and Functionality Using NIRS	47
<i>Gaurav Sharma, Yashika Arora, and Shubhajit Roy Chowdhury</i>	
An Investigation of Power-Performance Aware Accelerator/Core Allocation Challenges in Dark Silicon Heterogeneous Systems	52
<i>Pranshu Kalra, Shaista Hussain, and Nitin Chaturvedi</i>	

Session 05: Hardware for Secure Information Processing

Securing IEEE 1687 Standard On-chip Instrumentation Access Using PUF	56
<i>Sudeendra Kumar K, Naini Satheesh, Abhishek Mahapatra, Sauvagya Sahoo, and K. K. Mahapatra</i>	
Hardware Security Threats to DSP Applications in an IoT Network	62
<i>Azhar Syed and R. Mary Lourde</i>	
Area and Throughput Analysis of Different AES Architectures for FPGA Implementations	67
<i>Disha Yadav and Arvind Rajawat</i>	

Session 06: Special Session: Optimizing Power Converter Technology for Consumer Electronics Devices: An Indian Prospective

Power Converter Systems for Consumer Electronics Devices	72
<i>Santanu K. Mishra</i>	

Session 07: Student Research Forum: Hardware & Security

Graphene Nanoribbon Field Effect Transistor Based Ultra-Low Energy SRAM Design	76
<i>Shital Joshi, Saraju P. Mohanty, Elias Kougianos, and Venkata P. Yanambaka</i>	
Protecting Ownership of Reusable IP Core Generated during High Level Synthesis	80
<i>Deepak Kachave and Anirban Sengupta</i>	

Session 08: Low Power Device Technologies

Performance Analysis of Wavy FinFET and Optimization for Leakage Reduction	83
<i>C. Anju, Nisha Kuruvilla, T. E. Ayoob Khan, and T. A. Shahul Hameed</i>	
Novel Ultra Low Leakage FinFET Based SRAM Cell	89
<i>Vivek Kumar, Vikas Mahor, and Manisha Pattanaik</i>	
Variation Aware Performance Analysis of TFETs for Low-Voltage Computing	93
<i>Vikash Sehwal, Saurav Maji, and Mrigank Sharad</i>	

Session 09: Reliable VLSI Systems

A Quadro Coding Technique to Reduce Self Transitions in VLSI Interconnects	98
<i>Ojashri Sharma, Aakash Saini, Sandeep Saini, and Abhishek Sharma</i>	
An Efficient Approach Targeting Broken Topological Clock Path for Master — Generated Clock Pair	102
<i>Pawan Sehgal, Akhilesh C. Mishra, Rangarajan Ramanujam, and Sujay Deb</i>	
Parametric Performance Analysis of Synchronous and Asynchronous Heterogeneous Network on Chip	108
<i>Ayas Kanta Swain, Anil Kumar Rajput, and Kamalakanta Mahapatra</i>	

Session 10: Emerging Device Technologies

Aromaticity Influence on Electron Transport of Molecular Single Electron Transistor: DFT Investigation	113
<i>Boddepalli Santhi Bhushan, Anurag Srivastava, Jyoti Bhadouria, Rinkoo Bhatia, and Pankaj Mishra</i>	
Proposal of Heterogate Technique for Performance Enhancement of DM-TFET	118
<i>Chaitanya Maradana and Jawar Singh</i>	
Investigation of DC Characteristic on DG-Tunnel FET with High-K Dielectric Using Distinct Device Parameter	124
<i>Shraddha Thakre, Ankur Beohar, Vikas Vijayvargiya, Nandakishor Yadav, and Santosh Kumar Vishvakarma</i>	

Session 11: Special Session: Post CMOS Computing

Post CMOS Computing Beyond Si: DNA Computer as Future Alternative	129
<i>Mayukh Sarkar and Prasun Ghosal</i>	
A Provably Good Method to Generate Good DNA Sequences	134
<i>Swapan Shakhari, Prasun Ghosal, and Mayukh Sarkar</i>	

Session 12: Amplifier Systems

A 60 dB Bulk-Driven Rail-to-Rail Input/Output OTA	139
<i>Abhishek Shrivastava, Ajay Pratap Gangwar, Rahul Kumar, and Rohit Dhiman</i>	
A 0.5V Voltage-Combiner Based Pseudo Differential OTA Design in CMOS Using Weakly Inverted Transistors	144
<i>Antaryami Panigrahi and Abhipsa Parhi</i>	

Mixed-Mode Simulation of Common Emitter Amplifier Design Using Bipolar Charge Plasma Transistor	149
<i>Chitrakant Sahu and Nitesh Agrawal</i>	

Session 13: Cyber Physical Systems and Social Networks

An Edge Contribution-Based Approach to Identify Influential Nodes from Online Social Networks	155
<i>Samya Muhuri, Susanta Chakraborty, and S. K. Setua</i>	
Naïve Bayes Approach for Predicting Missing Links in Ego Networks	161
<i>Anand Kumar Gupta and Neetu Sardana</i>	
A Neural Network-Based Appliance Scheduling Methodology for Smart Homes and Buildings with Multiple Power Sources	166
<i>Raj Mani Shukla, Prasanna Kansakar, and Arslan Munir</i>	

Session 14: Physical Unclonable Functions for Security

Novel FinFET Based Physical Unclonable Functions for Efficient Security Integration in the IoT	172
<i>Venkata P. Yanambaka, Saraju P. Mohanty, and Elias Kougianos</i>	
A Modified RO-PUF with Improved Security Metrics on FPGA	178
<i>Naini Satheesh, Abhishek Mahapatra, Sudeendra Kumar K, Sauvagya Sahoo, and K. K. Mahapatra</i>	
TV-PUF: A Fast Lightweight Analog Physical Unclonable Function	182
<i>Vikash Sehwal and Tanujay Saha</i>	
A Novel Aging Tolerant RO-PUF for Low Power Application	187
<i>Sauvagya Ranjan Sahoo, Sudeendra Kumar, Kamalakanta Mahapatra, and Ayaskanta Swain</i>	

Session 15: Special Session: Turning Software into Hardware — Hastlayer

Turning Software into Hardware — Hastlayer	193
<i>Zoltán Lehóczky, Richárd Tóth, Márk Bartha, András Retzler, Benedek Farkas, and Krisztián Somogyi</i>	

Session 16: Special Session: Modeling and Usage of Nanoscale Process Variations in Emerging Technology

Compact Behavioral Modeling and Time Dependent Performance Degradation Analysis of Junction and Doping Free Transistors	194
<i>Meena Panchore, Jawar Singh, Saraju P. Mohanty, and Elias Kougianos</i>	
Secure Multi-key Generation Using Ring Oscillator Based Physical Unclonable Function	200
<i>Venkata P. Yanambaka, Saraju P. Mohanty, Elias Kougianos, and Jawar Singh</i>	

Session 17: Student Research Forum: Information Communication & IoT

Classification of Non-functional Requirements from SRS Documents Using Thematic Roles	206
<i>Prateek Singh, Deepali Singh, and Ashish Sharma</i>	
A Computation Offloading Scheme Leveraging Parameter Tuning for Real-Time IoT Devices	208
<i>Raj Mani Shukla and Arslan Munir</i>	

Session 18: Quantum and Reversible Technologies

Optical Characteristics of Solution Processed MoO ₂ /ZnO Quantum Dots Based Thin Film Transistor	210
<i>Hemant Kumar, Yogesh Kumar, Gopal Rawat, Chandan Kumar, Bhola N. Pal, and Satyabrata Jit</i>	
Electrical and Optical Characteristics of Pd/ZnO Quantum Dots Based Schottky Photodiode on n-Si	214
<i>Yogesh Kumar, Hemant Kumr, Gopal Rawat, Chandan Kumar, Bhola N. Pal, and S. Jit</i>	
Design of ESOP-RPLA Array Using DRG2 and DRG4 Gates Based on Reversible Logic Technology	218
<i>A. G. Rao and A. K. D. Dwivedi</i>	

Session 19: Special Session: Cyber-Physical Power Systems: Security Threats and Counter Measures

Bid Modification Attack in Smart Grid for Monetary Benefits	224
<i>Kush Khanna, Bijaya Ketan Panigrahi, and Anupam Joshi</i>	

Session 20: Biomedical VLSI Systems

Computing in Ribosomes: Implementing Sequential Circuits Using mRNA-Ribosome System	230
<i>Pratima Chatterjee, Mayukh Sarkar, and Prasun Ghosal</i>	
Memristor Crossbar-Based Pattern Recognition Circuit Using Perceptron Learning Rule	236
<i>Muhammad Khalid and Jawar Singh</i>	
Mathematics Using DNA: Performing GCD and LCM on a DNA Computer	240
<i>Mayukh Sarkar and Prasun Ghosal</i>	

Session 21: Energy-Efficient VLSI Systems

Area and Power-Efficient Timing Error Predictor for Dynamic Voltage and Frequency Scaling Application	244
<i>Govinda Sannena and Bishnu Prasad Das</i>	
LECTOR Based Gated Clock Approach to Design Low Power FSM for Serial Adder	250
<i>Pritam Bhattacharjee and Alak Majumder</i>	
Energy Detection Based Dynamic Spectrum Sensing for 2.4GHz ISM Band	255
<i>Saket Srivastava, Mohammad Hashmi, Supratim Das, and Dibakar Barua</i>	

Session 22: FinFET Devices

Impact of Work Function Fluctuations on Threshold Voltage Variability in a Nanoscale FinFETs	261
<i>Rituraj Singh Rathore, Rajneesh Sharma, and Ashwani K. Rana</i>	
Analysis of Single-Trap-Induced Random Telegraph Noise on Asymmetric High-k Spacer FinFET	264
<i>Nandakishor Yadav, Ankur Beohar, and Santosh K. Vishvakarma</i>	

Low Stand-By Power and Process Variation Tolerant FinFET Based SRAM Cell	268
<i>Akanksha Bhadoria, Mukesh Chaturvedi, Vikas Mahor, and Manisha Pattanaik</i>	
FinFET-Based Low Power Address Decoder under Process Variation	274
<i>Mukesh Chaturvedi, Akanksha Bhadoria, Vikas Mahor, and Manisha Pattanaik</i>	
Session 23: Special Session: An Efficient Design Methodology for CNFET Based Ternary Logic Circuits	
An Efficient Design Methodology for CNFET Based Ternary Logic Circuits	278
<i>Chetan Vudadha, P. Sai Phaneendra, and M. B. Srinivas</i>	
Session 24: Special Session: QSCsim — Charge Based Switched Capacitor Simulator	
QSCsim — Charge Based Switched Capacitor Simulator	284
<i>Binsu J. Kailath and G. Dinesh</i>	
Session 25: IEEE WIE	
Author Index	285