

2016 First International Workshop on Communication Optimizations in HPC (COMHPC 2016)

**Salt Lake City, Utah, USA
18 November 2016**



**IEEE Catalog Number: CFP16J34-POD
ISBN: 978-1-5090-3830-5**

**Copyright © 2016 by the Institute of Electrical and Electronics Engineers, Inc
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP16J34-POD
ISBN (Print-On-Demand):	978-1-5090-3830-5
ISBN (Online):	978-1-5090-3829-9

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

2016 First International Workshop on Communication Optimizations in HPC

COMHPC 2016

Table of Contents

Message from the Workshop Chairs.....	v
Committees.....	vii

Technical Papers

Scalable Hierarchical Aggregation Protocol (SHArP): A Hardware Architecture for Efficient Data Reduction	1
<i>Richard L. Graham, Devendar Bureddy, Pak Lui, Hal Rosenstock, Gilad Shainer, Gil Bloch, Dror Goldenberg, Mike Dubman, Sasha Kotchubievsky, Vladimir Koushnir, Lion Levi, Alex Margolin, Tamir Ronen, Alexander Shpiner, Oded Wertheim, and Eitan Zahavi</i>	
Extending a Message Passing Runtime to Support Partitioned, Global Logical Address Spaces	11
<i>D. Brian Larkins and James Dinan</i>	
Topology-Aware Performance Optimization and Modeling of Adaptive Mesh Refinement Codes for Exascale	17
<i>Cy P Chan, John D Bachan, Joseph P Kenny, Jeremiah J Wilke, Vincent E Beckner, Ann S Almgren, and John B Bell</i>	
Efficient Reliability Support for Hardware Multicast-Based Broadcast in GPU-enabled Streaming Applications	29
<i>C.-H. Chu, K. Hamidouche, H. Subramoni, A. Venkatesh, B. Elton, and D. K. Panda</i>	
Network Topologies and Inevitable Contention	39
<i>Grey Ballard, James Demmel, Andrew Gearhart, Benjamin Lipshitz, Yishai Oltchik, Oded Schwartz, and Sivan Toledo</i>	
DISP: Optimizations towards Scalable MPI Startup	53
<i>Huansong Fu, Swaroop Pophale, Manjunath Gorentla Venkata, and Weikuan Yu</i>	
Topology and Affinity Aware Hierarchical and Distributed Load-Balancing in Charm++	63
<i>Emmanuel Jeannot, Guillaume Mercier, and François Tessier</i>	

Topology-Aware Data Aggregation for Intensive I/O on Large-Scale Supercomputers	73
<i>François Tessier, Preeti Malakar, Venkatram Vishwanath, Emmanuel Jeannot, and Florin Isaila</i>	
Author Index	82