

**2017 30th International
Conference on VLSI Design
and 2017 16th International
Conference on Embedded
Systems (VLSID 2017)**

**Hyderabad, India
7-11 January 2017**



**IEEE Catalog Number: CFP17041-POD
ISBN: 978-1-5090-5741-2**

**Copyright © 2017 by the Institute of Electrical and Electronics Engineers, Inc
All Rights Reserved**

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP17041-POD
ISBN (Print-On-Demand):	978-1-5090-5741-2
ISBN (Online):	978-1-5090-5740-5
ISSN:	1063-9667

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

CURRAN ASSOCIATES INC.
proceedings
.com

2017 30th International Conference on VLSI Design and 2017 16th International Conference on Embedded Systems

VLSID 2017

Table of Contents

Message from the Steering Committee Chair.....	xiv
Message from the General Chair.....	xv
Message from the Technical Program Chairs.....	xvi
Message from the Organizing Chair.....	xvii
Message from the President, VLSI Society of India.....	xviii
Message from Student Conference Chair.....	xix
About the Cover from the Publication Chairs.....	xx
VLSI Design 2016 Conference Steering Committee.....	xxi
VLSI Design 2017 Conference Committee.....	xxii
Advisory Committee.....	xxvi
Technical Program Committee.....	xxvii
Reviewers.....	xxx
VLSI Design Conference History.....	xxxii
Embedded Systems Design Conference History.....	xxxiii
Tutorial T1: 22fdx FDSOI Application towards IOT for Smart Devices.....	xxxiv
Tutorial T2: Memory is Everywhere.....	xxxv
Tutorial T3: Thermal Aware Testing of VLSI Circuits and Systems.....	xxxvi

Tutorial T4: Evolved Supply Set Based UPF Methodology	xxxvii
Tutorial T5: The World beyond DRC: Design for Manufacturing (DFM) - Impact on Yield & Reliability for Advanced Technology Nodes and Their Elucidations	xxxviii
Tutorial T6: High Level Modeling of Digital Circuits	xxxix
Tutorial T7: Designing with Xilinx SDSoC	xl
Tutorial T8: Communication Infrastructure for Future Exascale Processors	xlii
Tutorial T9: Devices and Circuits to Address the Challenges in IOT	xliii
Tutorial T10: Memristors: Technology, Circuit Models and Applications	xliv
Tutorial T11: Design of Energy and Area Efficient Circuits Using Spin Devices in Combination with CMOS	xlv
Tutorial T12: Design, Simulation, Fabrication and Testing of Microwave CMOS Distributed Oscillators, Amplifiers, Noise Cancelling LNA with Temperature Performances and Finally Design of 60 GHz 5G Receiver for Mobile Communication	xlvi
Tutorial T13: Pushing the Envelope on Ultra High Speed SerDes Interfaces	xlvii
Tutorial T14: Privacy Assurance in the IoT World	xlviii

Session A1: Analog, Mixed Signal and RF Design I

Two-Step Residue Transfer Technique for High-Speed Pipeline A/Ds	3
<i>Sudipta Sarkar, Yongda Cai, and Anubhav Adak</i>	
A Low Power Multi-channel Input Delta-Sigma ADC without Reset	9
<i>Ashwin Kumar Siva Kumar, Debasish Behera, and Nagendra Krishnapura</i>	

A Clock Retiming Circuit for Repeaterless Low Swing On-Chip Interconnects	15
<i>Naveen Kadayinti, Maryam Shojaei Baghini, and Dinesh K. Sharma</i>	
On-Chip Non-intrusive Temperature Detection and Compensation of a Fully Integrated CMOS RF Power Amplifier	21
<i>Javed S. Gaggatur, Immanuel Raja, and Gaurab Banerjee</i>	

Session B1: Caches and Memory

Towards a Better Lifetime for Non-volatile Caches in Chip Multiprocessors	29
<i>Sukarn Agarwal and Hemangee K. Kapoor</i>	
An Experimental Study on Dynamic Bank Partitioning of DRAM in Chip Multiprocessors	35
<i>Debiprasanna Sahoo, Manoranjan Satpathy, and Madhu Mutyam</i>	
DyPhase: A Dynamic Phase Change Memory Architecture with Symmetric Write Latency	41
<i>Ishan G. Thakkar and Sudeep Pasricha</i>	
Virtual Two-Port Memory Architecture for Asymmetric Memory Technologies	47
<i>Jiayin Li and Kartik Mohanram</i>	

Session C1: FPGA and Reconfigurable Systems

An FPGA Based High throughput Discrete Kalman Filter Architecture for Real-Time Image Denoising	55
<i>Bibin Johnson, Nimin Thomas, and J. Sheeba Rani</i>	
Efficient Scale Invariant Human Detection Using Histogram of Oriented Gradients for IoT Services	61
<i>D. Sangeetha and P. Deepa</i>	
DFGenTool: A Dataflow Graph Generation Tool for Coarse Grain Reconfigurable Architectures	67
<i>Manideepa Mukherjee, Alexander Fell, and Apala Guha</i>	

Session D1: Low Power I

Towards Controlling Chip Temperature by Dynamic Cache Reconfiguration in Multiprocessors	75
<i>Shounak Chakraborty and Hemangee K. Kapoor</i>	
A 50nW Voltage Monitor Scheme for Minimum Energy Sensor Systems	81
<i>Anand Savanth, Alex Weddell, James Myers, David Flynn, and Bashir Al-Hashimi</i>	
Energy-Efficient Transceiver for Wireless NoC	87
<i>Hemanta Kumar Mondal, Shashwat Kaushik, Sri Harsha Gade, and Sujay Deb</i>	

Session A2: Low Power II

A Single Inductor, Single Input Dual Output (SIDO) Piezoelectric Energy Harvesting System	95
<i>Sumit Naikwad, Murali K. Rajendran, Priya Sunil, and Ashudeb Dutta</i>	
Ultra Low Power Sensor Node for Security Applications, Facilitated by Algorithm-Architecture Co-design	101
<i>Saransh Sharma, Avilash Mukherjee, Abhishek Dongre, and Mrigank Sharad</i>	
Markov Chain Model Using Lévy Flight for VLSI Power Grid Analysis	107
<i>Sukanta Dey, Satyabrata Dash, Sukumar Nandi, and Gaurav Trivedi</i>	

Session B2: VLSI Architectures

Design of Coherence Verification Unit for Heterogeneous CMPs Integrating Update and Invalidate Protocols	115
<i>Bidesh Chakraborty, Mamata Dalui, and Biplab K. Sikdar</i>	
High Performance Integer DCT Architectures for HEVC	121
<i>Mohamed Asan Basiri M. and Noor Mahammad Sk</i>	
Low Complexity and Critical Path Based VLSI Architecture for LMS Adaptive Filter Using Distributed Arithmetic	127
<i>Mphd Tasleem Khan, Shaik Rafi Ahamed, and Forrest Brewer</i>	

Session C2: Test, Reliability and Fault Tolerance I

Accurate Diagnosis of Interconnect Open Defects Based on the Robust Enhanced Aggressor Victim Model	135
<i>Pascal Raiola, Dominik Erb, Sudhakar M. Reddy, and Bernd Becker</i>	
Improved Path Recovery in Pseudo Functional Path Delay Test Using Extended Value Algebra	141
<i>Prasenjit Biswas and D. M. H. Walker</i>	
A Methodology for Trace Signal Selection to Improve Error Detection in Post-Silicon Validation	147
<i>Binod Kumar, Ankit Jindal, Virendra Singh, and Masahiro Fujita</i>	

Session D2: Security I

A Study of Power Supply Variation as a Source of Random Noise	155
<i>Fatemeh Tehranipoor, Nima Karimian, Wei Yan, and John A. Chandy</i>	
Compact Implementations of FPGA-based PUFs with Enhanced Performance	161
<i>N. Nalla Anandakumar, Mohammad S. Hashmi, and Somitra Kumar Sanadhya</i>	

NORA: Algorithmic Balancing without Pre-charge to Thwart Power Analysis Attacks	167
<i>Darshana Jayasinghe, Aleksandar Ignjatovic, and Sri Parameswaran</i>	

Session A3: Analog, Mixed Signal and RF Design II

LNA-LO Co-design Considerations for Low Intermediate Frequency Receivers in 401-406 MHz MedRadio Spectrum for Healthcare Applications	175
<i>Abhishek Srivastava, Nithin Sankar, Devarshi Das, and Maryam Shojaei Baghini</i>	
Optimization of 2.4 GHz CMOS Low Noise Amplifier Using Hybrid Particle Swarm Optimization with Lévy Flight	181
<i>Deepak Joshi, Satyabrata Dash, Ayush Malhotra, Pulimi Venkata Sai, Rahul Das, Dikshit Sharma, and Gaurav Trivedi</i>	
A 6V to 42V High Voltage CMOS Bandgap Reference Robust to RF Interference for Automotive Applications	187
<i>Sanjeev Nyshadham and A. G. Krishna Kanth</i>	
Programmable Output Multi-phase Switched Capacitor Step-Up DC-DC Converter with SAR-based Regulation	193
<i>Mahesh Zanwar and Subhajit Sen</i>	

Session B3: Embedded Systems

High Gain Capacitance Sensor Interface for the Monitoring of Cell Volume Growth	201
<i>Javed S. Gaggatur and Gaurab Banerjee</i>	
DTLB: Deterministic TLB for Tightly Bound Hard Real-Time Systems	207
<i>Kajal Varma, Geeta Patil, and Biju Raveendran</i>	
MAVI: An Embedded Device to Assist Mobility of Visually Impaired	213
<i>Rajesh Kedia, K. K. Yoosuf, Pappireddy Dedeepya, Munib Fazal, Chetan Arora, and M. Balakrishnan</i>	
Migration Aware Low Overhead ERfair Scheduler	219
<i>Anshuman Tripathi, Arnab Sarkar, and P. P. Chakrabarti</i>	

Session C3: Formal Techniques in Design

Dynamic Power Optimization Based on Formal Property Checking of Operations	227
<i>Shrinidhi Udipi, Joakim Urdahl, Dominik Stoffel, and Wolfgang Kunz</i>	
Generating AMS Behavioral Models with Formal Guarantees on Feature Accuracy	233
<i>Antonio Anastasio Bruto Da Costa and Pallab Dasgupta</i>	

Formal Verification of Power Management Logic with Mixed-Signal Domains	239
<i>Sudipa Mandal, Antonio Bruto Da Costa, Aritra Hazra, Pallab Dasgupta, Bhushan Naware, Rama Mohan Chunduri, and Sanjib Basu</i>	

Feature Based Identification of Transmission Line Faults by Synchronous Monitoring of PMUs	245
<i>Antara Ain, Akshay Mambakam, Pallab Dasgupta, and Siddhartha Mukhopadhyay</i>	

Session A4: Analog, Mixed Signal and RF Design III

A High Performance Switchable Multiband Inductor Structure for LC-VCOs	253
<i>R. R. Manikandan and Venkat Narayana Rao Vanukuru</i>	

High Accuracy, Multi-output Bandgap Reference Circuit in 16nm FinFet	259
<i>Sanjay Kumar Wadhwa and Nidhi Chaudhry</i>	

A Novel Design of Compact Broadband Microstrip Directional Coupler with High Directivity	
<i>S. Karthikeyan and B. Ravi Kishore</i>	

A Sub-0.5V Reliability Aware-Negative Bitline Write-Assisted 8T DP-SRAM and WL Strapping Novel Architecture to Counter Dual Patterning Issues in 10nm FinFET	269
<i>Vinay Kumar, Nikhil Puri, Sudhir Kumar, and Sumit Srivastav</i>	

Session B4: Emerging Technologies I

Efficient Binary Basic Linear Algebra Operations on ReRAM Crossbar Arrays	277
<i>Debjyoti Bhattacharjee and Anupam Chattopadhyay</i>	

Extraction and Analysis of Mobility in Double Gate Junctionless Transistor	283
<i>Y. V. Bhuvaneshwari and Abhinav Kranti</i>	

Improved NCV Gate Realization of Arbitrary Size Toffoli Gates	289
<i>Abhoy Kole and Kamalika Datta</i>	

Heuristic Based Majority/Minority Logic Synthesis for Emerging Technologies	295
<i>Vipul Kumar Mishra and Himanshu Thapliyal</i>	

Session C4: Digital Circuits

A 64b/66b Line Encoding for High Speed Serializers	303
<i>Satyajit Mohapatra, Hari Shanker Gupta, Jatindeep Singh, and Nihar Ranjan Mohapatra</i>	

Characterization of a Novel 10T Low-Voltage SRAM Cell with High Read and Write Margin for 20nm FinFET Technology	309
<i>Mitesh Limachia, Pathik Viramgama, Rajesh Thakker, and Nikhil Kothari</i>	

Within-Die Threshold Voltage Variability Estimation Using Reconfigurable Ring Oscillator	315
<i>Poorvi Jain and Bishnu Prasad Das</i>	

Clock Skew Measurement Using an All-Digital Sigma-Delta Time to Digital Converter	321
<i>Mahadev Govind Shirwaikar, Naveen Kadayinti, and Dinesh K. Sharma</i>	

Session A5: Analog, Mixed Signal and RF Design IV

A Switched-Capacitor Amplifier with True Rail-to-Rail Input Range without Using a Rail-to-Rail Op-Amp	329
<i>Anjali Gopinath, Ravi Kumar Adusumalli, Veeresh Babu Vulligaddala, and M. B. Srinivas</i>	

A New Sense Amplifier Design with Improved Input Referred Offset Characteristics for Energy-Efficient SRAM	335
<i>B. S. Reniwal, P. Singh, V. Vijayvargiya, and S. K. Vishvakarma</i>	

A Low-Voltage 13T Latch-Type Sense Amplifier with Regenerative Feedback for Ultra Speed Memory Access	341
<i>Venkatesh Mani Tripathi, Sandeep Mishra, Jyotishman Saikia, and Anup Dandapat</i>	

Frequency Enhancement in Miller Divider with Injection-Locking Portrait	347
<i>Mohammed Umar Shaikh, Sivaramakrishna Rudrapati, Nandish Bharat Thaker, and Shalabh Gupta</i>	

Session B5: Emerging Technologies II

A Novel Approach towards Biochemical Synthesis on Cyberphysical Digital Microfluidic Biochip	355
<i>Sarit Chakraborty and Susanta Chakraborty</i>	

ESD Behavior of AlGaIn/GaN HEMT on Si: Physical Insights, Design Aspects, Cumulative Degradation and Failure Analysis	361
<i>Bhawani Shankar, Ankit Soni, Manikant Singh, Rohith Soman, K. N. Bhat, Srinivasan Raghavan, Navakanta Bhat, and Mayank Shrivastava</i>	

Electrical Modeling and Characterization of Copper/Carbon Nanotubes in Tapered through Silicon Vias	366
<i>Madhav Rao</i>	

Multi-objective Optimization of Placement and Assignment of TSVs in 3D ICs	372
<i>Debasri Saha and Susmita Sur-Kolay</i>	

Session C5: CMOS Technologies I

Modeling of Body-Bias Dependence of Overlap Capacitances in Bulk MOSFETs	381
<i>Avirup Dasgupta, Chetan Gupta, Anupam Dutta, Yen-Kai Lin, Srikanth Srihari, Tamilmani Ethirajan, Chenming Hu, and Yogesh S. Chauhan</i>	
DC Drain Current Model for Tunnel FETs Considering Source and Drain Depletion Regions	385
<i>Rajat Vishnoi, Pratyush Panday, and M. Jagadesh Kumar</i>	
Physics of Current Filamentation in ggNMOS Revisited: Was Our Understanding Scientifically Complete?	391
<i>Milova Paul, Christian Russ, B. Sampath Kumar, Harald Gossner, and Mayank Shrivastava</i>	

Session A6: Test, Reliability and Fault Tolerance II

On Testing of Superscalar Processors in Functional Mode for Delay Faults	397
<i>Nihar Hage, Rohini Gulve, Masahiro Fujita, and Virendra Singh</i>	
Post-Silicon Validation: Automatic Characterization of RF Device Nonidealities via Iterative Learning Experiments on Hardware	403
<i>Barry Muldrey, Sabyasachi Deyati, and Abhijit Chatterjee</i>	
Design and Analysis of Soft-Error Resilience Mechanisms for GPU Register File	409
<i>Sparsh Mittal, Haonan Wang, Adwait Jog, and Jeffrey S. Vetter</i>	

Session B6: Security II

Self Aware SoC Security to Counteract Delay Inducing Hardware Trojans at Runtime	417
<i>Krishnendu Guha, Debasri Saha, and Amlan Chakrabarti</i>	
Hardware Software Codesign for a Hybrid Substitution Box	423
<i>K. B. Anuroop, Anu James, and M. Neema</i>	
A New Logic Encryption Strategy Ensuring Key Interdependency	429
<i>Rajit Karmakar, N. Prasad, Santanu Chattopadhyay, Rohit Kapur, and Indranil Sengupta</i>	

Session C6: CMOS Technologies II

A Systematic Study on the Hysteresis Behaviour and Reliability of MoS ₂ FET	437
<i>Adil Meersha, B. Sathyajit, and Mayank Shrivastava</i>	

Suppressing Single Transistor Latch Effect in Energy Efficient Steep Switching Junctionless MOSFETs	441
<i>Manish Gupta and Abhinav Kranti</i>	
Hybrid OPC Technique for Fast and Accurate Lithography Simulation	447
<i>Pardeep Kumar, S. Srivatsa, P. Mantripragada, S. Upreti, and K. V. Shravya</i>	
Author Index	451