

# **2017 IEEE 8th Latin American Symposium on Circuits & Systems (LASCAS 2017)**

**Bariloche, Argentina  
20-23 February 2017**



**IEEE Catalog Number: CFP17LAS-POD  
ISBN: 978-1-5090-5860-0**

**Copyright © 2017 by the Institute of Electrical and Electronics Engineers, Inc  
All Rights Reserved**

*Copyright and Reprint Permissions:* Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

***\*\*\* This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP17LAS-POD
ISBN (Print-On-Demand):	978-1-5090-5860-0
ISBN (Online):	978-1-5090-5859-4
ISSN:	2330-9954

**Additional Copies of This Publication Are Available From:**

Curran Associates, Inc  
57 Morehouse Lane  
Red Hook, NY 12571 USA  
Phone: (845) 758-0400  
Fax: (845) 758-2633  
E-mail: [curran@proceedings.com](mailto:curran@proceedings.com)  
Web: [www.proceedings.com](http://www.proceedings.com)

CURRAN ASSOCIATES INC.  
**proceedings**  
.com

# TABLE OF CONTENTS

## KEYNOTE

<b>KEYNOTE: INTEGRATED DESIGN-FOR-RELIABILITY FOR ICS</b> .....	iii
<i>A. Wang, F. Lu, Q. Chen, C. Wang, C. Li, F. Zhng</i>	

## PAPERS

<b>4D REVERBERATOR-BASED DIGITAL FILTERS</b> .....	1
<i>M. Kousoulis, C. Coutras, G. Antoniou</i>	
<b>CALIBRATION-LESS NAUTA OTA OPERATING AT 0.25-V POWER SUPPLY IN A 130-NM DIGITAL CMOS PROCESS</b> .....	5
<i>R. Braga, L. Ferreira, G. Colletta, O. Dutra</i>	
<b>DESIGNING AN OPTIMUM NON-DISSIPATIVE LC SNUBBER FOR STEP-UP FLYBACK CONVERTERS IN DCM</b> .....	9
<i>E. Lindstrom, L. Garcia-Rodriguez, A. Oliva, J. Balda</i>	
<b>A LOW-POWER, HIGH-ACCURACY CAPACITANCE-TO-TIME CONVERTER FOR DIFFERENTIAL CAPACITIVE SENSORS</b> .....	13
<i>S. Ogawa</i>	
<b>OSCILLATION-BASED TEST IN A CCH-BASED BANDPASS FILTERS</b> .....	17
<i>P. Petrashin, L. Toledo, W. Lancioni, P. Osuch, T. Stander</i>	
<b>EXPLORING THE VOLTAGE DIVIDER APPROACH FOR ACCURATE MEMRISTOR STATE TUNING</b> .....	21
<i>I. Vourkas, J. Gomez, A. Abusleme, N. Vasileiadis, G. Sirakoulis</i>	
<b>OBJECT IDENTIFICATION USING VSWR EVALUATION BASED ON A NARROWBAND MICROSTRIP ANTENNA AND A TUNED AMPLIFIER</b> .....	25
<i>M. Donatti, L. Manera</i>	
<b>BIASED CAPACITIVE DIVIDER ELECTROSTATIC GENERATORS FOR ENERGY HARVESTING</b> .....	29
<i>A. Queiroz</i>	
<b>A SWITCHED-CAPACITOR FILTER WITH DYNAMIC SWITCHING BIAS OP AMPLIFIERS</b> .....	33
<i>H. Wakaumi</i>	
<b>A VERSATILE, CMOS COMPATIBLE, INTEGRATED ANTENNA FOR MILLIMETER-WAVE APPLICATIONS</b> .....	37
<i>R. Murphy, L. Granados</i>	
<b>EVALUATION OF THE UMODEL FACTORY SOFTWARE USED FOR THE MODELING OF EMBEDDED SYSTEMS WITH CONCURRENT STATES</b> .....	41
<i>M. Prieto, L. Sugezky, N. Gonzalez, M. Giura, Y. Kuo, M. Trujillo, J. Cruz</i>	
<b>ENHANCING I2C ROBUSTNESS TO SOFT ERRORS</b> .....	45
<i>V. Carvalho, F. Kastensmidt</i>	
<b>A 4-WIRE INTERFACE SOC FOR SHARED MULTI-IMPLANT POWER TRANSFER AND FULL-DUPLEX COMMUNICATION</b> .....	49
<i>S. Ghoreishizadeh, D. Haci, Y. Liu, T. Constandinou</i>	
<b>A 0.45 V, 93 PW TEMPERATURE-COMPENSATED CMOS VOLTAGE REFERENCE</b> .....	53
<i>A. Oliveira, D. Cordova, H. Klimach, S. Bampi</i>	
<b>SETTLING TIME-BASED DESIGN OF A FULLY DIFFERENTIAL OTA FOR A SC INTEGRATOR</b> .....	57
<i>D. Calderon-Preciado, F. Sandoval-Ibarra, F. Silveira</i>	
<b>CO-DESIGN SYSTEM FOR TEMPLATE MATCHING USING DEDICATED CO-PROCESSOR AND PARTICLE SWARM OPTIMIZATION</b> .....	61
<i>Y. Tavares, N. Nedjah, L. Mourelle</i>	
<b>HARDWARE IMPLEMENTATION FOR PERMUTATION FUNCTION OF MULTIPLICATION-HARDENED SPONGE BLAMKA</b> .....	65
<i>J. Rossetti, W. Ruggiero</i>	
<b>COMPARATIVE TOPOLOGY AND POWER LOSS STUDY FOR HIGH POWER DENSITY AND HIGH CONVERSION RATIO INTEGRATED SWITCHING POWER CONVERTERS</b> .....	69
<i>K. Wei, D. Ma</i>	
<b>DESIGN OF RESIDUE GENERATORS WITH CLA/COMPRESSOR TREES AND MULTI-BIT EAC</b> .....	73
<i>P. Patronik, S. Piestrak</i>	
<b>A 28GHZ SELF-CONTAINED POWER AMPLIFIER FOR 5G APPLICATIONS IN 28NM FD-SOI CMOS</b> .....	77
<i>B. Moret, V. Knopik, E. Kerherve</i>	
<b>ASYMMETRICAL LENGTH BIASING FOR ENERGY EFFICIENT DIGITAL CIRCUITS</b> .....	81
<i>F. Veirano, F. Silveira, L. Naviner</i>	

<b>SILICON PHOTO-MULTIPLIERS CHARACTERIZATION SYSTEM</b> .....	85
<i>L. Yelos, F. Suarez, M. Bignert, J. Lust, A. Almela, A. Cancio, M. Josebachuili, A. Lucero, A. Mancilla, J. Maya, B. Garcia</i>	
<b>PROCESS AND TEMPERATURE IMPACT ON SINGLE-EVENT TRANSIENTS IN 28NM FDSOI CMOS</b> .....	89
<i>W. Bartra, A. Vladimirescu, R. Reis</i>	
<b>APPLYING LOCKSTEP IN DUAL-CORE ARM CORTEX-A9 TO MITIGATE RADIATION-INDUCED SOFT ERRORS</b> .....	93
<i>A. Oliveira, L. Tambara, F. Kastensmidt</i>	
<b>EVALUATING THE EFFICIENCY OF USING TMR IN THE HIGH-LEVEL SYNTHESIS DESIGN FLOW OF SRAM-BASED FPGA</b> .....	97
<i>A. Santos, L. Tambara, F. Kastensmidt</i>	
<b>FIXED-POINT FPGA IMPLEMENTATION AND OPTIMIZATION FOR HENON MAP CHAOTIC GENERATORS DESIGN</b> .....	101
<i>L. Zhang</i>	
<b>HW/SW CODESIGN OF MAXIMUM LYAPUNOV EXPONENT ESTIMATOR</b> .....	105
<i>L. De Micco, M. Antonelli, M. Crespo, A. Cicuttin</i>	
<b>GOLD-COPPER-BASED BIOSENSOR FOR IMPEDANCE ANALYSIS OF MAMMALIAN ADHERENT CELLS</b> .....	109
<i>F. Giana, F. Bonetto, M. Bellotti</i>	
<b>A CHOPPED FRONT-END SYSTEM WITH COMMON-MODE FEEDBACK FOR REAL TIME ECG APPLICATIONS</b> .....	113
<i>P. Gardella, E. Fernandez, E. Baez, J. Cesaretti</i>	
<b>NONRECURSIVE COMB-BASED STRUCTURE FOR POWER OF THREE DECIMATION FACTORS: DESIGN AND FPGA IMPLEMENTATION</b> .....	117
<i>G. Dolecek, R. Baez</i>	
<b>RISC-V BASED ASP SOUND CLASSIFIER INTENDED FOR ACOUSTIC SURVEILLANCE IN PROTECTED NATURAL ENVIRONMENTS</b> .....	121
<i>C. Salazar-Garcia, R. Castro-Gonzalez, A. Chacon-Rodriguez</i>	
<b>EVALUATION OF MULTIPLE BIT UPSET TOLERANT CODES FOR NOCS BUFFERING</b> .....	125
<i>F. Silva, W. Magalhaes, J. Silveira, J. Ferreira, P. Magalhaes, O. Lima, C. Marcon</i>	
<b>EFFICIENT USE OF GAIN-BANDWIDTH PRODUCT IN ACTIVE FILTERS: GM-C AND ACTIVE-R ALTERNATIVES</b> .....	129
<i>A. Sanabria-Borbon, E. Sanchez-Sinencio</i>	
<b>FILTERED-X ERROR CODED AFFINE PROJECTION ALGORITHM WITH EVOLVING ORDER FOR ACTIVE NOISE CONTROL</b> .....	133
<i>A. Rodriguez, J. Avalos, J. Sanchez</i>	
<b>A STUDY OF CHARACTERIZING CROSSTALK EFFECTS IN 3-D VIAS</b> .....	137
<i>S. Harb, W. Eisenstadt</i>	
<b>RADIATION SENSITIVITY OF XOR TOPOLOGIES IN MULTIGATE TECHNOLOGIES UNDER VOLTAGE VARIABILITY</b> .....	141
<i>Y. Aquiar, C. Meinhardt, R. Reis</i>	
<b>APPROXIMATE FREQUENT ITEMSETS MINING ON DATA STREAMS USING HASHING AND LEXICOGRAPHIC ORDER IN HARDWARE</b> .....	145
<i>L. Bustio-Martinez, R. Cumplido, M. Letras-Luna, R. Hernandez-Leon, J. Bande-Serrano</i>	
<b>HIGH-FREQUENCY MEMRISTIVE SYNAPSES</b> .....	149
<i>I. Carro-Perez, H. Gonzalez-Hernandez, C. Sanchez-Lopez</i>	
<b>STATISTICAL LIBRARY CHARACTERIZATION USING ARBITRARY POLYNOMIAL CHAOS</b> .....	153
<i>M. Ince, S. Ozev, S. Vrudhula</i>	
<b>IMPROVING A MOSFET MODEL FOR DESIGN BY HAND</b> .....	157
<i>A. Costa, B. Alves, S. Soares</i>	
<b>RECONFIGURABLE MULTIPLE-GAIN ACTIVE-RECTIFIER FOR MAXIMUM EFFICIENCY POINT TRACKING IN WPT</b> .....	161
<i>P. Perez-Nicoli, F. Silveira</i>	
<b>BEARINGS-ONLY AERIAL SHOOTER LOCALIZATION USING A MICROPHONE ARRAY MOUNTED ON A DRONE</b> .....	165
<i>R. Fernandes, J. Apolinario, A. Ramos</i>	
<b>FPGA IMPLEMENTATION OF A FEEDFORWARD NEURAL NETWORK-BASED CLASSIFIER USING THE XQUANT TECHNIQUE</b> .....	169
<i>E. Machado, T. Marques, C. Llanos, R. Coral, R. Jacobi</i>	
<b>BLIND RANGE LEVEL SHIFTERS FROM 0 TO 18V</b> .....	173
<i>J. Gak, M. Miguez, A. Arnaud, P. Mandolesi</i>	

<b>A COMPARISON OF FOUR PDE-SPATIAL DENOISING SYSTEMS FOR MOLECULAR IMAGES.....</b>	177
<i>S. Lahmiri, M. Boukadoum</i>	
<b>A 2.2 UW ANALOG FRONT-END FOR MULTICHANNEL NEURAL RECORDING.....</b>	181
<i>J. Valtierra, M. Delgado-Restituto, A. Rodriguez-Vazquez</i>	
<b>A HIGH IP3 6.5 MW SELF-BIASED 0.3 - 3 GHZ SMALL AREA LNA .....</b>	185
<i>A. Costa, H. Klimach, S. Bampi</i>	
<b>DOUBLE QUADRATURE BANDPASS SAMPLING FOR A PLL AND MIXER-LESS LOW-IF MULTISTANDARD RECEIVER.....</b>	189
<i>G. Sionek, L. Lolis, J. Cunha, M. Matia, S A. Mariano, B. Leite</i>	
<b>ENERGY EVALUATION OF THE HEVC DECODING FOR DIFFERENT ENCODING CONFIGURATIONS .....</b>	193
<i>D. Correa, D. Palomino, L. Agostini, B. Zatt</i>	
<b>A 5UA WIRELESS PLATFORM FOR CATTLE HEAT DETECTION.....</b>	197
<i>B. Bellini, A. Arnaud</i>	
<b>A SMALL-SIGNAL AVERAGED MODEL OF A COUPLED-INDUCTOR BOOST CONVERTER.....</b>	201
<i>M. D'Amico, S. Gonzalez</i>	
<b>PORTABLE ELECTROMAGNETIC FIELD APPLICATOR FOR MAGNETIC HYPERTHERMIA EXPERIMENTS.....</b>	205
<i>S. Gonzalez, E. Spinelli, A. Veiga, D. Coral, M. Van Raap, P. Zelis, G. Pasquevich, F. Sanchez</i>	
<b>LOW POWER SUM OF ABSOLUTE DIFFERENCES ARCHITECTURE USING NOVEL HYBRID ADDER.....</b>	209
<i>R. Ferreira, B. Silveira, M. Fonseca, C. Diniz, E. Costa</i>	
<b>LOW COST ROLLBACK TO IMPROVE FAULT-TOLERANCE IN VLSI CIRCUITS.....</b>	213
<i>T. Bonnoit, N. Zergainoh, M. Nicolaidis, R. Velazco</i>	
<b>COEXISTENCE OF SOLUTIONS IN A BOOST-FLYBACK CONVERTER WITH CURRENT MODE CONTROL.....</b>	217
<i>J. Munoz, G. Gallo, F. Angulo, G. Osorio</i>	
<b>A COMPACT FPGA-BASED MICROCODED COPROCESSOR FOR EXPONENTIATION IN ASYMMETRIC ENCRYPTION .....</b>	221
<i>L. Rodriguez-Flores, M. Morales-Sandoval, R. Cumplido, C. Feregrino-Uribe, I. Algreto-Badillo</i>	
<b>ALL DIGITAL RECONFIGURABLE IR-UWB PULSE GENERATOR USING BPSK MODULATION IN 130NM RF-CMOS PROCESS .....</b>	225
<i>L. Moreira, G. Novaes, E. Rios, J. Neto, T. Ferauche</i>	
<b>CHARACTERIZING ENERGY CONSUMPTION IN SOFTWARE HEVC ENCODERS: HM VS X265.....</b>	229
<i>I. Machado, W. Penny, M. Porto, L. Agostini, B. Zatt</i>	
<b>ASPECTS ON THE SHAPE DEPENDENCE WITH ENERGY OF POINT-LIKE EVENTS IN HIGH RESISTIVITY CCDS.....</b>	233
<i>G. Moroni, M. Haro, J. Tiffenberg, E. Paolini, J. Estrada, X. Bertou, G. Cancelo</i>	
<b>A 90% EFFICIENCY 60 MW MPPT SWITCHED CAPACITOR DC - DC CONVERTER FOR PHOTOVOLTAIC ENERGY HARVESTING AIMING FOR IOT APPLICATIONS.....</b>	237
<i>R. Zamparetti, H. Klimach, S. Bampi</i>	
<b>ADHERENCE OF A HIGH-SPEED RRP LDMOS CHARACTERIZATION SETUP TO JESD 24-10 STANDARD.....</b>	241
<i>C. Bernal, M. Jimenez</i>	
<b>EXPLOITING ADDITION SCHEMES FOR THE IMPROVEMENT OF OPTIMIZED RADIX-2 AND RADIX-4 FFT BUTTERFLIES.....</b>	245
<i>R. Neuenfeld, M. Fonseca, E. Costa, J. Oses</i>	
<b>DESIGN OF EXPERIMENTS IMPLEMENTATION TOWARDS OPTIMIZATION OF POWER DISTRIBUTION NETWORKS .....</b>	249
<i>F. Leal-Romo, J. Rayas-Sanchez, J. He</i>	
<b>A COMPARISON OF ASYNCHRONOUS QDI TEMPLATES USING STATIC LOGIC .....</b>	253
<i>R. Guazzelli, M. Moreira, N. Calazans</i>	
<b>HIGH DENSITY EMERGING RESISTIVE MEMORIES: WHAT ARE THE LIMITS?.....</b>	257
<i>A. Levisse, G. Giraud, J. Noel, M. Moreau, J. Portal</i>	
<b>STUDIES OF DYNAMICS OF MEMRISTOR-BAASED MEMORY CELLS.....</b>	261
<i>B. Garda, M. Ogorzalek, K. Kasinski, Z. Galias</i>	
<b>ANALOG MEMRISTIVE AND MEMCAPACITIVE PROPERTIES OF TI / AL<sub>2</sub>O<sub>3</sub> / NB<sub>2</sub>O<sub>5</sub> / TI RESISTIVE SWITCHES.....</b>	265
<i>S. Slesazek, H. Wylezich, T. Mikolajick</i>	

**OPTIMIZATION OPPORTUNITIES IN RRAM-BASED FPGA ARCHITECTURES** ..... 269

*X. Tang, G. Micheli, P.-E. Gaillardon*

**Author Index**