2017 IEEE 28th International Conference on Application-specific Systems, Architectures and Processors (ASAP 2017)

Seattle, Washington, USA
10 – 12 July 2017

IEEE

IEEE Catalog Number: CFP17063-POD
ISBN: 978-1-5090-4826-7

****** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.***

IEEE Catalog Number:	CFP17063-POD
ISBN (Print-On-Demand):	978-1-5090-4826-7
ISBN (Online):	978-1-5090-4825-0
ISSN:	2160-0511

Additional Copies of This Publication Are Available From:

Curran Associates, Inc
57 Morehouse Lane
Red Hook, NY 12571 USA
Phone: (845) 758-0400
Fax: (845) 758-2633
E-mail: curran@proceedings.com
Web: www.proceedings.com

ASAP 2017 Table of Contents

Message from the General Chair and Program Chair vii

Organizing Committee viii

Program Committee ix

Additional Reviewers x

Keynotes xi

Program Overview xii

Technical Papers

SESSION 1 - Machine Learning

CATERPILLAR: Coarse Grain Reconfigurable Architecture for Accelerating the Training of Deep Neural Networks 1
Yuanfang Li and Ardavan Pedram

Fast and Efficient Implementation of Convolutional Neural Networks on FPGA 11
Abhinav Podili, Chi Zhang and Viktor Prasanna

Parallel Multi Channel Convolution using General Matrix Multiplication - Short Paper 19
Aravind Vasudevan, Andrew Anderson and David Gregg

High-Performance FPGA Implementation of Equivariant Adaptive Separation via Independence Algorithm for Independent Component Analysis - Short Paper 25
Mahdi Nazemi, Shahin Nazarian and Massoud Pedram

SESSION 2 - Security

Design and Comparative Evaluation of GPGPU- and FPGA-based MPSoC ECU Architectures for Secure, Dependable, and Real-Time Automotive CPS 29
Bikash Poudel, Naresh Giri and Arslan Munir

High-Level Synthesis for Side-Channel Defense 37
Sven Tenzing Choden Konigsmark, Deming Chen and Martin Wong

DoSGuard: Protecting Pipelined MPSoCs Against Hardware Trojan Based DoS Attacks 45
Amin Malekpour, Roshan Ragel, Aleksandar Ignjatovic and Sri Parameswaran

Hardwiring the OS Kernel into a Java Application Processor 53
Chun-Jen Tsai, Cheng-Ju Lin, Cheng-Yang Chen, Yan-Hung Lin, Wei-Jhong Ji and Sheng-Di Hong

Hardware Support for Embedded Operating System Security - Short Paper 61
Arman Pouraghily, Tilman Wolf and Russell Tessier

SESSION 3 - Image Processing

Hardware-accelerated CCD Readout Smear Correction for Fast Solar Polarimeter 67
Stefan Tabel, Korbinian Weikl and Walter Stechele

Real-time Object Detection in Software with Custom Vector Instructions and Algorithm Changes 75
Joe Edwards and Guy G. F. Lemiuex

SESSION 4 - Memory/Storage

An Efficient Embedded Multi-Ported Memory Architecture for Next-Generation FPGAs 83
S. Navid Shahrouzi and Darshika G. Perera

A Staged Memory Resource Management Method for CMP Systems 91
Yangguo Liu, Junlin Lu, Dong Tong and Xu Cheng

CFStore: Boosting Hybrid Storage Performance by Device Crossfire 99
Wei Zhou, Dan Feng and Zhipeng Tan

RVNet: a Fast and High Energy Efficiency Network Packet Processing System on RISC-V - Short Paper 107
Yanpeng Wang, Mei Wen, Chunyuan Zhang and Jie Lin

SESSION 5 - High Performance Computing

Massive Spatial Query on the Kepler Architecture 111
Yili Gong, Jia Tang, Wenhai Li and Zihui Ye

PFSI.sw: A Programming Framework for Sea Ice Model Algorithms Based on Sunway Many-core Processor 119
Binyang Li, Bo Li and Depei Qian

MicRun: A Framework for Scale-free Graph Algorithms on SIMD Architecture of the Xeon Phi 127
Jie Lin, Qingbo Wu, Yusong Tan, Jie Yu, Qi Zhang, Xiaoling Li, and Lei Luo

Hierarchical Dataflow Model for Efficient Programming of Clustered Many-Core Processors - Short Paper 137
Julien Hascoët, Karol Desnos, Jean-François Nezan and Benoît Dupont de Dinechin

Modeling and Evaluation for Gather/Scatter Operations in Vector-SIMD Architectures - Short Paper 143
Hongbing Tan, Sheng Liu, Haiyan Chen and Wu jianguo

reMinMin: A Novel Static Energy-Centric List Scheduling Approach Based on Real Measurements - Short Paper 149
Achim Lösch and Marco Platzner

SESSION 6 - Digital Signal Processing

Hardware Design and Analysis of Efficient Loop Coarsening and Border Handling for Image Processing 155
M. Akif Oezkan, Oliver Reiche, Frank Hannig and Jürgen Teich

High performance hardware architectures for Intra Block Copy and Palette Coding for HEVC Screen Content Coding extension - Short Paper 164
Rishan Senanayake, Namitha Liyanage, Sasindu Wijeratne, Sachille Atapattu, Kasun Athukorala, P.M.K. Tharaka, Geethan Karunaratne, R.M.A.U. Senarath, Ishantha Perera, Ashen Ekanayake and Ajith Pasqual

Design and Implementation of Adaptive Signal Processing Systems Using Markov Decision Processes - Short Paper 170
Lin Li, Adrian Sapio, Jiahao Wu, Yanzhou Liu, Kyunghun Lee, Marilyn Wolf and Shuvra Bhattacharyya

SESSION 7 - Control Systems and Parallel Programming Languages

An Embedded Scalable Linear Model Predictive Hardware-based Controller using ADMM 176
Pei Zhang, Joseph Zambreno and Phillip H. Jones

CGRA-ME: A Unified Framework for CGRA Modelling and Exploration - Short Paper 184
S. Alexander Chin , Noriaki Sakamotoy, Allan Rui , Jim Zhao, Jin Hee Kim , Yuko Hara-Azumiy and Jason Anderson

OpenCL-Based Design Pattern for Line Rate Packet Processing - Short Paper 190
Jehandad Khan, Peter Athanas, Skip Booth and John Marshall

Acceleration of Frequent Itemset Mining on FPGA Using SDAccel and Vivado HLS - Short Paper 195
Vinh Dang and Kevin Skadron

OpenMP Device Offloading to FPGA Accelerators - Short Paper 201
Lukas Sommer, Jens Korinth and Andreas Koch

Posters

SESSION 1

DeepPump: Multi-Pumping Deep Neural Networks 206
Ruizhe Zhao, Tim Todman, Wayne Luk and Xinyu Niu

Efficiency in ILP Processing by Using Orthogonality 207
Marcel Brand, Frank Hannig, Alexandru Tanase and Jürgen Teich

A Fast and Accurate Logarithm Accelerator for Scientific Applications 208
Jing Chen and Xue Liu

Model Checking Cloud Rendering System for the QoS Evaluation 209
Haoyu Liu, Huahu Xu, Honghao Gao, Minjie Bian and Danqi Chu

SESSION 2

High-throughput Area-efficient Processor for 3GPP LTE Cryptographic Core Algorithms 210
Yuanhong Huo 1 and Dake Liu2

KV-FTL: A Novel Key-Value Based FTL Scheme for Large Scale SSDs 211
Juan Li, Zhengguo Chen, Zhiguang Chen, Nong Xiao and Fang Liu

Author Index 213