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**Trantenna: Monolithic Transistor-Antenna Device for Real-Time THz Imaging System**, M. W. Ryu, R. Patel, S. H. Ahn, H. J. Jeon, M. S. Choe, E. Choi, K. J. Han and K. R. Kim, UNIST, Korea

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**T11-5 - 17:40**

**(Late News) Comparison of Key Fine-Line BEOL Metallization Schemes for Beyond 7 nm Node**, T. Nogami\*, X. Zhang\*\*, J. Kelly\*, B. Briggs\*, H. You\*\*, R. Patlolla\*, H. Huang\*, P. McLaughlin\*, J. Lee\*, H. Shobha\*, S. Nguyen\*, S. DeVries\*, J. Demarest\*, G. Lian\*, J. Li\*, J. Maniscalco\*, P. Bhosale\*, X. Lin\*\*, B. Peethala\*, N. Lanzillo\*, T. Kane\*, C. C. Yang\*, K. Motoyama\*, D. Sil\*, T. Spooner\*, D. Canaperi\*, T. Standaert\*, S. Lian\*\*, A. Grill\*, D. Edelstein\* and V. Paruchuri\*, \*IBM Research, \*\*GLOBALFOUNDRIES, \*\*\*Samsung Electronics Inc., USA

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**SESSION 12 - Ferroelectric [Shunju I]**

Wednesday, June 7, 16:00-17:40

Chairpersons: B. H. Lee, Gwangju Institute of Science and Technology  
S. Salahuddin, Univ. of California, Berkeley

**T12-1 - 16:00**

**Nano-Scaled Ge FinFETs with Low Temperature Ferroelectric HfZrO<sub>x</sub> on Specific Interfacial Layers Exhibiting 65% S.S. Reduction and Improved I<sub>ON</sub>**, C.-J. Su\*, Y.-T. Tang\*, Y.-C. Tsou\*\*, P.-J. Sung\*\*\*\*, F.-J. Hou\*, C.-J. Wang\*, S.-T. Chung\*\*\*, C.-Y. Hsieh\*\*\*\*, Y.-S. Yeh\*, F.-K. Hsueh\*\*\*\*, K.-H. Kao\*\*, S.-S. Chuang\*\*\*, C.-T. Wu\*, T.-Y. You\*, Y.-L. Jian\*, T.-H. Chou\*, Y.-L. Shen\*, B.-Y. Chen\*, G.-L. Luo\*, T.-C. Hong\*\*, K.-P. Huang\*\*\*\*, M.-C. Chen\*, Y.-J. Lee\*, T.-S. Chao\*\*\*, T.-Y. Tseng\*\*\*, W.-F. Wu\*, G.-W. Huang\*, J.-M. Shieh\*, W.-K. Yeh\* and Y.-H. Wang\*\*\*\*, \*National Nano Device Laboratories, \*\*National Cheng Kung Univ., \*\*\*National Chiao Tung Univ., \*\*\*\*National Sun Yat-Sen Univ., \*\*\*\*\*Industrial Technology Research Institute and \*\*\*\*\*National Applied Research Laboratories, Taiwan

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**T12-2 - 16:25**

**Impact of Total and Partial Dipole Switching on the Switching Slope of Gate-Last Negative Capacitance FETs with Ferroelectric Hafnium Zirconium Oxide Gate Stack**, P. Sharma\*, K. Tapily\*\*, A. K. Saha\*\*\*, J. Zhang\*, A. Shaughnessy\*, A. Aziz\*\*\*, G. L. Snider\*, S. Gupta\*\*\*, R. D. Clark\*\* and S. Datta\*, \*Univ. of Notre Dame, \*\*TEL Technology Centre, America and \*\*\*Penn State Univ., USA

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**T12-3 - 16:50**

**A Nonvolatile SRAM Integrated with Ferroelectric HfO<sub>2</sub> Capacitor for Normally-Off and Ultralow Power IoT Application**, M. Kobayashi, N. Ueyama and T. Hiramoto, The Univ. of Tokyo, Japan

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**T12-4 - 17:15**

**First Demonstration of Vertically Stacked Ferroelectric Al Doped HfO<sub>2</sub> Devices for NAND Applications**, K. Florent\*\*, S. Lavizzari\*\*, L. Di Piazza\*\*, M. Popovici\*\*, E. Vecchio\*\*, G. Potoms\*\*, G. Groeseneken\*\*\* and J. Van Houdt\*\*\*, \*KU Leuven and \*\*imec, Belgium

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**Technology / Circuits Joint Focus Session 3****Ultra Low Power for IoT [Shunju II, III]**

Thursday, June 8, 8:30-10:10

Chairpersons: M. Tada, NEC Corp.  
L. Bair, AMD

- JFS3-1 - 8:30 (Invited)**  
**Computing Platform for Automotive Electronics of Automated Driving Generation**, H. Sugimoto, DENSO Corp., Japan **122**
- JFS3-2 - 8:55 (Invited)**  
**Semiconductor Platforms for Ultra Low Power IoT Solutions**, T. Dry and T. Letavic, GLOBALFOUNDRIES, USA **124**
- JFS3-3 - 9:20**  
**Performance Boost of Crystalline In-Ga-Zn-O Material and Transistor with Extremely Low Leakage for IoT Normally-Off CPU Application**, S. H. Wu\*, X. Y. Jia\*, X. Li\*, C. C. Shuai\*, H. C. Lin\*, M. C. Lu\*, T. H. Wu\*, M. Y. Liu\*, J. Y. Wu\*, D. Matsubayashi\*\*, K. Kato\*\* and S. Yamazaki\*\*, \*United Microelectronics Corporation, Singapore and \*\*Semiconductor Energy Laboratory Co., Ltd., Japan **126**
- JFS3-4 - 9:45**  
**A 65 nm 1.0 V 1.84 ns Silicon-On-Thin-Box (SOTB) Embedded SRAM with 13.72 nW/Mbit Standby Power for Smart IoT**, M. Yabuuchi\*, K. Nii\*, S. Tanaka\*, Y. Shinozaki\*\*, Y. Yamamoto\*, T. Hasegawa\*, H. Shinkawata\* and S. Kamohara\*, \*Renesas Electronics Corp. and \*\*Nippon Systemware Co. Ltd., Japan **128**
- SESSION 13 - Quantum Neuromorphic Computing [Shunju I]**  
Thursday, June 8, 8:30-10:10  
Chairpersons: K. Endo, AIST  
G. Jurczak, ASM
- T13-1 - 8:30**  
**Towards Quantum Computing in Si MOS Technology: Single-Shot Readout of Spin States in a FDSOI Split-Gate Device with Built-In Charge Detector**, M. Urdampilleta\*, L. Hutin\*\*, B. Jadot\*, B. Bertrand\*\*, H. Bohuslavskyj\*\*\*\*, R. Maurand\*\*\*, S. Barraud\*\*, C. Bäuerle\*, M. Sanquer\*\*\*, X. Jehl\*\*\*, S. De Franceschi\*\*\*, T. Meunier\* and M. Vinet\*\*, \*Institut Néel, \*\*CEA-LETI and \*\*\*CEA, INAC-PHELIQS, France **130**
- T13-2 - 8:55**  
**Achieving Ideal Accuracies in Analog Neuromorphic Computing Using Periodic Carry**, S. Agarwal, R. B. J. Gedrim, A. H. Hsia, D. R. Hughart, E. J. Fuller, A. A. Talin, C. D. James, S. J. Plimpton and M. J. Marinella, Sandia National Laboratories, USA **132**
- T13-3 - 9:20**  
**Novel Ferroelectric FET Based Synapse for Neuromorphic Systems**, H. Mulaosmanovic\*, J. Ocker\*, S. Müller\*, M. Noack\*, J. Müller\*\*, P. Polakowski\*\*, T. Mikolajick\*\*\*\* and S. Slesazek\*, \*NaMLab gGmbH, \*\*Fraunhofer IPMS and \*\*\*IHM TU Dresden, Germany **134**
- T13-4 - 9:45**  
**Design-Technology Co-Optimization for OxRRAM-Based Synaptic Processing Unit**, A. Mallik\*, D. Garbin\*, A. Fantini\*, D. Rodopoulos\*, R. Degraeve\*, J. Stuijt\*\*, A. K. Das\*\*, S. Schaafsma\*\*, P. Debacker\*, G. Donadio\*, H. Hody\*, L. Goux\*, G. S. Kar\*, A. Furnemont\*, A. Mocuta\* and P. Raghavan\*, \*imec-BE, Belgium and \*\*imec-NL, The Netherlands **136**

**Technology / Circuits Joint Focus Session 4**  
**Computing Beyond Von Neumann [Shunju II, III]**

Thursday, June 8, 10:30-12:10

Chairpersons: M. Kobayashi, The Univ. of Tokyo  
M. Vinet, CEA-LETI, MINATEC

- JFS4-1 - 10:30 (Invited)**  
**Implementation Challenges for Scalable Neuromorphic Computing**, S. Yamamichi, A. Horibe, T. Aoki, K. Hosokawa, T. Hisada and H. Mori, IBM Research, Japan **138**
- JFS4-2 - 10:55 (Invited)**  
**Distributed Quantum Computing Systems: Technology to Quantum Circuits**, R. Van Meter, Keio Univ., Japan **140**
- JFS4-3 - 11:20**  
**Ultra-Low Power Probabilistic IMT Neurons for Stochastic Sampling Machines**, M. Jerry\*, A. Parihar\*\*, B. Grisafe\*, A. Raychowdhury\*\* and S. Datta\*, \*Univ. of Notre Dame and \*\*Georgia Institute of Technology, USA **142**
- JFS4-4 - 11:45**  
**A 462GOPS/J RRAM-Based Nonvolatile Intelligent Processor for Energy Harvesting IoT System Featuring Nonvolatile Logics and Processing-In-Memory**, F. Su\*, W.-H. Chen\*\*, L. Xia\*, C.-P. Lo\*\*, T. Tang\*, Z. Wang\*, K.-H. Hsu\*\*, M. Cheng\*, J.-Y. Li\*\*, Y. Xie\*\*\*, Y. Wang\*, M.-F. Chang\*\*, H. Yang\* and Y. Liu\*, \*Tsinghua Univ., China, \*\*National Tsing Hua Univ., Taiwan and \*\*\*Univ. of California, Santa Barbara, USA **144**
- SESSION 14 - SiGe / Ge FET 2 [Shunju I]**  
Thursday, June 8, 10:30-12:10  
Chairpersons: S. Takagi, The Univ. of Tokyo  
T. Palacios, Massachusetts Institute of Technology
- T14-1 - 10:30**  
**First Experimental Observation of Channel Thickness Scaling (Down to 3 nm) Induced Mobility Enhancement in UTB GeOI nMOSFETs**, W. H. Chang, T. Irisawa, H. Ishii, H. Hattori, H. Ota, H. Takagi, Y. Kurashima, N. Uchida and T. Maeda, AIST, Japan **146**
- T14-2 - 10:55**  
**Strained Germanium Gate-All-Around PMOS Device Demonstration Using Selective Wire Release Etch Prior to Replacement Metal Gate Deposition**, L. Witters\*, F. Sebaai\*, A. Hikavy\*, A. P. Milenin\*, R. Loo\*, A. De Keersgieter\*, G. Eneman\*, T. Schram\*, K. Wostyn\*, K. Devriendt\*, A. Schulze\*, R. Lieten\*\*, S. Bilodeau\*\*, E. Cooper\*\*, P. Storck\*\*\*, C. Vrancken\*, H. Arimura\*, P. Favia\*, E. Vancoille\*, J. Mitard\*, R. Langer\*, A. Opdebeeck\*, F. Holsteyns\*, N. Waldron\*, K. Barla\*, V. De Heyn\*, D. Mocuta\* and N. Collaert\*, \*imec, \*\*Entegris, Inc. and \*\*\*Siltronic AG, Belgium **148**
- T14-3 - 11:20**  
**Performance and Electrostatic Improvement by High-Pressure Anneal on Si-Passivated Strained Ge pFinFET and Gate All Around Devices with Superior NBTI Reliability**, H. Arimura\*, L. Witters\*, D. Cott\*, H. Dekkers\*, R. Loo\*, J. Mitard\*, L.-Å. Ragnarsson\*, K. Wostyn\*, G. Boccardi\*, E. Chiu\*\*, A. Subirats\*, P. Favia\*, E. Vancoille\*, V. De Heyn\*, D. Mocuta\* and N. Collaert\*, \*imec, Belgium and \*\*Poongsan Corp., USA **150**

**T14-4 - 11:45**

**The First GeSn FinFET on a Novel GeSnOI Substrate Achieving Lowest S of 79 mV/decade and Record High  $G_{m,int}$  of 807  $\mu\text{S}/\mu\text{m}$  for GeSn P-FETs**, D. Lei\*, K. H. Lee\*\*, S. Bao\*\*.\*, W. Wang\*, S. Masudy-Panah\*, S. Yadav\*, A. Kumar\*, Y. Dong\*, Y. Kang\*, S. Xu\*, Y. Wu\*, Y.-C. Huang\*\*\*\*, H. Chung\*\*\*\*, S. S. Chu\*\*\*\*, S. Kuppurao\*\*\*\*, C. S. Tan\*\*\*\*, X. Gong\* and Y.-C. Yeo\*\*\*\*\*, \*National Univ. of Singapore, \*\*Singapore MIT Alliance for Research and Technology, \*\*\*Nanyang Technological Univ., Singapore, \*\*\*\*Applied Materials, USA and \*\*\*\*\*Currently with TSMC, Taiwan

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**Luncheon Talk [Suzaku I]**

Thursday, June 8, 12:40-14:00

Organizers: M. Ikeda, The Univ. of Tokyo  
M. Masahara, AIST**Approach to Develop Prosthetic Technology as a Part of Body**, K. Endo, Xiborg**SESSION 15 - Memory 2 Flash MRAM [Shunju II, III]**

Thursday, June 8, 14:00-15:40

Chairpersons: H.-T. Lue, Macronix International Co., Ltd.  
N. Ramaswamy, Micron Technology, Inc.**T15-1 - 14:00**

**High-Speed and Logic-Compatible Split-Gate Embedded Flash on 28-nm Low-Power HKMG Logic Process**, Y. K. Lee, C. Jeon, H. Min, B. Seo, K. Kim, D. Kim, K. Min, J. S. Woo, H. Kang, Y. S. Chung, M. Kim, J. Jang, K. S. Yeom, J.-S. Kim, M. H. Oh, H. Lee, S. Cho and D. Lee, Samsung Electronics Co., Ltd., Korea

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**T15-2 - 14:25**

**First Demonstration of Diode-Type 3-D NAND Flash Memory String Having Super-Steep Switching Slope**, N. Choi, H.-J. Kang, S. Chung, S.-H. Bae, B.-G. Park and J.-H. Lee, Seoul National Univ. and SK hynix Inc., Korea

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**T15-3 - 14:50**

**Flash Reliability Boost Huffman Coding (FRBH): Co-Optimization of Data Compression and  $V_{TH}$  Distribution Modulation to Enhance Data-Retention Time by Over 2900x**, Y. Deguchi, A. Kobayashi, H. Watanabe and K. Takeuchi, Chuo Univ., Japan

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**T15-4 - 15:15**

**CMOS-Embedded STT-MRAM Arrays in 2x nm Nodes for GP-MCU Applications**, D. Shum\*, D. Houssameddine\*, S. T. Woo\*, Y. S. You\*, J. Wong\*, K. W. Wong\*, C. C. Wang\*, K. H. Lee\*, K. Yamane\*, V. B. Naik\*, C. S. Seet\*, T. Tahmasebi\*, C. Hai\*, H. W. Yang\*, N. Thiagarajah\*, R. Chao\*, J. W. Ting\*, N. L. Chung\*, T. Ling\*, T. H. Chan\*, S. Y. Siah\*, R. Nair\*, S. Deshpande\*\*, R. Whig\*\*, K. Nagel\*\*, S. Aggarwal\*\*, M. DeHerrera\*\*, J. Janesky\*\*, M. Lin\*\*, H.-J. Chia\*\*, M. Hossain\*\*, H. Lu\*\*, S. Ikegawa\*\*, F. B. Mancoff\*\*, G. Shimon\*\*, J. M. Slaughter\*\*, J. J. Sun\*\*, M. Tran\*\*, S. M. Alam\*\* and T. Andre\*\*, \*GLOBALFOUNDRIES Singapore Pte, Ltd., Singapore and \*\*Everspin Technologies, Inc., USA

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**SESSION 16 - Process [Shunju I]**

Thursday, June 8, 14:00-15:40

Chairpersons: T. Miyashita, Toshiba Corp.  
C. Mazure, Soitec Group**T16-1 - 14:00**

**Dual Beam Laser Annealing for Contact Resistance Reduction and Its Impact on VLSI Integrated Circuit Variability**, Z. Liu\*, O. Gluschenkov\*, H. Niimi\*\*, B. Liu\*\*, J. Li\*, J. Demarest\*, S. Mochizuki\*, P. Adusumilli\*, M. Raymond\*\*, A. Carr\*, S. Chen\*\*\*, Y. Wang\*\*\*, H. Jagannathan\* and T. Yamashita\*, \*IBM Research, \*\*GLOBALFOUNDRIES and \*\*\*Ultratech Inc, USA

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**T16-2 - 14:25**

**Sub-10<sup>-9</sup>  $\Omega\cdot\text{cm}^2$  Contact Resistivity on p-SiGe Achieved by Ga Doping and Nanosecond Laser Activation**, J.-L. Everaert\*, M. Schaeckers\*, H. Yu\*\*\*, L.-L. Wang\*\*\*\*\*, A. Hikavy\*, L. Date\*\*\*\*, J. del Agua Bornique\*\*\*\*, K. Hollar\*\*\*\*, F. A. Khaja\*\*\*\*, W. Aderhold\*\*\*\*, A. J. Mayur\*\*\*\*, J. Y. Lee\*\*\*\*, H. van Meer\*\*\*\*, Y.-L. Jiang\*\*\*, K. De Meyer\*\*\*, D. Mocuta\* and N. Horiguchi\*, \*imec, \*\*KU Leuven, Belgium, \*\*\*Fudan Univ., China and \*\*\*\*Applied Materials, USA

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**T16-3 - 14:50**

**Highly-Selective Superconformal CVD Ti Silicide Process Enabling Area-Enhanced Contacts for Next-Generation CMOS Architectures**, N. Breil\*, A. Carr\*\*, T. Kuratomi\*, C. Lavoie\*\*, I.-C. Chen\*, M. Stolfi\*, K. D. Chiu\*, W. Wang\*\*, H. Van Meer\*, S. Sharma\*, R. Hung\*, A. Gelatos\*, J. Jordan-Sweet\*\*, E. Levrau\*\*, N. Loubet\*\*, R. Chao\*\*, J. Ye\*, A. Ozcan\*\*, C. Surisetty\*\* and M. Chudzik\*, \*Applied Materials and \*\*IBM Research, USA

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**T16-4 - 15:15**

**Record Low Specific Contact Resistivity ( $1.2 \times 10^{-9} \Omega\cdot\text{cm}^2$ ) for P-Type Semiconductors: Incorporation of Sn into Ge and In-Situ Ga Doping**, Y. Wu\*, S. Luo\*, W. Wang\*, S. Masudy-Panah\*, D. Lei\*, X. Gong\*, G. Liang\* and Y.-C. Yeo\*\*\*, \*National Univ. of Singapore, Singapore and \*\*Currently with TSMC, Taiwan

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**SESSION 17 - CMOS Integration II [Shunju II, III]**

Thursday, June 8, 16:00-18:05

Chairpersons: K. Tateiwa, TowerJazz Panasonic Semiconductor Co., Ltd.  
S.-C. Song, Qualcomm Inc.**T17-1 - 16:00**

**Low-Variation SRAM Bitcells in 22nm FDSOI Technology**, V. Joshi, H. Ramamurthy, S. Balasubramanian, S. Seo, H. Yoon, X. Zou, N. Chan, J. Yun, T. Klick, E. Smith, J. Schmid, R. van Bentum, J. Faul and C. Weintraub, GLOBALFOUNDRIES, USA

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**T17-2 - 16:25**

**Impact of Strain on Access Resistance in Planar and Nanowire CMOS Devices**, R. Berthelon\*\*\*\*\*, F. Andrieu\*, F. Triozon\*, M. Cassé\*, L. Bourdet\*, G. Ghibaudo\*\*\*\*, D. Rideau\*\*, Y. M. Niquet\*\*, S. Barraud\*, P. Nguyen\*, C. Le Royer\*, J. Lacord\*, C. Tabone\*, O. Rozeau\*, D. Dutartre\*\*, A. Clavier\*\*\*, E. Josse\*\*, F. Arnaud\*\* and M. Vinet\*, \*CEA-LETI, \*\*STMicroelectronics, \*\*\*CEMES and \*\*\*\*IMEP-LaHC, France

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**T17-3 - 16:50**

**Key Process Steps for High Performance and Reliable 3D Sequential Integration**, C.-M. V. Lu\*\*\*, F. Deprat\*, C. Fenouillet-Beranger\*, P. Batude\*, X. Garros\*, A. Tsiara\*, C. Leroux\*, R. Gassilloud\*, D. Nouguiet\*\*, D. Ney\*\*, X. Federspiel\*\*, P. Besombes\*, A. Toffoli\*, G. Romano\*\*\*, N. Rambal\*, V. Delaye\*, D. Barge\*\*, M.-P. Samson\*\*\*, B. Previtali\*, C. Tabone\*, L. Pasini\*\*\*, L. Brunet\*, F. Andrieu\*, J. Micoud\*, T. Skotnicki\*\* and M. Vinet\*, \*CEA-LETI and \*\*STMicroelectronics, France

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**T17-4 - 17:15**

**Influence of Stress Induced CT Local Layout Effect (LLE) on 14nm FinFET**, P. Zhao, S. M. Pandey, E. Banghart, X. He, R. Asra, V. Mahajan, H. Zhang, B. Zhu, K. Yamada, L. Cao, P. Balasubramanian, M. Joshi, M. Eller, F. Benistant and S. Samavedam, GLOBALFOUNDRIES, USA

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**Stacked Nanosheet Gate-All-Around Transistor to Enable Scaling Beyond FinFET**, N. Loubet\*, T. Hook\*, P. Montanini\*, C.-W. Yeung\*, S. Kanakasabapathy\*, M. Guillorn\*, T. Yamashita\*, J. Zhang\*, X. Miao\*, J. Wang\*, A. Young\*, R. Chao\*, M. Kang\*\*, Z. Liu\*, S. Fan\*, B. Hamieh\*, S. Sieg\*, Y. Mignot\*, W. Xu\*, S.-C. Seo\*, J. Yoo\*\*, S. Mochizuki\*, M. Sankarapandian\*, O. Kwon\*\*, A. Carr\*, A. Greene\*, Y. Park\*\*, J. Frougier\*\*\*, R. Galatage\*\*\*, R. Bao\*, J. Shearer\*, R. Conti\*, H. Song\*\*, D. Lee\*\*, D. Kong\*, Y. Xu\*, A. Arceo\*, Z. Bi\*, P. Xu\*, R. Muthinti\*, J. Li\*, R. Wong\*, D. Brown\*\*\*, P. Oldiges\*, R. Robison\*, J. Arnold\*, N. Felix\*, S. Skordas\*, J. Gaudiello\*, T. Standaert\*, H. Jagannathan\*, D. Corliss\*, M.-H. Na\*, A. Knorr\*\*\*, T. Wu\*, D. Gupta\*, S. Lian\*\*, R. Divakaruni\*, T. Gow\*, C. Labelle\*\*\*, S. Lee\*\*, V. Paruchuri\*, H. Bu\* and M. Khare\*, \*IBM, \*\*Samsung Electronics Co., Ltd., \*\*\*GLOBALFOUNDRIES, USA