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Organizers: M. Ikeda, The Univ. of Tokyo
M. Masahara, AIST**Approach to Develop Prosthetic Technology as a Part of Body**, K. Endo, Xiborg**SESSION 22 - Circuits Focus Session - Advanced Sensing Systems [Suzaku III]**

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Chairpersons: Y. Oike, Sony Semiconductor Solutions Corp.
H. Lee, Google**C22-1 - 14:00****320x240 Back-Illuminated 10µm CAPD Pixels for High Speed Modulation Time-of-Flight CMOS Image Sensor**, Y. Kato*, T. Sano*, Y. Moriyama*, S. Maeda*, T. Yamazaki*, A. Nose*, K. Shina*, Y. Yasu*, W. van der Tempel**, A. Ercan** and Y. Ebiko*, *Sony Semiconductor Solutions Corp., Japan and **SoftKinetic, Belgium 222**C22-2 - 14:25****An Imager Using 2-D Single-Photon Avalanche Diode Array in 0.18-µm CMOS for Automotive LIDAR Application**, H. Akita*, I. Takai**, K. Azuma*, T. Hata* and N. Ozaki*, *DENSO Corp. and **Toyota Central R&D Labs., Inc., Japan 224**C22-3 - 14:50****A 16.5 Giga Events/s 1024 × 8 SPAD Line Sensor with Per-Pixel Zoomable 50ps-6.4ns/bin Histogramming TDC**, A. T. Erdogan, R. Walker, N. Finlayson, N. Krstajić, G. O. S. Williams and R. K. Henderson, Univ. of Edinburgh, UK 226**C22-4 - 15:15****A 272.49 pJ/pixel CMOS Image Sensor with Embedded Object Detection and Bio-Inspired 2D Optic Flow Generation for Nano-Air-Vehicle Navigation**, K. Lee, S. Park, S.-Y. Park, J. Cho and E. Yoon, Univ. of Michigan, USA 228**SESSION 23 - High-Speed and Power Efficient Wireless Transceivers [Suzaku II]**

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A. Molnar, Cornell Univ.**C23-1 - 14:00****A 100mW 3.0 Gb/s Spectrum Efficient 60 GHz Bi-Phase OOK CMOS Transceiver**, Y. Wang*, B. Liu*, H. Liu*, A. T. Narayanan*, J. Pang*, N. Li*, T. Yoshioka*, Y. Terashima*, H. Zhang*, D. Tang*, M. Katsuragi*, D. Lee**, S. Choi**, R. Wu*, K. Okada* and A. Matsuzawa*, *Tokyo Institute of Technology, Japan and **Samsung Electronics Co., Ltd., Korea 230**C23-2 - 14:25****A 230-260GHz Wideband Amplifier in 65nm CMOS Based on Dual-Peak G_{max} -Core**, D.-W. Park*, D. R. Utomo*, J.-P. Hong** and S.-G. Lee*, *KAIST and **CBNU, Korea 232**C23-3 - 14:50****A 65nm CMOS I/Q RF Power DAC with 24 - 42dB 3rd Harmonic Cancellation and up to 18dB Mixed-Signal Filtering**, B. Yang, E. Y. Chang, A. Niknejad, B. Nikolić and E. Alon, Univ. of California, Berkeley, USA 234**C23-4 - 15:15****A 43%-Efficiency 20dBm Sub-GHz Transmitter Employing Rise-Edge-Synchronized Harmonic Calibration with 33.3% Duty Cycle**, M. Mizokami*, T. Uozumi*, Y. Yamashita**, K. Shibata* and H. Sato*, *Renesas Electronics Corp. and **Renesas System Design Co., Ltd., Japan 236**SESSION 24 - Physical Sensors [Suzaku III]**

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B. Ginsburg, Texas Instruments**C24-1 - 16:00****A 10.1” 56-Channel, 183 uW/electrode, 0.73 mm²/sensor High SNR 3D Hover Sensor Based on Enhanced Signal Refining and Fine Error Calibrating Techniques**, Y. Huh*, S.-W. Hong**, S.-H. Park*, J.-S. Bang*, C. Park**, S. Park**, H.-D. Gwon*, S.-U. Shin*, H. Shin*, S.-W. Choi*, Y.-M. Ju*, J.-H. Lee* and G.-H. Cho*, *KAIST and **Samsung Electronics Co., Ltd., Korea 238**C24-2 - 16:25****A Robust and Versatile, -40°C to +180°C, 8Sps to 1kSps, Multi Power Source Wireless Sensor System for Aeronautic Applications**, R. Grezard*, L. Sibeud*, F. Lepin*, J. Willemin*, J.-C. Riou** and B. Gomez*, *CEA-LETI and **SAFRAN Electronics & Defense, France 240**C24-3 - 16:50****A 6×5×4mm³ General Purpose Audio Sensor Node with a 4.7µW Audio Processing IC**, M. Cho*, S. Oh*, S. Jeong*, Y. Zhang*, I. Lee*, Y. Kim*, L.-X. Chuo*, D. Kim*, Q. Dong*, Y.-P. Chen*, M. Lim**, M. Daneman**, D. Blaauw*, D. Sylvester* and H.-S. Kim*, *Univ. of Michigan and **Invensense, USA 242**C24-4 - 17:15****A 4.7µW Switched-Bias MEMS Microphone Pre-amplifier for Ultra-Low-Power Voice Interfaces**, S. Oh, T. Jang, K. D. Choo, D. Blaauw and D. Sylvester, Univ. of Michigan, USA 244

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Chairpersons: K. Sunaga, NEC Corp.
B. Casper, Intel Corp.**C25-1 - 16:00****A 32Gb/s, 4.7pJ/bit Optical Link with -11.7dBm Sensitivity in 14nm FinFET CMOS**, J. Proesel*, Z. Deniz*, A. Cevrero**, I. Ozkaya**, S. Kim*, D. Kuchta*, S. Lee***, S. Rylov*, H. Ainspan*, T. Dickson*, J. Bulzacchelli* and M. Meghelli*, *IBM T. J. Watson Research Center, USA, **IBM Research, Switzerland and ***IBM Systems, USA

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C25-2 - 16:25**A 60 Gb/s 1.9 Pj/bit NRZ Optical-Receiver with Low Latency Digital CDR in 14nm CMOS FinFET**, A. Cevrero*, I. Ozkaya***, P. A. Francesc*, C. Menolfi*, M. Braendli*, T. Morf*, D. Kuchta**, M. Kossel*, L. Kull*, D. Luu*, J. Proesel**, Y. Leblebici*** and T. Toifl*, *IBM Research, Switzerland, **IBM Research, USA and ***EPFL, Switzerland

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C25-4 - 17:15**A 26-Gb/s 8.1-mW Receiver with Linear Sampling Phase Detector for Data and Edge Equalization**, Y. Wang***, Z. Li*, J. Zhuang***, C. Zhi*** and C. P. Yue*, *The Hong Kong Univ. of Science and Technology, China, **Xilinx Inc., Singapore and ***Brite Semiconductor, China

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C25-5 - 17:40**A 28.05Gb/s Transceiver Using Quarter-Rate Triple-Speculation Hybrid-DFE Receiver with Calibrated Sampling Phases in 32nm CMOS**, G. Gangasani*, J. F. Bulzacchelli**, M. Wielgos*, W. Kelly*, V. Sharma***, A. Prati***, G. Cervelli***, D. Gardellini***, M. Baecher*, M. Shannon*, T. Beukema**, J. Garlett*, H. H. Xu*, T. Toifl***, M. Meghelli**, J. Ewen* and D. Storaska*, *GLOBALFOUNDRIES, **IBM Research, USA, ***Miromico and ****IBM Research, Switzerland

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SESSION 26 - Processors and SoC [Suzaku I]

Thursday, June 8, 16:00-18:05

Chairpersons: M. Hashimoto, Osaka Univ.
J. Wu, AMD**C26-1 - 16:00****A 501mW 7.61Gb/s Integrated Message-Passing Detector and Decoder for Polar-Coded Massive MIMO Systems**, Y.-T. Chen*, C.-C. Cheng**, T.-L. Tsai**, W.-C. Sun**, Y.-L. Ueng** and C.-H. Yang***, *National Chiao Tung Univ., **National Tsing Hua Univ. and ***National Taiwan Univ., Taiwan

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C26-2 - 16:25**A 12.4pJ/cycle Sub-Threshold, 16pJ/cycle Near-Threshold ARM Cortex-M0+ MCU with Autonomous SRPG/DVFS and Temperature Tracking Clocks**, J. Myers, A. Savanth, P. Prabhat, S. Yang, R. Gaddh, S. O. Toh and D. Flynn, ARM Ltd., UK

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C26-3 - 16:50**A 2.267 Gbps, 93.7pJ/b Non-Binary LDPC Decoder for Storage Applications**, Y. Toriyama and D. Marković, Univ. of California, Los Angeles, USA

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C26-4 - 17:15**A 130nm FeRAM-Based Parallel Recovery Nonvolatile SOC for Normally-OFF Operations with 3.9x Faster Running Speed and 11x Higher Energy Efficiency Using Fast Power-On Detection and Nonvolatile Radio Controller**, Z. Wang*, F. Su*, Y. Wang*, Z. Li*, X. Li*, R. Yoshimura**, T. Naiki**, T. Tsuwa**, T. Saito**, Z. Wang**, K. Taniuchi**, M.-F. Chang***, H. Yang* and Y. Liu*, *Tsinghua Univ., China, **Rohm Co., Ltd., Japan and ***National Tsing Hua Univ., Taiwan

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C26-5 - 17:40**A Battery-Less 507nW SoC with Integrated Platform Power Manager and SiP Interfaces**, F. Yahya*, C. J. Lukas*, J. Breiholz*, A. Roy*, H. N. Patel*, N. Liu*, X. Chen**, A. Kosari**, S. Li*, D. Akella*, O. Ayorinde*, D. Wentzloff** and B. H. Calhoun*, *Univ. of Virginia and **Univ. of Michigan, USA

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Technology SESSION 6 - Highlight [Shunju I, II, III]

Wednesday, June 7, 8:30-10:10

Chairpersons: Y.-C. Yeo, TSMC
W. Rachmady, Intel Corp.**T6-1 - 8:30****Highly Manufacturable 7nm FinFET Technology Featuring EUV Lithography for Low Power and High Performance Applications**, D. Ha, C. Yang, J. Lee, S. Lee, S. H. Lee, K.-I. Seo, H. S. Oh, E. C. Hwang, S. W. Do, S. C. Park, M.-C. Sun, D. H. Kim, J. H. Lee, M. I. Kang, S.-S. Ha, D. Y. Choi, H. Jun, H. J. Shin, Y. J. Kim, J. Lee, C. W. Moon, Y. W. Cho, S. H. Park, Y. Son, J. Y. Park, B. C. Lee, C. Kim, Y. M. Oh, J. S. Park, S. S. Kim, M. C. Kim, K. H. Hwang, S. W. Nam, S. Maeda, D.-W. Kim, J.-H. Lee, M. S. Liang and E. S. Jung, Samsung Electronics Co., Ltd., Korea

N/A

T6-2 - 8:55**10nm High Performance Mobile SoC Design and Technology Co-Developed for Performance, Power, and Area Scaling**, S. Yang*, Y. Liu*, M. Cai*, J. Bao*, P. Feng*, X. Chen*, L. Ge*, J. Yuan*, J. Choi*, P. Liu*, Y. Suh*, H. Wang*, J. Deng*, Y. Gao*, J. Yang*, X.-Y. Wang*, D. Yang*, J. Zhu*, P. Penzes*, S. C. Song*, C. Park**, S. Kim**, J. Kim**, S. Kang**, E. Terzioglu*, K. Rim* and P. C. Chidambaram*, *Qualcomm Technologies Inc., USA and **Samsung Electronics Co., Ltd., Korea

N/A

T6-3 - 9:20**First Demonstration of Flash RRAM on Pure CMOS Logic 14nm FinFET Platform Featuring Excellent Immunity to Sneak-Path and MLC Capability**, E. R. Hsieh*, Y. C. Kuo**, C. H. Cheng*, J. L. Kuo*, M. R. Jiang*, J. L. Lin*, H. W. Cheng*, S. S. Chung*, C. H. Liu**, T. P. Chen***, Y. H. Yeah***, T. J. Chen*** and O. Cheng***, *National Chiao Tung Univ., **National Taiwan Normal Univ. and ***United Microelectronics Corp., Taiwan

N/A

T6-4 - 9:45**First Demonstration of 3D SRAM Through 3D Monolithic Integration of InGaAs n-FinFETs on FDSOI Si CMOS with Inter-Layer Contacts**, V. Deshpande*, H. Hahn*, E. O'Connor*, Y. Baumgartner*, M. Sousa*, D. Caimi*, H. Boutry**, J. Widiez**, L. Brévard**, C. Le Royer**, M. Vinet**, J. Fompeyrine* and L. Czornomaz*, *IBM Research, Switzerland and **CEA-LETI, France

N/A