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Chair: Jin Liu, *University of Texas at Dallas*
Co-Chair: Donald Lie, *Texas Tech University*
Time: Monday, August 7, 2017, 10:20 - 12:00
Location: Braker Hall 001

A Time-Resolved CMOS Image Sensor with High Conversion-Gain Pixels and Pipelined ADCs 1
Song Chen (Dartmouth College), Eric R. Fossum (Dartmouth College)

This paper presents a CMOS image sensor with high conversion-gain pixels and column-shared pipelined ADCs for Fluorescence-lifetime imaging microscopy (FLIM). Pixel conversion gain of 121 uV/e- is achieved by creating a distal floating diffusion from transfer gate and reset transistor gate without any process modification. 32-channel 10-bit on-chip column-shared pipelined ADCs with sampling rate up to 5MS/s are designed using area-efficient ring amplifiers for the sensor readout. The ring amplifiers are designed based on actively-biased technique which reduces the area further by 40%. This image sensor chip is fabricated in a standard 180nm CMOS image sensor (CIS) process.

Phased Arrays in Wireless Power Transfer 5
Jerry Lopez (NoiseFigure Research / Texas Tech University), Jerry Tsay (Texas Tech University), Bernabe A. Guzman (Texas Tech University), Jill Mayeda (NoiseFigure Research / Texas Tech University), Donald Y.C. Lie (Texas Tech University)

The recent increase in RFID usage coupled with the evolving IoT has revamped the need for Wireless Power Transfer (WPT). In this paper, a brief review of systems using WPT is offered including RFIDs, inductively coupled systems and electromagnetic harvesters. A case study for phased array antenna beamforming and its benefits to wireless power transfer is given. A 3x linear patch array at 5.8GHz is designed and measured. Also, a 5.8GHz SOI CMOS based integrated harvester circuit is designed and measured to showcase the possible advancement of WPT at higher frequencies using directive power in the 5G network spectrum

A Multi-Loop Low-Dropout FVF Voltage Regulator with Enhanced Load Regulation 9
Mahender Manda (New Mexico State University), Sri Harsh Pakala (New Mexico State University), Paul M. Furth (New Mexico State University)

This paper introduces a multi-loop fast transient response flipped voltage follower (FVF) low-dropout (LDO) voltage regulator suitable for system-on-chip (SOC) applications. While typical FVF-based LDOs exhibit fast transient response, which is critical for SOC applications, their output DC accuracy is limited due to low loop gain of the FVF. In this work, we introduce a multi-loop design aimed at improving the DC accuracy while preserving the transient performance. The LDO is implemented in a 180 nm CMOS process to provide an output voltage of 1.5 V at a maximum load current of 10 mA froman input line voltage of 1.8 V. The designed LDO's quiescent current is 53μA at minimum load. Simulation results showcase the advantages of the multi-loop design with a transient response time of 0.73 ns and a figure of merit (FOM) of 3.9 ps.

A Short Survey on Recent Highly Efficient cm-Wave 5G Linear Power Amplifier Design 13
D.Y.C. Lie (Texas Tech University), J.C. Mayeda (Texas Tech University), J. Lopez (Texas Tech University / NoiseFigure Research LLC)

The 5G wireless revolution will bring some fundamental changes on the design of handsets and communication infrastructures, delivering over 10 Gbps download speed with unprecedented densely connected wireless devices. The 5G RF transmitters using phased-array MIMO (multiple-input and multiple-output) antennas will demand excellent power efficiency with high integration and linearity at the cm-Wave/mm-Wave frequencies, making the design of highly efficient and linear 5G power amplifier (PA) one of the most challenging tasks for RF IC designers. As the cm-Wave 5G systems will probably be deployed in the market earlier than their mm-Wave counterparts, we will survey in this paper some latest development on 15 GHz and 28 GHz 5G cm-Wave PA design.

On the Analysis of Low Output Impedance Characteristic of Flipped Voltage Follower (FVF) and FVF LDOs 17
Punith R. Surkanti (New Mexico State University), Annajirao Garimella (New Mexico State University), Mahender Manda (New Mexico State University), Paul M. Furth (New Mexico State University)

The flipped voltage follower (FVF), a variant of the common-drain transistor amplifier, comprising local feedback, finds application in circuits such as voltage buffers, current mirrors, class AB amplifiers, frequency compensation circuits and low dropout voltage regulators (LDOs), among others. One of the important characteristics of the FVF, which makes the circuit desirable, is its low output impedance. In this tutorial-flavored paper, we perform a theoretical analysis of the transfer function, poles and zeros of the output impedance of the FVF and correlate it with transistor-level simulation results. Utilization of the FVF and its variants has wide application in the analog, mixed-signal and power management circuit design space.

Session A1L-B: System Architectures

Chair: Soumyajit Mandal, *Case Western Reserve University*
Co-Chair: John McNeill, *Worcester Polytechnic Institute*
Time: Monday, August 7, 2017, 10:20 - 12:00
Location: Eaton Hall 201

Recent Advances in Analog/RF Interference Mitigation for Massive MIMO Receivers 21
Linxiao Zhang (Columbia University), Harish Krishnaswamy (Columbia University)

Digital MIMO receivers featuring digitization at each element are critical for (massive) MIMO applications since they support complex space-time signal processing. However, the lack of spatial selectivity in the analog/RF do- main necessitates high-dynamic-range analog-to-digital con- verters (A/Ds) to accommodate the uneven spatial power distribution, limiting the scale of such MIMO systems. This paper reviews analog/RF spatial filtering techniques that have been proposed in recent years to address this problem. A scalable spatial notch suppression technique allows the synthesis of a steerable spatial notch, which eliminates the strongest in-band spatial block in the analog/RF domain. The spatial notch is synthesized in the baseband, and the impedance transparency of passive mixers is used to translate the notch to the antenna interface. In a second prototype, a more general arbitrary spatial filter (ASF) adaptively filters the spatial domain signals to equalize the power levels across all directions. Current mode operation ensures superior linearity and ultra-wideband spatial suppression. Measurements from CMOS prototypes have been provided to verify the claims.

µLeech: A Side-Channel Evaluation Platform for IoT 25
Michael Moukarzel (Worcester Polytechnic Institute), Thomas Eisenbarth (Worcester Polytechnic Institute), Berk Sunar (Worcester Polytechnic Institute)

We propose uLeech, a new embedded trusted platform module for next generation power scavenging devices. Such power scavenging devices are already widely deployed. For instance, the Square point-of-sale reader uses the microphone/speaker interface of a smartphone for communications and as power supply. While such devices are used as trusted devices in security critical applications in the wild, they have not been properly evaluated yet. uLeech can securely store keys and provide cryptographic services to any connected smart phone. Our design also facilitates physical security analysis by providing interfaces to facilitate acquisition of power traces and clock manipulation attacks. Thus uLeech empowers security researchers to analyze leakage in next generation embedded and IoT devices and to evaluate countermeasures before deployment.

Continuous-Time Algorithms for Solving the Electromagnetic Wave Equation in Analog ICs 29
Nilan Udayanga (University of Akron), Arjuna Madanayake (University of Akron), S.I. Hariharan (University of Akron)

A method that replaces the temporal partial differential operators of a partial differential equation (PDE) with Laplace domain impedances is proposed for realizing analog circuits that solve the wave equation. A systolic array of analog circuit modules is employed to simulate electromagnetic wave propagation. Mathematical models and corresponding analog circuits are described for internal and boundary modules in the systolic array. Dirichlet, Neumann, and radiation boundary conditions are considered. The system is simulated using ideal circuits in Cadence Spectre. Signal flow graphs and transfer functions for 1-D wave equation solvers are obtained. Errors associated with the analog wave equation solver is quantified by comparing the results with a MATLAB based finite difference time domain simulation. Finally, the case where multiple medium boundaries is present is analyzed.

Compact and Voltage-Scalable Sensor for Accurate Thermal Sensing in Dynamic Thermal Management 33
Teng Yang (Columbia University), Pavan K. Chundi (Columbia University), Seongjong Kim (Columbia University), Eren Kursun (Columbia University), Martha Kim (Columbia University), Peter R. Kinget (Columbia University), Mingoo Seok (Columbia University)

In this paper, we present a sensor circuit that is compact and deeply voltage-scalable and can be embedded among digital cells with little disruption. Simulation results show that it achieves a comparable accuracy to other compact sensor circuits for DTM.

Analog Limitations for High-Speed Digital Radios: Where the Bits Stop Working 37
David S. Ricketts (North Carolina State University)

Fundamental physical constraints, such as noise and channel capacity, set an upper bound to theoretical performance of many systems. In this work we examine the limitations of high-speed data in modern digital wireless radio systems. Although physical constraints provide an ultimate limit, we show that signal-to-noise-plus-distortion-ratio (SNDR) and nonlinearity of modern CMOS and Bipolar technologies limit current performance well before physical limitations. By examining several example circuit topologies used in data conversion in digital radios, we show that 3rd order harmonics HD3 likely set the practical barrier to high data rates at SNDRs above 40 dB and sampling rates above 20 GS/s.

Session A1L-C: MEMS and NEMS

Chair: Cristian Cassella, *Northeastern University*
Co-Chair: Robert A. Lake, *Air Force Institute of Technology*
Time: Monday, August 7, 2017, 10:20 - 12:00
Location: Eaton Hall 202

A Programmable Sustaining Amplifier for Reconfigurable MEMS-Referenced Oscillators 41
Mohammad S. Islam (Case Western Reserve University), Soumyajit Mandal (Case Western Reserve University), Siddharth Kumar Singh (Indian Institute of Technology Kharagpur)

We describe a highly-programmable integrated sustaining amplifier for reconfigurable MEMS-referenced oscillators. The frequency response, voltage gain, and phase shift of the amplifier can be independently controlled using bias currents, thus enabling it to be interfaced with a variety of MEMS devices with resonant frequencies in the 10-120kHz range. The chip, which was designed in 0.5µm CMOS, also includes i) an automatic level control (ALC) circuit; and ii) an independently adjustable background compensation network (BCN) that is used for canceling the parasitic electrical capacitance of the resonator. We present experimental data that confirms the functionality of individual circuit blocks and also the amplifier as a whole

Lithium Niobate MEMS Devices and Subsystems for Radio Frequency Signal Processing 45
Songbin Gong (University of Illinois at Urbana-Champaign), Yongh-Ha Song (University of Illinois at Urbana-Champaign), Tomas Manzaneque (University of Illinois at Urbana-Champaign), Ruochen Lu (University of Illinois at Urbana-Champaign), Yansong Yang (University of Illinois at Urbana-Champaign), Ali Kourani (University of Illinois at Urbana-Champaign)

This paper presents a review of the recent advancements in Lithium Niobate (LiNbO3) micro-electro-mechanical systems (MEMS). Several types of devices or subsystems, including resonators, transformers, filters, and delay lines, are discussed, targeting the different functions that are currently sought after in radio frequency signal processing for various existing and emerging applications. Technical challenges that remain in the path of deploying these devices are also summarized with a few suggested future research directions.

Damping in Aluminum Nitride Contour Mode MEMS Resonators 49
Jeronimo Segovia-Fernandez (Broadcom Ltd.)

This work compiles the efforts made to determine and model the main damping mechanisms in Aluminum Nitride (AlN) Contour Mode Resonators (CMRs). Experiments have proved that there are two main sources of damping dominating the AlN CMR quality factor (Q) at very and ultra high frequency (V/UHF): thermoelastic damping (TED) in the metal electrodes (Qted) and anchor losses (Qanc). A semi-analytical approach to predict TED (Qted) and a numerical approach to accurately model anchor losses (Qanc) in AlN CMRs are presented in this work. As an example of the experiments that demonstrate the impact of Qted and Qanc, we look at the temperature dependence of Q displayed by resonators having different electrodes materials.

Acoustic Wave Transduction in Gallium Nitride Heterostructures 53
Siddhartha Ghosh (MIT Lincoln Laboratory)

This paper highlights development efforts in the use of AlGaN/GaN heterostructures for launching, receiving and amplifying surface acoustic waves. High-electron mobility transistors (HEMTs) are demonstrated in acoustic wave delay lines with conventional interdigital transducers (IDTs). The amplitude for the transmitted Rayleigh mode is modulated through appropriate HEMT biasing conditions for a common source configuration. Modifying carrier density in the two-dimensional electron gas (2DEG) generates dynamic screening of the piezoelectric field. This directly affects the generation and detection of surface acoustic waves. In addition, the interaction of carriers with the phonons at the 2DEG can generate amplification of the traveling acoustic wave.

Session A1L-D: Student Paper Contest I

Chair: Ken Jenkins, *Pennsylvania State University*
Time: Monday, August 7, 2017, 10:20 - 12:00
Location: Eaton Hall 203

Microfluidic Platform to Study Intercellular Connectivity through On-Chip Electrical Impedance Measurement 56
Joel Dungan (Tufts University), Juanita Mathews (Tufts University), Michael Levin (Tufts University), Valencia Koomson (Tufts University)

A platform has been developed to study intercellular communication in non-neural cells as it relates to developmental biology and morphogenetic bioengineering. The versatile platform uses laminar flow in a microfluidic channel to create a "sucrose gap" that forces electrical signaling through a cell monolayer. The intercellular communication in the cell network is detected through electrical impedance measurements. A phase sensitive homodyne system has been designed and simulated in a 130nm CMOS process to provide a readout of cell monolayer complex impedance within the device. The system exhibits a highly linear conversion rate of 0.589mV/kΩ for cell layer impedances up to 1 MΩ.

A System-on-Chip NFC Bicycle Tire Pressure Measurement System 60
Carolin Kollegger (Infineon Technologies AG), Philipp Greiner (Technische Universität Graz), Christoph Steffan (Infineon Technologies AG), Martin Wiessflecker (Infineon Technologies AG), Heiko Froehlich (Infineon Technologies Dresden GmbH), Thoralf Kautzsch (Infineon Technologies Dresden GmbH), Gerald Holweg (Infineon Technologies AG), Bernd Deutschmann (Technische Universität Graz)

This paper presents a monolithically implemented NFC bicycle tire pressure measurement system (BTPMS) with integrated antenna, on-chip capacitive pressure and temperature sensor, RFID interface for HF/NFC and EEPROM. It provides cost advantages and impresses with its large scale integration. The used RFID communication protocol ensures compatibility with state-of-the-art NFC devices. This battery less stand-alone system is powered wirelessly by any state-of-the-art near field communication device. Using a two-point calibration technique, various measurements have been performed. In the pressure range of 1 bar to 6 bar and for temperatures between -15°C to 55°C a ±3σ accuracy of ±0.4 bar is achieved.

Design and Performance Analysis of Energy Harvesting Sensor Networks with Supercapacitor 64
Ruisi Ge (North Dakota State University), Zhibin Lin (North Dakota State University), Na Gong (North Dakota State University), Jinhui Wang (North Dakota State University)

Far field radio frequency (RF) harvesting technique have become popular method to power wireless sensor network recently. However, due to the low efficiency of RF energy harvester, RF powered wireless sensor network is unable to perform dynamic network allocation. Accordingly, the functionality is limited. This paper presents a practical RF powered wireless sensor node design that could dynamic join the network and send data packet. A non-ideal super capacitor storage estimate model is proposed. Test result indicated the proposed model can accurate estimate the storage state, the RF energy harvesting node could dynamically join network as far as 10 meter.

An Embeddable Algorithm for Gunshot Detection 68
Sainath Reddy Samireddy (University of Akron), Joan Carletta (University of Akron), Kye-Shin Lee (University of Akron)

A pre-processing algorithm for the detection of shotguns has been implemented using the General Cross-correlation (GCC) method. The relationship between Sound Pressure Level (SPL) and distance for different gunshot sounds are studied to determine whether the sound is loud enough to be detected as a gunshot at a certain distance range. The shotgun sound pattern received is made to correlate with a unique shotgun filter which is extracted from the muzzle blast pattern of a reference shotgun. In this paper, a brief description of detection approach is presented along with the corresponding simulation results.

On One Step Row Readout Technique of Selector-Less Resistive Arrays 72
Mohammed E. Fouda (University of California-Irvine), Ahmed M. Eltawil (University of California-Irvine), Fadi J. Kurdahi (University of California-Irvine)

Resistive crossbar arrays show significant improvement in terms of energy and area efficiency when compared to current SRAM based memory technologies. However, due to its resistive nature, it suffers from undesired current sneak paths complicating read-out procedures. In this paper, we present a voltage-based reading technique in resistive memories. The simplicity of the readout circuit enables parallel reading where it is possible to read all the row data in the same cycle. Simulations results confirm the robustness of the technique, with wire resistance and variability of switching devices taken into consideration. Finally, a general figure of merit is introduced in order to compare the one step readout approach to other approaches.

Session A1L-E: Special Session: Emerging Bio-Interface Technologies for Life Science Applications

Chair: Ebrahim Ghafar-Zadeh, *York University*
Time: Monday, August 7, 2017, 10:20 - 12:00
Location: Eaton Hall 206

An Area and Power-Efficient Mixed-Mode Fully Programmable FIR Filter for Biomedical Interface Microsystems 76
Hossein Kassiri (York University)

A mixed-mode analog-digital transposed 64-tap finite impulse response filter for multi-channel biomedical monitoring systems is presented. The proposed architecture conducts multiplication in analog domain by taking advantage of a preceding multiplying-ΔΣ ADC, resulting in ×16.4 saving in silicon area. The presented architecture along with the resource sharing scheme employed yields a total of ×31.5 saving in power x area. Mathematical analysis and simulation results based on IBM 0.13µm CMOS technology models are presented.

Modular Multi-Organ-on-Chips Platform with Physicochemical Sensor Integration 80
Yu Shrike Zhang (Brigham and Women's Hospital / Harvard Medical School)

Organs-on-chips systems are microfluidic three-dimensional miniature human organoid models designed to reproduce the key biological and physiological parameters of their in vivo counterparts. They have recently emerged as a viable platform for personalized medicine and drug screening. Here we propose the development of a fully integrated multi-organ-on-chips platform in conjunction with modular physical, biochemical, and optical sensing units, which together is operated in a continuous and automated manner. We believe that, this novel platform technology has opened a new avenue for integrating biomimetic organoids with the potential to achieve large-scale automation in drug screening processes.

Low-Cost Fabrication of Paper-Based Systems: Microfluidics, Sensors, Electronics and Deployment 84
Gerd Grau (York University)

Paper is a very interesting substrate material for sensing systems due to its porous nature, low cost, light weight and biodegradability. Low-cost sensing platforms can be created by combining paper substrates with low-cost printed fabrication methods. Here, recent progress is reviewed in the areas that will be needed to create powerful paper-based sensing systems: pump-free microfluidics to manipulate fluids of interest, biosensors to detect analytes, printed microelectronics for signal processing and novel methods of deploying paper-based systems such as printed gliders.

Biological Modeling Challenges in a Multiphysics Approach 88
Jessy Mathault (Université Laval), Hamza Landari (Université Laval), Frédéric Tessier (Université Laval), Paul Fortier (Université Laval), Amine Miled (Université Laval)

Modeling biological behaviour requires a multidisciplinary approach and very large computational resources. In this paper, we present an overview of our research work with regards to biological neuron network (NN) modeling, electro-chemical reaction emulation for neurotransmitters and finite element modeling (FEM) of a very low pressure micropump for neurotransmitter concentration modulations. Three different approaches have been explored, namely Matlab simulations of biological NN, Matlab simulations of electrochemical reactions and the FEM approach. Our objective through biological NN modeling is to investigate the need to develop a dedicated chip for a NN implementation or to use a strictly software approach. The objective of the electrochemical emulator is to provide a tool which can help us to understand how to decompose cyclic voltammetry curves into more conventional and easy to interpret graphs. However, although the three approaches appear independent, they are in fact all related as we investigate the computer performances needed for biological modeling.

A Current based Capacitance-to-Frequency Converter for Lab-on-Chip Applications 92
Saghi Forouhi (York University / Isfahan University of Technology), Omid Farhanieh (York University), Resoul Dehghani (Isfahan University of technology), Ebrahim Ghafar-Zadeh (York University)

This paper presents a novel multimodal CMOS based biosensor consisting of integrated capacitive and thermal sensors for Lab-on-Chip applications. A new capacitive sensor is also proposed which converts the capacitance changes to frequency by using a current-controlled oscillator. This sensor works based on charge based capacitance measurement (CBCM) technique. Its operation in current mode helps this capacitive sensor to have a relatively wide dynamic range along with a suitable resolution. We also put forward the analysis of sensing and parasitic capacitances using a 3D field solver incorporated with Cadence software. Based on these results, the proposed multi-sensor system offers advantages for high-throughput cellular monitoring purposes.

GPU base Calling for DNA Strand Sequencing 96
Roksana Hossain (University of Calgary), Robinson Mittmann (York University), Ebrahim Ghafar-Zadeh (York University), Geoffery G. Messier (University of Calgary), Sebastian Magierowski (York University)

Emerging third-generation DNA strand-sequencers are achieving unprecedented levels of sensor speed density in a portable platform. A substantial computing effort is need to process the data from these machines in real-time. Among the processing challenges is base calling, a sequence labelling step that associates raw measurements with DNA bases. We have implemented a serial and a GPU based parallel version of the hidden Markov model based Base calling. The throughput of Parallel Base calling is 2.85X faster than the existing tool.

Session A1L-F: Digital Circuits and Systems I

Chair: Reyad El-Khazali El-Khazali, *KUSTAR*
Co-Chair: Srinivas Katkoori, *University of South Florida*
Time: Monday, August 7, 2017, 10:20 - 12:00
Location: Paige Hall - Crane Room

Ultra-Compact sub-10nm Logic Circuits based on Ambipolar SB-FinFETs 100
Talha Furkan Canan (Ohio University), Savas Kaya (Ohio University), Avinash Kodi (Ohio University), Hao Xin (University of Arizona), Ahmed Louri (George Washington University)

Novel ultra-compact two-transistor (2T) XOR, NAND, NOR gates in sub-10nm CMOS are proposed and verified via TCAD simulations. The approach utilizes independent-gate Schottky-barrier FinFETs with specific gate work-functions that can be conveniently adjusted to design unique 2T logic circuits. the 2T-XOR circuit is based on a novel hitherto unexplored conjugate-gate device with separate electron and hole channels between a single pair of source/drain contacts. The 2T NAND/NOR circuit utilizes high-threshold devices via work function engineering as well. Hence, It has been shown that circuits operate with as low as 0,6V supply and down to 5nm gate length with a power-delay product of ~5e-18J.

Analysis and Design of CMOS Resettable C-Elements 104
Nasim Soufizadeh-Balaneji (North Dakota State University), Scott C. Smith (North Dakota State University)

This paper reviews existing reset schemes for the Muller C-element, one of the main primitives in asynchronous paradigms. Using a mathematical-based method and with the help of pass-transistor logic, an efficient implementation is developed that yields better performance. Simulations with a standard IBM 130-nm CMOS process, confirm that the proposed design achieves substantial improvement over existing implementations with respect to throughput, energy, and area.

Partially Universal Modules for High Performance Logic Circuit Design 108
Ke Chen (Northeastern University), Fabrizio Lombardi (Northeastern University), Jie Han (University of Alberta)

This paper investigates a partial ULM (PULM) in which only specific functions are incorporated in the logic module. As instances of a PULM, two types of a 4-input PULM are proposed in this paper. These PULMs are initially found by profiling the most common combinational functions in benchmarks to be used in the module circuits. A number of functions of the highest occurrence (4 and 8 functions respectively) are utilized and their performances with respect to average delay and power dissipation are assessed by HSPICE simulation.

A Low Power AES-GCM Authenticated Encryption Core in 65nm SOTB CMOS Process 112
Van-Phuc Hoang (Le Quy Don Technical University), Van-Tinh Nguyen (Le Quy Don Technical University), Anh-Thai Nguyen (Le Quy Don Technical University), Cong-Kha Pham (University of Electro-Communications)

This paper presents a low power AES-GCM IP core which combines an improved four-parallel architecture, an advanced 65nm SOTB CMOS ASIC library and a low complexity clock gating technique. The power consumption of the proposed AES-GCM core with clock gating is only 8.9mW which is much lower than other AES-GCM IP cores presented in literature.

In-Memory Area-Efficient Signal Streaming Processor Design for Binary Neural Networks 116
Kota Ando (Hokkaido University), Kodai Ueyoshi (Hokkaido University), Kazutoshi Hirose (Hokkaido University), Kentaro Orimo (Hokkaido University), Shinya Takamaeda-Yamazaki (Hokkaido University), Masayuki Ikebe (Hokkaido University), Tetsuya Asai (Hokkaido University), Masato Motomura (Hokkaido University), Haruyoshi Yonekawa (Tokyo Institute of Technology), Shimpei Sato (Tokyo Institute of Technology), Hiroki Nakahara (Tokyo Institute of Technology)

The expanding use of deep learning algorithms causes the demands for accelerating neural network (NN) signal processing. For the NN processing, in-memory computation is desired, in which expensive data transfer can be eliminated. In reflection of recently proposed binary neural networks (BNNs), which can reduce the computation resource and area requirements, we designed an in-memory BNN signal processor that densely stores binary weights in on-chip memories and can scale linearly with serial-parallel-serial signal stream. It achieved 3 and 71 times better per-power and per-area performance than an existing in-memory neuromorphic processor.

Session A1L-G: SoC and NoC

Chair: Srinivas Katkoori, *University of South Florida*
Co-Chair: Hector Solar, *CEIT*
Time: Monday, August 7, 2017, 10:20 - 12:00
Location: Paige Hall - Terrace Room

SoC-FPGA Implementation of the Sparse Fast Fourier Transform Algorithm 120
Alexander López-Parrado (Universidad del Quindío), Jaime Velasco-Medina (Universidad del Valle)

This brief presents the SoC-FPGA implementation of the modified Nearly Optimal Sparse Fast Fourier Transform (sFFT) algorithm. The implementation was carried out by using hardware/software co-design based on software profiling that helped to find out that pseudo-random Spectral Permutation, Windowing, and Sub-Sampling (SPWS) are the signal processing operations that require most processing time in the modified sFFT algorithm. Then, by considering the software profiling results, a SPWS hardware accelerator was designed by using structural and generic VHDL. The SPWS hardware accelerator is composed of one Random Sampling Direct Memory Access Controller (RS-DMAC) and one Windowing and Sampling (WS) circuit. Later, the SPWS is integrated into the FPGA fabric of the SoC-FPGA to accelerate the whole modified sFFT algorithm. In this case, the software sub-system is managed by the Real Time Operating System (RTOS) QNX Neutrino. Finally, the verification results showed that 4.6 times acceleration is achieved for the SPWS, and 3.1 times acceleration is achieved for the whole modified sFFT algorithm when it is compared with the fully software implementation.

A System On Chip Design for Fast Time Domain Impedance Spectroscopy 124
Edmund Spencer (University of South Alabama), David Clark (University of South Alabama), Ravi Gollapalli (University of South Alabama), Samuel Russ (University of South Alabama), Brannon Kerrigan (Virginia Polytechnic Institute and State University)

We describe a Time Domain Impedance Probe (TDIP) circuit design that is used to measure the absolute density of ionospheric plasmas. A preliminary version of this instrument was flown on a sounding rocket, but here we outline the system and circuit design that is being implemented for a Low Earth Orbit (LEO) micro-satellite. The design employs a bridge architecture together with a software adaptive filter and LMS algorithm for fast calibration and data compression.

Global Clock Distribution on Standing Wave with CMOS Active Inductor Loading 128
Jing Yang (Northeastern University), Yong-bin Kim (Northeastern University)

In this paper, an X-tree clock distribution topology based on standing wave oscillator is introduced. To increase output amplitude at the loading point and saving chip area, a novel CMOS active inductor is designed and applied to each loading points of the network. The cascoded differential active inductor is 1 nH with Q = 344 at 10 GHz. This makes the two stage, 6.2 mm x 6.2 mm dimensional standing wave based clock distribution network perfectly convey clock signals everywhere on the chip without taking much of the chip area while keeping a relatively high output voltage swing. The clock jitter is 0.139 ps with almost zero clock skew.

Path Loss-Aware Adaptive Transmission Power Control Scheme for Energy-Efficient Wireless NoC 132
Shashwat Kaushik (Indraprastha Institute of Information Technology Delhi), Muni Agrawal (Indraprastha Institute of Information Technology Delhi), Hemanta Kumar Mondal (Indraprastha Institute of Information Technology Delhi), Sri Harsha Gade (Indraprastha Institute of Information Technology Delhi), Sujay Deb (Indraprastha Institute of Information Technology Delhi)

Wireless Networks-on-Chip offer unprecedented advantages to replace the long-distance multi-hop communication bottlenecks of conventional NoCs by augmenting them with single hop, long-range wireless links in many-core systems. In wireless interfaces (WIs), RF transceiver components are consuming significant amount of total power budgets to replace the multi-hop communications. Specifically, transmitter accounts a significant portion of overall transmission energy. To improve energy efficiency, we propose the Path Loss-aware Adaptive Transmission Power Control (PATPC) scheme using multi-voltage scaling based on present destination. To implement this, we estimate the required power using path loss model for on-chip wireless channel. Proposed method is achieved an average saving of 53% compared with traditional approaches with low silicon overheads.

Advertiser Elevator: A Fault Tolerant Routing Algorithm for Partially Connected 3D Network-on-Chips 136
Ebadollah Taheri (Boston University), Mihailo Isakov (Boston University), Ahmad Patooghy (Boston University), Michel A. Kinsy (Boston University)

In this paper, we propose an adaptive routing algorithm for vertically partially connected 3D NoCs to (1) overcome failures in vertical links, and (2) find the nearest available vertical link for rerouting of packets. To track the position of each vertical link and distance to the other nodes, the proposed routing algorithm, named Advertiser Elevator, indexes each vertical link and implements a mechanism for announcing and sharing these indexes with the other nodes of the network.

Session A2P-H: Signal and Image Processing

Chair: Neeraj Magotra, *WNEU*
Time: Monday, August 7, 2017, 13:00 - 14:20
Location: Ballou Hall - Coolidge Room

Spatially Constrained Generalized Dirichlet Mixture Model for Image Segmentation 140
Jai Puneet Singh (Concordia University), Nizar Bouguila (Concordia University)

A new color image segmentation of noisy images based on spatial information with the Generalized Dirichlet mixture model is presented. The methodology uses Markov Random Field distribution with a novel factor that is induced in a mixture model. The model is learned using Expectation-Maximization (EM) algorithm based on Newton-Raphson approach. The obtained results using real images are more encouraging than those proposed in earlier algorithms/models.

Performance Analysis of Superdirective Beamforming of Circular Hydrophone Array 144
Zhengyao He (Northwestern Polytechnical University), Qiang Shi (Northwestern Polytechnical University), Yuanliang Ma (Northwestern Polytechnical University)

The performance of superdirective beamforming of a practical circular hydrophone array is investigated. The received signal of a 16-element circular hydrophone array with radius of 0.25m are measured in the anechoic water tank. The array manifold at the frequency of 1.11kHz is obtained. The superdirective beamforming of the circular array is designed and realized. The correctness and effectiveness of the superdirective beamforming method is verified by the experimental results. The practical directivity of the circular array obtained by the superdirective beamforming method is obviously superior to that obtained by the conventional beamforming method.

Wave Digital Information Anticipator 148
Karlheinz Ochs (Ruhr-Universität Bochum), Eloy Hernandez-Guevara (Ruhr-Universität Bochum), Enver Solan (Ruhr-Universität Bochum)

Pioneering developments in electrical engineering are based on inspirations from biology. They exhibit naturally an efficient information processing. For example, hardware realizations of memristive circuits mimicking the anticipatory behavior of unicellular organisms like amoebas have been developed in this context. Unfortunately, circuits are not appropriate for algorithms dedicated in the area of digital signal processing. We intended to get an algorithmic model of the anticipation circuit for utilizations in digital signal processing applications. In our approach we have applied the wave digital method to get a digital replica of the analog circuit. This offers several benefits, like the ability for preserving the passivity of the analog counterpart, the possibility for a parallel processing approach, efficiency, and robustness of the resulting algorithmic model. The memristive device of the original circuit has been replaced by a novel multilevel memristor model with suitable features for anticipation of digital patterns. The resulting algorithmic model offers innovative applications in e.g. robotics or artificial neural networks.

Wave Digital Emulation of Spike-Timing Dependent Plasticity 152
Karlheinz Ochs (Ruhr-Universität Bochum), Eloy Hernandez-Guevara (Ruhr-Universität Bochum), Enver Solan (Ruhr-Universität Bochum)

Neuromorphic circuits are potential candidates for solving costly computations in an efficient manner. Such circuits, mimicking partial functionalities of the brain, need a large number of components. Simulation models are appropriate for first investigations, but they are very time-consuming regarding complex systems. Hardware realizations of specific components, like memristive devices, in such circuits are not possible for a desired functionality. We propose a methodology based on emulation techniques to overcome such problems. Therefore, the wave digital method has been utilized to get a digital replica of a memristive circuit mimicking long-term changes in the strength of synaptic coupling. In this work, both longterm potentiation as well as long-term depression are successful emulated. This approach can also be used for a partial emulation of the subsystems, e.g. only memristive devices, of a more complex overall system.

Noise Estimation with an Inverse Comb Filter in Non-Stationary Noise Environments 156
Tetsuya Shimamura (Saitama University), Fumiya Kato (Saitama University)

We propose a new noise estimation method using only the current frame of noisy speech. The proposed method utilizes an inverse comb filter for noisy speech to suppress the power of speech, and estimates the noise from the resulting spectrum. It is shown by experiments that the spectral subtraction combined with the proposed noise estimation method is superior to the conventional speech enhancement methods in non-stationary noise environments.

An Enhanced TDoA Approach Handling Multipath Interference in Wi-Fi based Indoor Localization Systems 160
Tuo Xie (Tsinghua University), Chun Zhang (Tsinghua University), Yongming Li (Tsinghua University), Hanjun Jiang (Tsinghua University), Zhihua Wang (Tsinghua University)

Received Signal Strength Indicator (RSSI) is simplest among various indoor localization methods. The main drawback is requiring a training phase to build fingerprints database, which is time consuming and sensitive to changes of test environment. Time based approaches such as Time of Arrival (ToA) and Time Difference of Arrival (TDoA) achieve better performance with some hardware expenditure, while location accuracy is significantly affected by multipath interference. By employing Super-resolution techniques (SRTs), multipath components can be estimated to improve localization precision, but limited to OFDM-based Multiple Input Multiple output (MIMO) wireless communication systems. Considering for general radio signals with strong correlation, we propose an enhanced TDoA approach based on RSS-assisted cross-correlation method. Simulation and experimental results demonstrate that our method is effective to mitigate multipath interference, verified by IEEE 802.11b WLAN. Compared with SRTs, our method achieves comparable localization precision, and has superiority in computational complexity and anti-noise performance.

Performance Study of the SURE Trimmed Denoising Method for One Dimensional Signals 164
Maha A. Hassanein (Cairo University), Magdy Tawfik Hanna (Fayoum University)

An adaptive data driven threshold is proposed for denoising one dimensional signals. The threshold is derived in a SURE (Stein Unbiased Risk Estimator) based framework using hybrid trimmed thresholding and the wavelet coefficients are obtained by a Translation Invariant transform. A detailed mathematical derivation of the threshold is provided. An optimized selection of the trimmed thresholding parameter (alpha) at each decomposition level of the transform is tackled and its effect on the overall performance of the proposed method is investigated. The experimental results show that the proposed method with automatic parameter adjustment is typically better or at least not worse than other wavelet based and non-wavelet based methods. It has been found that the method with optimal parameter value outperforms that with fixed parameter value more than 75% of the time over a wide range of input SNRs.

Overdetermined Blind Source Separation using Approximate Joint Diagonalization 168
Taiki Asamizu (Tokyo University of Science), Shinya Saito (Tokyo University of Science), Kunio Oishi (Tokyo University of Technology), Toshihiro Furukawa (Tokyo University of Science)

Blind separation of mixtures has been achieved by approximate joint diagonalization (AJD) approaches. This paper presents an approach for overdetermined blind source separation (BSS) using AJD. The approach is based on an alternative minimization of the indirect and direct least-squares criteria to the diagonal matrices in the first phase and to the mixing matrix in the second phase, respectively. Simulation result demonstrates that the proposed algorithm is capable for achieving better separation performance in overdetermined mixtures than in determined mixtures at reduced complexity.

Embedded Multiple Object Detection based on Deep Learning Technique for Advanced Driver Assistance System 172
Fong-An Chang (National Chiao Tung University), Chia-Chi Tsai (National Chiao Tung University), Ching-Kan Tseng (National Chiao Tung University), Jiun-In Guo (National Chiao Tung University)

This paper proposes an optimized pedestrian and vehicle detection method based on deep learning technique. We optimize the convolutional neural network architecture by three mainly methods. The first one is the choice of the learning policy. The second one is to simplify the convolutional neural network architecture. The last one is careful choice of training samples. With limited loss of accuracy, we can greatly speed up the original deep learning method coming from CAFFE. The proposed system is developed on PCs and implemented on the platforms of both the PC and embedded systems. We can achieve around 90% accuracy when it is tested on an open-source dataset. On PCs with Intel i7@3.5GHz CPU, the proposed design can reach the performance about 720x480 video at 25 frames per second. On the NVIDIA JETSON TX1 embedded system, the proposed design can reach the performance about 720x480 video at 5 frames per second

Teager Energy Operated Perceptual Wavelet Packet Transform Coefficients for Arithmetic Task Classification from EEG Signals 176
Celia Shahnaz (Bangladesh University of Engineering and Technology), Tanmoy Sarker (Bangladesh University of Engineering and Technology), Sudip Paul (Bangladesh University of Engineering and Technology), M. Omair Ahmad (Concordia University), Wei-Ping Zhu (Concordia University)

Recently the development of brain-computer interface applications has drawn the attention of research community as it can assist physically challenged people to communicate with their brain electroencephalogram (EEG) signal. In this paper, a Brain-Computer Interface (BCI) is designed using electroencephalogram (EEG) signals where the subjects have to think of only a single mental task. The presented BCI approach includes three stages: (a) filtering out the electrical frequency components and segmentation of the raw signals (b) Perceptual wavelet packet transform of the segments and calculating the Teager Energy(TE) of the subbands (c) classification using SVM classifier. Perceptual wavelet packet transform is used to decompose the EEG signals into a number of frequency bands, and Teager Energy is calculated to maintain distinguishable energy profiles of those bands which provide a maximum classification accuracy of about 100%.

FPGA Implementation of a Support Vector Machine Classifier for Ultrasonic Flaw Detection 180
Yiyue Jiang (Illinois Institute of Technology), Kushal Virupakshappa (Illinois Institute of Technology), Erdal Oruklu (Illinois Institute of Technology)

In this work, we investigate the hardware implementation of Support Vector Machine (SVM) prediction on an FPGA platform for industrial ultrasound applications. Specifically, SVM is used as classifier for identifying ultrasonic A-scan signals as signals with flaw or signals without flaw. Hardware acceleration using FPGA is the main theme of the presented work. The architecture used to implement the SVM prediction is discussed in detail. Synthesis results indicate that Ultrasonic flaw detection using SVM algorithm is feasible for real-time applications on programmable hardware such as FPGAs.

Traffic Sign Recognition based on the NVIDIA Jetson TX1 Embedded System using Convolutional Neural Networks 184
Yan Han (Illinois Institute of Technology), Erdal Oruklu (Illinois Institute of Technology)

Traffic sign recognition is an important step for integrating smart vehicles into existing road transportation systems. In this paper, an NVIDIA Jetson TX1-based traffic sign recognition system is introduced for driver assistance applications. The system incorporates two major operations, traffic sign detection and recognition. Image color and shape based detection is used to locate potential signs in each frame. A pre-trained convolutional neural network performs classification on these potential sign candidates. The proposed system is implemented on NVIDIA Jetson TX1 board with web-camera. Based on a well-known benchmark suite, 96% detection accuracy is achieved while executing at 1.6 frames per seconds.

Underwater Channel Estimation and Multiple Object Tracking using Embedded Computing 188
Edwin Anaya (Recinto Universitario de Mayagüez), David Marquez (Recinto Universitario de Mayagüez), Neysha Matos (Recinto Universitario de Mayagüez), Genesis Nieves (Recinto Universitario de Mayagüez), Juan Valera (Turabo University), Cesar Aceros (Universidad Pontificia Bolivariana), Domingo Rodriguez (Recinto Universitario de Mayagüez)

This work presents an embedded computing framework for the analysis and design of large scale algorithms utilized in the estimation of acoustic doubly dispersive, randomly time-variant, underwater communication channels. Channel estimation results are used, in turn, in the proposed framework for the development of efficient high performance algorithms, based on fast Fourier transformations, for the search, detection, estimation, and tracking (SDET) of underwater moving objects through acoustic wavefront signal analysis techniques associated with real-time electronic surveillance and acoustic monitoring (eSAM) operations. Particular importance is given in this work to the estimation of the range and speed of deep underwater moving objects modeled as point targets. The work demonstrates how to use Kronecker products signal algebra (KSA), a branch of finite-dimensional tensor signal algebra, is used as a mathematical language to assist in the development and implementation of the embedded computing algorithms.

Speeding Up Tone Mapping Operators: Exploiting Parallelism for Real-Time, High Dynamic Range Video 192
Ziad Youssfi (Ohio Northern University), Firas Hassan (Ohio Northern University)

Tone mapping operators map high dynamic range images so that they can be displayed with a high dynamic range appearance in a limited range medium. However, these operators have been computationally expensive to implement in real-time video image processing. In this paper, we revisit these operators to simplify them so that we can speed up their execution on parallel processing platforms such as GPUs. We offer CUDA implementations of these functions that achieve significant speedups. For example, our global tone mapping implementation achieves 12,850 fps. We also offer insight into how local tone mapping functions could run into memory bottlenecks of GPU architecture.

Book Organization Checking Algorithm using Image Segmentation and OCR 196
Mohammad Azim Ul Ekram (Texas State University), Anjani Chaudhary (Texas State University), Ashutosh Yadav (Texas State University), Jagadish Khanal (Texas State University), Semih Aslan (Texas State University)

Organizing and rearranging library books in appropriate order requires attention and care of librarians. The book indexing and organizing algorithm will detect misplaced library books and suggest a proper position to the user. It can be implemented in a smartphone or a server or an autonomous embedded system. It first segments the captured image to find proper tag area in the book. Then crops that tag area and process that with OCR to detect string. From the string, it is possible to determine if a book is on the right shelf or row.

Comprehensive Comparison of Gradient-Based Cross-Spectral Stereo Matching Generated Disparity Maps 200
Christopher B. Picardo (Brown University), Justin G.R. Delva (Draper Lab), R. Iris Bahar (Brown University)

We provide a systematic means of classifying and easily identifying optimal disparity maps (in terms of a combination of runtime, accuracy, and validity). Our experimental results show how a Pareto frontier of optimal disparity maps can be generated as a result of our analysis. Finally, our software tool serves as a baseline for the development of new and improved GB-CSSM algorithms that can be applied to a broader range of applications.

Fractional-Order Discrete-Time PIλ Controllers Design 205
Reyad El-Khazali (Khalifa University)

This paper introduces a new design method of discrete-time fractional-order PI controllers. It is based on using an exact discretization method that always guarantees the implementation of 3rd-order, minimum-phase, and stable discrete-time fractional-order controllers. The structure of the controller can be considered as an adaptive one since it depends on the order of the controller, which is one of three tuning parameters. The other two parameters are the controller gain, and its integral reset time constant. The exact discretization method is more effective than the direct or indirect ones, where rational z-transfer functions are developed instead of using generating functions. The hereditary effect of the proposed PI^λ controllers can be extended by increasing the order of the discrete-time operators beyond three. The main points of the proposed method are illustrated via a numerical simulation.

Antenna on Chip Design Utilizing 3D Integration for Mixed Signal Applications 209
S. Adamshick (Western New England University), A. Johnson (Western New England University), K. Moriarty (Western New England University), W. Tremblay (Western New England University), J. Burke (Western New England University)

This paper proposes implementing an antenna operating in the millimeter wave band of 56-64 GHz on the backside of an Integrated Circuit (IC) that uses Through Silicon Via (TSV) technology for a System in Package (SiP) approach to mixed signal design. A folded monopole antenna that utilizes a coaxial TSV feed line is selected to implement the design on the backside of the silicon die. Furthermore, the initial design is modeled using Ansys's High Frequency Structure Simulator (HFSS) to measure appropriate antenna parameters including a directivity of 1.27 dB. The final design proposes using an artificial magnetic conductor as a reflector to improve antenna directivity by 4.87 dB and eliminates propagation of electromagnetic waves back into the substrate.

Session A2P-J: Energy Processing Circuits and Systems

Chair: Aatmesh Shrivastava, *Northeastern University*
Time: Monday, August 7, 2017, 13:00 - 14:20
Location: Ballou Hall - Coolidge Room

A Particle Swarm Optimization and Branch and Bound based Algorithm for Economical Smart Home Scheduling 213
Yangyizhou Wang (Waseda University/Shanghai Jiao Tong University), Cong Hao (Waseda University), Takeshi Yoshimura (Waseda University)

Smart home scheduling, as one of the most effective techniques in Demand Side Management (DSM), is now attracting more and more research interests in the recent years. In this paper we propose an efficient scheduling algorithm for smart home resident to reduce the monetary cost of the electricity. The proposed algorithm is an improved particle swarm optimization(PSO) algorithm that can schedule the smart appliances under discrete power level and quadratic pricing model. Branch and bound method is adopted to map real number values to discrete power level values. Simulation results shows that our method exceeds the previous

On the Stability of Distributed On-Chip Low Dropout Regulators 217
Albert Ciprut (University of Rochester), Eby G. Friedman (University of Rochester)

Distributed on-chip low dropout (LDO) voltage regulators have become common due to the increasing number of on-chip voltage domains, dynamic voltage scaling, and the need for high quality power. Due to the current limitations of on-chip LDOs, hundreds of these regulators are required to deliver high quality power within modern high performance microprocessors. As the number of parallel connected LDOs increases, however, the stability of the power grid degrades due to the off-chip and inpackage parasitic inductance. In this paper, the stability of the onchip power grid composed of multiple distributed LDO regulators is evaluated from the perspective of the parasitic impedance. The relation between the grid stability and the number of LDOs that share the grid is described, and a guideline for evaluating grid stability is proposed. Moreover, several design solutions are offered to compensate for the off chip inductance to enhance the stability of on-chip power grids, supporting the deployment of a large number of LDO regulators.

Unipolar Symmetrical Variable-Capacitance Generators for Energy Harvesting 221
Antonio Carlos M. de Queiroz (Universidade Federal do Rio de Janeiro), Luiz Carlos Macedo de Oliveira Filho (Universidade Federal do Rio de Janeiro)

This paper investigates a class of electrical generators based on capacitors and diodes, with two capacitors being variable. Their main characteristics are a symmetrical structure and that they produce two outputs with the same polarity. The simplest version is analyzed in more detail, although in an approximate way, and generalizations of it are obtained, identified with a particular form of two-phase voltage multiplier. The generalized versions require less capacitance variation for operation, and are shown, by simulation to have faster startup than structures with a single variable capacitor. The structures are tested experimentally with a 3D-printed pair of variable capacitors that tries to emulate a structure built with microelectromechanics techniques.

Modelling of Charge and Selfdischarge Responses of Supercapacitors 225
Pankaj Saha (National Institute of Technology Silchar), Satadru Dey (University of California-Berkeley), Munmun Khanra (National Institute of Technology Silchar)

The paper proposes a framework to empirically model the terminal voltage response of supercapacitors during charge and selfdischarge. A set of empirical formulae has been identified from experimental data for modeling, separately, the charge and self-discharge response of supercapacitors. The proposed empirical models are the function of charging rate and time. The proposed framework for modeling supercapacitor terminal voltage response has been demonstrated by applying it on a 10 F Supercapacitor cell.

Multi-String LED Driver with Accurate Current Matching and Dynamic Cancellation of Forward Voltage Mismatch 229
Punith R. Surkanti (New Mexico State University), Disha Mehrotra (New Mexico State University), Manaswini Gangineni (New Mexico State University), Paul M. Furth (New Mexico State University)

In this paper, we present a Multi-String LED Driver which is capable of driving five LED strings with two series LEDs in each string. The current in the LED strings is regulated using a hysteretic control loop. Accurate current matching is achieved using a regulated cascode current mirror architecture. The Loser-Take-All circuit enables dynamic cancellation of LED forward voltage mismatch and also optimizes efficiency. A PFM dimming block is designed to operate with 200~kHz clock and has 11 programable dim ratios ranging from 2:1 to 2048:1. This LED driver is implemented in 0.5~μm CMOS process and operates with a li~-ion battery with a voltage range 3~-~4.2~V. Efficiency at steady state(no dimming), 4:1 and 8:1 dimming ratios are 89\%, 88\% and 85.4\%, respectively. This LED driver is best suitable for backlight LED display.

Semiconductor Losses of PWM Buck DC-AC Converter Operated as Dynamic Power Supply 233
Thomas Salvatierra (Wright State University), Agasthya Ayachit (Wright State University), Dalvir K. Saini (Wright State University), Marian K. Kazimierczuk (Wright State University)

This paper presents a method for calculating the semiconductor losses in asynchronous and synchronous PWM buck converters operated as a fixed-Vi, fixed-Rload, variable-Vo dynamic power supply. Equations are derived for all MOSFET switching and conduction losses in both circuits, as well as diode conduction and forward-voltage losses. This work provides a means of direct comparison of the two popular topologies from the perspective of semiconductor power loss to determine which circuit is inherently more lossy. The low-side switching MOSFET of the synchronous variant is shown via calculation and circuit simulation to contribute the most significant power loss, thus demonstrating the asynchronous topology is more efficient for variable output voltage operation if designs are comparable.

Regenerative Synchronous Electrical Charge Extraction for Highly Coupled Piezoelectric Generators 237
Adrien Morel (CEA, LETI), Gaël Pillonnet (CEA, LETI), Adrien Badel (Université Savoie Mont Blanc)

This paper proposes a new strategy for vibration harvesting using piezoelectric material. This work relies on an adaptation of the classical Synchronous Electrical Charge Extraction (SECE). Instead of harvesting the energy at every displacement extremum, we choose to wait a certain number of extremum before harvesting the accumulated energy. This technique extends the harvested power compared to SECE, especially with highly coupled piezoelectric generators. Measurements on a piezoelectric energy harvester exhibiting a large coupling coefficient have been realized and have proven the efficiency and potential of this technique (193% harvested power improvement at resonance compared with a standard SECE strategy).

Design and Implementation of Home Energy and Power Management and Control System 241
Vanessa Barnes (University of Ghana), Thomas K. Collins (University of Ghana), Godfrey A. Mills (University of Ghana)

This work presents the design and implementation of a home energy and power management system that enables users to monitor, regulate and manage their demand response through scheduling and controlling of their appliances using a mobile application. The system consists of a microcontroller which communicates with a Raspberry pi server using Bluetooth communication. The mobile application communicates with the system via the Raspberry Pi server using Wi-Fi communication protocol. This system allows the user to self-regulate the amount of power usage, which translates into cost savings with the overall effect of flattening of the demand peaks.

Session A2P-K: Biomedical Circuits III

Chair: Jacob Rosenstein, *Brown University*
Co-Chair: Benoit Gosselin, *Laval University*
Time: Monday, August 7, 2017, 13:00 - 14:20
Location: Ballou Hall - Coolidge Room

Concentric Helical Coils for Efficient and Resilient Wireless Link in Biomedical Implants 245
Ehsan Ashoori (Michigan State University), Andrew J. Mason (Michigan State University)

Wireless transceivers for biomedical implants suffer from low coupling coefficients and variations due to misalignment. This paper introduces concentric helical coils for wireless power transmission in implantable devices. The transmitter coil can be implemented in any continuous circle form, such as a bracelet, an arm cuff, or a collar. It is shown that this structure produces a high coupling coefficient that is less sensitive than conventional methods to coil misalignment. Furthermore, this approach reduces expose of living tissue to electromagnetic power density, enabling a higher level of power to be safely transferred. A high mutual inductance between transmitter and receiver coils (k=0.44) is achieved, and this decreases no more than 19.9% with the worst case of misalignment. This high coupling along with high coil quality factors (Q=470, 195) enable a high power transfer efficiency of η=93.6%. This power transfer efficiency is also very resilient to misalignment of coils, with a worst case decrease of only 9%.

Design and Simulation of Nano Plasmonic Biosensors 249
Sina Pourjabar (Texas A&M University), Mona Zaghloul (George Washington University)

Nano plasmonic biosensor is composed of metallic nanoparticles on a dielectric substrate. In a certain wavelength of the incident light these metallic nanoparticles create a strong localized electric field that is extremely sensitive to an adjacent material, creating a highly sensitive sensor. Producing a higher electric field results in a more sensitive sensor for detection of biomolecules. In this work, 2 different nano structures were studied to find the structure producing a higher amount of electric field with a narrower linewidth which results in a more sensitive sensor for detection. In addition, a bow tie nanoantenna with the optimum size was studied and was able to produce an enhanced electric field of 90 times of the incident electric field

A Sub-µW CMOS Temperature to Frequency Sensor for Implantable Devices 253
Ava Hedayatipour (University of Tennessee), Aysha Siddique Shanta (University of Tennessee), Nicole McFarlane (University of Tennessee)

In this paper an ultra-low power CMOS temperature sensor for bio-implantable applications is implemented in a 0.18 um CMOS process. Sensors used in bio-implantable devices must have sub-uW power consumption to avoid tissue overheating, thus this temperature sensor employs subthreshold MOS as the sensing element to reduce power consumption and enable minimum supply voltage. Temperature is converted to frequency using a pW voltage reference. With the sensor core operating under 0.5 V, the sensor dissipates a total power of 290 nW and achieves temperature measurement of changes smaller than 0.5 °C from 0 °C to 50 °C.

Digitally Assisted Analog Processing Unit for MPG based Wearable Device 257
Himanshu Chaudhary (Indian Institute of Technology Kharagpur), Sangamesh Kodge (Indian Institute of Technology Kharagpur), Mrigank Sharad (Indian Institute of Technology Kharagpur)

Efficient and smart techniques for analog data acquisition and processing may play crucial role in the design of miniature wearable devices, meant to continuously record, process and wirelessly transmit vital physiological parameters for real time health monitoring. In this work we propose a low-power, all-analog processing unit for an MPG (magneto-plethysmograph) based wearable device, which is meant to detect heart-rate and respiration rate with the help of a megnto-resistive sensor. The analog unit constituting of functional units like the frontend amplifier, filters and comparators relies on digital calibration for adjusting the block parameters like gain and bandwidth, in order to swiftly track the changes in the signal characteristics, without relying on continuous digital signal processing like FFT. This leads to significant power saving due to of ADC and DSP operation, otherwise commonly employed for ensuring tracking of wide parameter range of such physiological parameters.

Session A2P-L: Digital Filters: Architectures and Applications

Chair: Manuel Jimenez, *University of Puerto Rico Mayaguez*
Co-Chair: Jabulani Nyathi, *EWU Engineering and Design*
Time: Monday, August 7, 2017, 13:00 - 14:20
Location: Ballou Hall - Coolidge Room

Design of Second-Degree IIR Digital Differentiators without Frequency Sampling and Recursive Optimization 261
Masayoshi Nakamoto (Hiroshima University), Naoyuki Aikawa (Tokyo University of Science)

We treat the design problem of second-degree IIR digital differentiators. The design problem (cost function) is formulated in the quadratic form without any frequency sampling. Since the cost function is the quadratic form, the solution is unique and the optimization scheme does not require any recursive optimization. Hence, the procedure of the design for the second-degree differentiators is very easy. Also, the second-degree differentiators obtained by our method have a robust stability since the maximum pole radius can be prescribed. Finally, we show a design example in order to demonstrate the effectiveness of the proposed method.

New 2-D Filter Architectures with Quadrantal Symmetry and Octagonal Symmetry and their Error Analysis 265
Pei-Yu Chen (National Chiao Tung University), Lan-Da Van (National Chiao Tung University), Hari C. Reddy (California State University-Long Beach), I.H. Khoo (California State University-Long Beach)

In this paper, two new two-dimensional (2-D) IIR and FIR filter architectures possessing quadrantal and octagonal symmetries are proposed. Furthermore, the theoretical error analysis for the proposed filters is also presented. Utilizing the presented error analysis, user can decide the bit width of the filters with satisfactory error tolerance.

Frequency and Amplitude Estimation of Noncircular Sinusoid using Complex Adaptive Notch Filters 269
Shotaro Nishimura (Shimane University), Aloys Mvuma (University of Dodoma), Takao Hinamoto (Hiroshima University)

In this paper, a technique for estimating frequency and amplitude of noncircular complex sinusoid has been presented. A cascade scheme of first-order complex notch filters has been introduced where complex sequence with negative frequency is rejected in the first section and sequence with positive frequency is removed in the second section. Closed-form expression for bias and mean square error (MSE) for frequency estimation have been presented. By using band-pass outputs of first-order notch filters, amplitudes sinusoidal sequences with positive and negative frequencies have been also estimated. Computer simulations show the effectiveness of proposed analyses.

Designing High Order Low Delay Maximally Flat FIR Digital Differentiators with Equiripple Stopband 273
Takahiro Fujikawa (Tokyo University of Science), Takashi Yoshida (Tokyo University of Science), Naoyuki Aikawa (Tokyo University of Science)

The transfer function of low delay maximally flat in passband and equiripple in stopband (MFER) FIR Digital Differentiators (DDs) is defined as the difference between the stopband function and the passband function. The passband function and the stopband function realizes flatness characteristics and equiripple characteristics, respectively. In this article, we propose a design method of higher order low-pass/band-pass MFER FIR DDs than conventiona. In the proposed method, the passband function is chosen as the transfer function of the low delay low-pass/band-pass MF FIR DDs. The stopband function is designed by complex Remez.

Session A2P-M: FPGA Applications

Chair: Jabulani Nyathi, *EWU Engineering and Design*
Co-Chair: Manuel Jimenez, *University of Puerto Rico Mayaguez*
Time: Monday, August 7, 2017, 13:00 - 14:20
Location: Ballou Hall - Coolidge Room

Area-Optimized Lattice-Based Cryptographic Processor for Constrained Devices 277
Liu Dongsheng (Huazhong University of Science and Technology), Zhang Cong (Huazhong University of Science and Technology), Lin Hui (Wuhan University of Technology)

Lattice-based cryptography has been widely researched due to its quantum attack resistance and versatility, but a practical hardware implementation that suitable for constrained devices is still challenging. In this paper, a novel area-optimized Ring-LWE (Learning with Error) cryptographic processor is proposed. Effective structures are presented to solve the huge circuit consumption of high precision Gaussian sampling and modular multiplication in Ring-LWE public-key cryptosystem. The Ring-LWE processor is smaller than the current state of the art hardware implementations, occupying only 948 slices, 3 BRAMs and none DSP module on a Xilinx Spartan-6 FPGA. Additionally, this processor is designed with resistance to side-channel attack, while it can encrypt/decrypt 256-bit message in 1.4ms/0.4ms.

Deep Learning Binary Neural Network on an FPGA 281
Yuteng Zhou (Worcester Polytechnic Institute), Shrutika Redkar (Worcester Polytechnic Institute), Xinming Huang (Worcester Polytechnic Institute)

In deep learning, convolutional neural network (CNN) has been proven very efficient in the tasks such as image classification and object recognition. This paper presents FPGA design of an efficient CNN with binary weights and activations, also known as binary neural network (BNN). Weights and input activations are binarized to take only two values, +1 and -1. This reduces all the fixed-point multiplication operations in convolutional layers and fully connected layers to 1-bit XNOR operations. We introduce an efficient method to implement this BNN on an FPGA by utilizing on-chip memory only. When evaluating the CIFAR-10 benchmark, the proposed FPGA design can achieve a processing rate of 332,164 images per second with error rate of 13.92% using 1-bit quantized weights and activations.

FPGA-Based Frequent Items Counting using Matrix of Equality Comparators 285
Trong-Thuc Hoang (Ho Chi Minh City University of Science), Xuan-Thuan Nguyen (University of Electro-Communications), Hong-Thu Nguyen (University of Electro-Communications), Nhu-Quynh Truong (Ho Chi Minh City University of Science), Duc-Hung Le (Ho Chi Minh City University of Science), Katsumi Inoue (Advanced Original Technologies Co., Ltd.), Cong-Kha Pham (University of Electro-Communications)

In this paper, an FPGA-based implementation of Frequent Items Counting is proposed. The architecture deploys the equality comparator matrix for comparing the input items with themselves to count them instantly within a single operating clock. The proposed architecture is applied to the case of the 8-bit item. That means 256 different types of items in total. The system is built and verified on the Altera Arria V SoC Development Kit. The experimental results show that the implementation can perform on the maximum clock frequency of 40.85 MHz and requires 51,094 ALUTs and 8,417 registers, which is about 29% of the FPGA's resources. The average throughput performance achieves 1,280 millions items per second, which is about 50 times faster than that of the software-based application at the same setting.

Session A3L-A: Analog Circuits and Systems II

Chair: Punith Surkanti, *Nokia*
Co-Chair: Marvin Onabajo, *Northeastern University*
Time: Monday, August 7, 2017, 14:40 - 16:20
Location: Braker Hall 001

Spatiotemporal Compressed Sensing for Video Compression 289
Tao Xiong (Johns Hopkins University), John Rattray (Johns Hopkins University), Jie Zhang (Massachusetts Institute of Technology), Chetan Singh Thakur (Johns Hopkins University), Sang Peter Chin (Johns Hopkins University / Boston University), Trac D. Tran (Johns Hopkins University), Ralph Etienne-Cummings (Johns Hopkins University)

We present an on-chip spatiotemporal compressed sensing (CS) framework for video compression. Our framework incorporates random sampling in both spatial and temporal domains to encode a video scene into a single coded image prior to A/D conversion. During decoding, the video is reconstructed using dictionary learning and sparse recovery. We have previously utilized this CS framework to build a low power real-time CMOS Integrated Circuit with an energy efficiency of 0.7 nJ/pixel. Here, we constructed a detailed simulation analysis to compare the compression rate and reconstruction quality with the state of the art MPEG compression algorithm. We demonstrate that our CS based method achieves a high compression rate (10:1-30:1) and a robust reconstruction quality (>20 dB) on a noisy database and shows better performance than a standard MPEG video compression technique.

Power Analysis and Maximum Output-Power Scheme for Inductively Coupled Resonant Power Receivers 293
Nan Xing (Georgia Institute of Technology), Gabriel A. Rincón-Mora (Georgia Institute of Technology)

Although microsensors nowadays can save money, energy, and lives, highly functional devices can exhaust a tiny battery very quickly. Harvesting ambient energy can help replenish the battery, but only when an ambient source is available. Unfortunately, many embedded microsensors are small, stationary, and enclosed, so thermal gradients, motion, and light are absent. Wireless power in these cases is often the only option left. But since the receiving coil is small and centimeters away from the transmitter, drawn power is low. Switched resonant bridges are popular in this respect because they output more power with fewer components than their non-switched and non-resonant counterparts. But still, power can be so low that losses can be overwhelming. This paper introduces a power-loss analysis and proposes a skipping collection scheme that boosts output power. Analysis and simulations demonstrate how switched resonant bridges consume conduction and switching power and how skipping half cycles can boost output power.

High-Performance Continuous-Time MASH Sigma-Delta ADCs for Broadband Wireless Applications 297
Qiyuan Liu (Texas A&M University), Alexander Edward (Texas A&M University), Carlos Briseno-Vidrios (Texas A&M University), Negar Rashidi (Texas A&M University), Jose Silva-Martinez (Texas A&M University)

This paper focuses on design and analysis of multi-stage noise-shaping (MASH) sigma-delta modulators. Fundamentals and properties of MASH modulators are discussed. A detailed methodology on analyzing continuous-time MASH (CT-MASH) modulator based on the impulse invariant transformation is also described. Two design examples are discussed: a 130 nm CMOS CT-MASH 4-0 employing a digital pseudo-MASH compensation consumes 20mW and achieves 75 dB peak SNDR over a 15 MHz bandwidth; a 40 nm CMOS CT-MASH 2-2 architecture achieves peak SNDR of 74.4 dB within the signal bandwidth of 50.3 MHz with power consumption of 43.0 mW.

Low-Complexity N-Port ADCs using 2-D Δ-Σ Noise-Shaping for N-Element Array Receivers 301
A. Nikoofard (Case Western Reserve University), J. Liang (Case Western Reserve University), M. Twieg (Case Western Reserve University), S. Handagala (University of Akron), A. Madanayake (University of Akron), L. Belostotski (University of Calgary), S. Mandal (Case Western Reserve University)

A novel multi-dimensional noise-shaping method is proposed to extend delta-sigma modulation to the two-dimensional (2-D) (space, time) case. It uses spatial oversampling to provide another degree of freedom for ADC designers to shape quantization noise when temporal oversampling is limited. The method uses lossless discrete integrators (LDIs) to implement spatial integrators and is suitable for use in microwave and mm-wave array processing systems. The resulting 2-D noise shaping reduces the spectral overlap of a desired array signal with that of quantization noise. Shaped noise can then be removed from the region of support (ROS) of the array signal using 2-D filtering, thus improving the overall signal-to-quantization noise ratio (SQNR) and effective number of bits (ENOB). Simulation results from an integrated 64-channel converter in UMC 65nm CMOS prove the functionality of the approach. Experimental results from a board-level 64-channel converter are also presented.

An Open-Loop 28GHz 16-Phase Clock Generator in 28nm CMOS 305
Jiu Xiong (University of Texas at Dallas), Jin Liu (University of Texas at Dallas), Yucheng Dai (University of Texas at Dallas), Hlaing Minn (University of Texas at Dallas)

This paper presents an open-loop 28GHz 16-phase clock generator in 28nm CMOS technology. The open loop architecture is composed of 22.5° delay units and uses phase compensation to account for delay time variations. The 16-phase 28GHz clock generator consumes 14mW, leading to a power efficiency of 0.032mW/GHz/phase. The maximum phase error is 6° and the RMS phase error is 3° when the input frequency varies from 27GHz to 29GHz.

Session A3L-B: Special Session: Analog and Digital Circuit Design for the Internet of Everything

Chair: Taewook Kim, *Yonsei University*
Co-Chair: Kyungki Kim, *Daegu University*
Time: Monday, August 7, 2017, 14:40 - 16:20
Location: Eaton Hall 201

Special Session: Low Power LDPC Decoder using Adaptive Forced Convergence Algorithm 309
JeongHyeon Bae (Ajou University), ByungJun Choi (Opticis / Ajou University), MyungHoon Sunwoo (Ajou University)

LDPC codes have been applied in recent communication standards, such as WiFi, WiGig, and 10GBased-T Ethernet as a forward error correction code. However, LDPC codes require a large number of computational complexity for high performances. To solve this problem, various studies have been continuously performed for reducing computational complexity. In this paper, we propose an adaptive forced convergence algorithm to deactivate the variable nodes and check nodes for reducing the computational complexity using only one adaptive threshold value.

A 1 V 2.5 µW Fully-Differential ASK Demodulator with 12.5 pJ/bit FOM for Ultra-Low Power Biomedical Applications 313
Seungyeob Baik (Daegu Gyeongbuk Institute of Science and Technology), Arup K. George (Daegu Gyeongbuk Institute of Science and Technology), Minkyu Je (KAIST), Junghyup Lee (Daegu Gyeongbuk Institute of Science and Technology)

Wireless transceivers that receive data and power are important circuit blocks in implantable biomedical devices. In such wirelessly powered devices, supply and common-mode variations increase the error rate of the received data. In this paper we propose a fully-differential amplitude-shift-keying (ASK) demodulator for suppressing the effect of such undesired common mode variations on the received data. The proposed demodulator consists of a fully-differential envelope detector (ED) and programmable gain amplifier (PGA) that operates in the sub-threshold region, and a differential comparator that consumes only dynamic current. The proposed system is implemented in a 0.18 µm CMOS process and consumes 2.5 µA from a 1 V power supply. At a data rate of 200 kbps, this leads to an FOM of 12.5 pJ/bit.

Low Power Asynchronous Circuit Design Methodology using a New Single Gate Sleep Convention Logic (SG-SCL) 317
Jin Kyung Lee (Daegu University), Kyung Ki Kim (Daegu University)

This paper proposes an asynchronous circuit design methodology using a new Single Gate Sleep Convention Logic (SG-SCL) with advantages such as low area overhead, low power consumption compared with the conventional null convention logic (NCL) methodologies. The delay-insensitive NCL asynchronous circuits consist of dual-rail structures using {DATA0, DATA1, NULL} encoding which carry a significant area overhead by comparison with single-rail structures. The area overhead can lead to high power consumption. In this paper, the proposed single gate SCL deploys a power gating structure for a new {DATA, SLEEP} encoding to achieve low area overhead and low power consumption maintaining high performance during DATA cycle. 4x4 multipliers have been designed in a 45nm predictive technology using the proposed SG-SCL gates and pipeline structure and using the conventional MTNCL (Safe SECRII architecture), and they have been compared in terms of speed, power consumption, energy and size. The simulation results show that the proposed design reduces 60% energy and 54% leakage power compared to the MTNCL (Safe SECRII architecture) design.

Subthreshold SRAM: Challenges, Design Decisions, and Solutions 321
Harsh N. Patel (University of Virginia), Farah B. Yahya (University of Virginia), Benton H. Calhoun (University of Virginia)

This paper presents an overview of various challenges, optimization strategies, and design requirements for subthreshold SRAM arrays targeting Ultra-Low Power (ULP) applications in the Internet of Things (IoTs). We study the impact of threshold voltage (VT) change due to process and temperature variations on various SRAM design decisions for ULP operation. We explore different solutions to enable reliable subthreshold operation ranging from technology to cell to architecture and assist. We also highlight the impact of process variations on optimal peripheral assist selection, and degree of assist requirements. We present trade-offs between reliability, energy, and performance to an application-specific SRAM design. Six different types of SRAM bitcells are compared for various subthreshold metrics to provide an optimal bitcell selection for the targeted application.

A Compressive Sensing Information Aware Analog Front End for IoT Sensors using Adaptive Clocking Techniques 325
Arya A. Rahimi (Washington State University), Huan Hu (Washington State University), Subhanshu Gupta (Washington State University)

Compressive sensing (CS) is a recent signal processing paradigm that exploits the inherent sparsity in input signal through data compression before wireless transmission. Recent CS implementations have shown impressive energy-efficiencies with good signal recovery but require apriori sparsity estimation and are thus not adaptable dynamic IoT environments resulting in loss of accuracy. This paper describes an information-aware compressive sensing architecture that leverages advances in data analytics to achieve ultra low-power operation while maintaining high reconstruction accuracy. Matrix-multiplication for feature-extraction and classification are implemented through scalable and reconfigurable switched-capacitor design approaches with variable power consumption up to 3 uW. The outcome of this approach enables transmission of either features, compressed or raw data as desired to achieve higher SNR at lower overall power consumption.

Session A3L-C: Power Management I

Chair: Robert Ashton, *Naval Postgraduate School*
Time: Monday, August 7, 2017, 14:40 - 16:20
Location: Eaton Hall 202

Solar/Wind Hybrid Energy Harvesting for Supercapacitor-Based Embedded Systems 329
Mohamadhadi Habibzadeh (State University of New York at Albany), Moeen Hassanalieragh (University of Rochester), Tolga Soyata (State University of New York at Albany), Gaurav Sharma (University of Rochester)

Autonomous embedded systems that rely solely on solar power may face intermittent interruptions during nights and cloudy days. A hybrid solar/wind energy supply could alleviate this problem. Supercapacitor buffering of energy in embedded systems has seen interest in the research community due to the superior energy predictability, low maintenance, and environmental friendliness of supercapacitors. In this paper, a systematic design of an energy harvesting system is presented that is capable of harvesting hybrid solar/wind energy and buffering to supercapacitors. Multiple alternative hybrid harvesting circuit designs are proposed and experimental results are provided.

A Self-Start Power Management Circuit for the Piezoelectric Energy Harvester of Speed Bump 333
Nan Chen (Northwestern Polytechnical University), Tingcun Wei (Northwestern Polytechnical University), Hyun Jun Jung (University of Maryland Baltimore County)

A self-start and self-powered power management circuit for impact-type piezoelectric energy harvester for speed bump is proposed. The piezoelectric impact-type cantilever was used to harvest the energy from speed bump as it is suitable for converting the low-frequency mechanical impact to high-frequency vibrations. Considering that vehicles passing speed bump are intermittent and random, a start-up circuit for this power management circuit is designed to save energy during the vacancy of electric energy. This start-up circuit also realizes the self-start and self-powered functions, when rechargeable battery is completely empty, the power management circuit can still transfer energy to load side. The experimental results show that the efficiency of the energy harvesting circuit is approximately 72% for the vehicle speeds of 5-20 km/h, and the controller of the energy harvesting circuit in active mode consumes 3.7% of input energy for the vehicle speed of 20 km/h, and don't loss power in sleep mode.

10 µW Converter for Energy Harvesting from Sedimentary Microbial Fuel Cells 337
A. Capitaine (CEA, LETI), G. Pillonnet (CEA, LETI), T. Chailloux (CEA, LETI), O. Ondel (Ampère), B. Allard (Ampère)

Sedimentary microbial fuel cells are promising harvesting systems generating powers as low as 10 µW, which is sufficient for powering underwater environmental sensors. This paper proposes a methodology and modeling to design a flyback converter in discontinuous conduction mode harvesting powers as low as 10th of µWs to maximize the harvested energy and boost its voltage to a minimum value required by sensors. Using a model validated experimentally, we figure out the converter loss contributors and balance them to maximize the power efficiency. We achieved 28% and 75%, efficiency with an input power of 10 µW and 30 µW respectively.

2Vrms 16Ω Switching Headphone Driver with 82% Peak Efficiency, 102 dB SNDR and 1.1mA/Channel Quiescent Current 341
Khaled M. Abdelfattah (University of California-Irvine), Michael M. Green (University of California-Irvine)

A new headphone driver IC based on a switching output stage in continuous conduction mode is described. The driver uses a sliding-mode peak-valley control scheme to regulate the inductor current. The output stage is switched between the battery voltage and the output of an integrated non-regulated inverting charge pump, and a second-order loop filter is used to regulate the output voltage. The system achieves a 2Vrms output audio signal to a 16Ω load while consuming a quiescent average current of 1.1mA/channel and 82% peak efficiency. Peak SNDR is about 102dB, A-weighted DR is 108dB, and the PSRR is more than 120dB.

A 16A, 2.5MHz Multi-Phase DC-DC Switching Converter with Low Standby Power Consumption for Mobile Applications 345
Shuyu Zhang (Zhejiang University), Menglian Zhao (Zhejiang University), Zhao Yang (Zhejiang University), Xuetong Bai (Zhejiang University), Xiaobo Wu (Zhejiang University)

To meet the demands of modern mobile devices on higher current and longer standby time, a novel 2.5MHz high driving capability multi-phase buck converter with low standby power consumption is proposed. The converter could supply maximum load current of 16A with four interleaved phases. By transferring the control scheme from adaptive-on-time (AOT) mode to pulse-frequency-modulation (PFM) mode, the efficiency at light load could be improved. With phase-shedding, the power consumption of the controller can be reduced by up to 72% and the standby quiescent current is as low as 7 µA.

Session A3L-D: Student Paper Contest II

Chair: Ken Jenkins, *Pennsylvania State University*
Time: Monday, August 7, 2017, 14:40 - 16:20
Location: Eaton Hall 203

A Medium-Grained Reconfigurable Architecture Targeting High-Level Synthesis Implementation 349
Jason Gorski (Oakland University), Darrin Hanna (Oakland University)

High-level synthesis is increasingly being used to automatically translate existing software algorithms into hardware quickly and efficiently. Typically, the circuits created by HLS are implemented on Field-Programmable Gate Arrays (FPGAs). While the fine-grained architecture of an FPGA is well suited for general circuit implementation, it can result in excessive routing resource utilization for larger dataflow circuits such as those generated by HLS. As an alternative, we present a medium grained reconfigurable architecture tailored to implementing HLS generated circuits. The proposed architecture achieves a 5.4x reduction in critical path delay compared to a standard FPGA during initial testing.

Constant-Based Truncated Cubing Architectures 353
Son Bui (Oklahoma State University), James E. Stine (Oklahoma State University)

A new technique for computing the truncated cube of an operand at length of power two is proposed, implemented, analyzed, and compared to existing techniques. The new proposed method is comparable to previously proposed methods that compute the cube of an operand in parallel. Post layout results are presented in a 65nm Application Specific Integrated Circuit implementation and are compared against previous methods. Results demonstrate an area reduction of 3 compared to previous cubing architectures and considerable energy reduction using truncated cubing architectures.

A Low Noise, Inductor-Less, Integer-N RF Synthesizer using Phase-Locked Loop with Reference Injection (PLL-RI) 357
Feiran Lei (Ohio State University), Marvin H. White (Ohio State University)

In this paper, a Reference Injected Phase-Locked Loop (PLL-RI) with delay-line ring-type oscillator is employed to implement an integer-N frequency synthesizer to achieve low phase noise and better locking behavior. This inductor-less PLL-RI is fabricated in a 1.2V, 130nm RF CMOS process with a 0.5-1.7GHz tracking range in a 0.02 mm2 core area. Simulation and measurement results show phase noise reduction and improved settling behavior of a PLL-RI synthesizer compared to a conventional synthesizer. Integrated RMS phase jitter from 10KHz to 30MHz is 0.84ps with a power consumption of 2.6mW at a 1GHz frequency.

A Synchronized Axon Hillock Neuron for Memristive Neuromorphic Systems 361
Ryan Weiss (University of Tennessee), Gangotree Chakma (University of Tennessee), Garrett S. Rose (University of Tennessee)

In this paper we present circuit techniques to optimize analog neurons specifically for operation in memristive neuromorphic systems. Since the peripheral circuits and control signals of the system are digital in nature, we take a mixed-signal circuit design approach to leverage analog computation in multiplying and accumulating digital input spikes and generate binary spikes as outputs to be consistent with surrounding synchronous digital logic circuits. A novel approach for synchronization is leveraged based on domino logic. The principal advantage of utilizing analog neurons within an overall digital system design is to ensure efficiency in size and power consumption. Energy per spike was determined to be 20 fJ, based on Cadence Spectre simulations of the proposed domino-based neural circuit.

Closed Form Delay Models for Buffer-Driven TSVs in 3D On-Chip Memory 365
Xiaowei Chen (North Dakota State University), Seyed Alireza Pourbakhsh (North Dakota State University), Na Gong (North Dakota State University), Jinhui Wang (North Dakota State University)

Buffer-driven TSVs (BD-TSV) are widely used in 3D on-chip memories, especially in bit-line circuit that is highly sensitive to delay time. Closed form delay models for BD-TSVs are proposed in this paper and are verified by simulation through a 128 KB 3D on-chip memory in both 180 nm and 16 nm technology. Results show that the error rate of models is less than 8.9%, which can be accepted in the design flow.

Session A3L-E: Biomedical Circuits I

Chair: Benoit Gosselin, *Laval University*
Time: Monday, August 7, 2017, 14:40 - 16:20
Location: Eaton Hall 206

Fully Discrete-Time Neural Recording Front-Ends: Feasibility and Design Considerations 369
Hossein Kassiri (York University)

The ever-increasing need for higher number of recording channels along with the stringent power and area requirements of a brain-implantable device, demand for novel ultra-compact and low power architectures. In this paper, we will first briefly discuss the fundamental scaling issues of conventional AC- and DC-coupled neural front-end architectures. Next, we will analytically examine the feasibility of a fully discrete-time neural front-end as an alternative, and will go over various design trade-offs that must be considered.

Catheter-Mounted CMOS Front-Ends for Broadband Intravascular Ultrasonic Imaging 373
Steve J.A. Majerus (Louis Stokes Cleveland VA Medical Center), Soumyajit Mandal (Case Western Reserve University), Aaron Fleischman (Cleveland Clinic Lerner Research Institute)

Intravascular ultrasonic (IVUS) imaging catheters use piezoelectric transducers to form radial images of blood vessel walls. Here, we present the design and optimization of an integrated CMOS front-end for integration on a 0.8-mm imaging catheter with a high-impedance polymer transducer. Noise optimization revealed that an impedance-matching optimum exists, which balances the system parasitic capacitances relative to the transducer impedance. Optimized design equations compared favorably to simulation results in predicting front-end bandwidth and transducer-referred SNR. The fully integrated front-end measured 0.74 x 1.8 mm, with a low imaging noise floor and wide imaging bandwidth.

CMOS-Based Opto-Electric Neural Interface Devices for Optogenetics 377
Takashi Tokuda (Nara Institute of Science and Technology), Makito Haruta (Nara Institute of Science and Technology), Toshihiko Noda (Nara Institute of Science and Technology), Kiyotaka Sasagawa (Nara Institute of Science and Technology), Jun Ohta (Nara Institute of Science and Technology)

In this study, CMOS-based on-chip neural interface devices with integrated optical stimulation capability are presented. The devices are designed for use in optogenetic applications. Two types of neural stimulators are presented. In one type, the on-chip CMOS image sensor was integrated with blue LEDs. Variations of device structures were developed as well. An in vivo experimental demonstration using a mouse was successfully performed. We also proposed and developed the structure of an opto-electric neural interface device with wide-area coverage. Multi-node device architecture including multiple CMOS chips is proposed for this type and its functionality is demonstrated.

Towards a Free-Floating Wireless Implantable Optogenetic Stimulating System 381
Yaoyao Jia (Georgia Institute of Technology), Byunghun Lee (Georgia Institute of Technology), S. Abdollah Mirbozorgi (Georgia Institute of Technology), Maysam Ghovanloo (Georgia Institute of Technology), Wasif Khan (Michigan State University), Wen Li (Michigan State University)

This paper presents a wirelessly-powered and free-floating implantable optogenetic stimulating (FF-WIOS) implant with negligible footprint and high power transfer efficiency (PTE). FF-WIOS ASIC with embedded µLED and reflective lens is expected to stimulate the target cortical neuronal ensembles at high temporal and spatial resolution with minimal damage and no tethering effects. To improve the PTE, and stay below the SAR limit, a flexible planar transmitter (Tx) resonator, L2, will be implanted under the scalp, but over the skull. The Tx coil, L1, embedded in a headstage, L2 resonator, and a wire-bond receiver (Rx) coil, L3, wound around the FF-WIOS device, form a 3-coil inductive link operating at 135 MHz, which directly charges a surface-mount storage capacitor. At the onset of stimulation, the storage capacitor discharges into the µLED, while the stimulation parameters are sent to FF-WIOS by amplitude modulating of the power carrier. Post-layout simulation results show functionality of the storage capacitor charging, forward data transmission, and optogenetic stimulation with adjustable parameters.

An 11-Bit 250-nW 10-kS/s SAR ADC with Doubled Input Range for Biomedical Applications 385
Mahmoud Sadollahi (Oregon State University), Gabor Temes (Oregon State University)

This paper presents a low power, area efficient 11-bit single-ended successive-approximation-register (SAR) analog-to-digital converter (ADC) with small loading effect targeted for biomedical applications. The design features an energy-efficient switching technique with an error cancelling capacitor network to cover an input range twice the reference voltage. The ADC's loading effect to previous stage is reduced by using single-ended structure and eliminating the largest capacitor in switching network. The common-mode voltage of the input signal, generated by other blocks, can be used as reference voltage. All building blocks were designed in subthreshold for power efficiency, with asynchronous self-controlled SAR logic. The ADC was fabricated in a 0.18 µm CMOS 2P4M process. The measured peak SNDR was 60.5 dB, the SFDR was 72 dB, the DNL +0.6/-0.37 LSB and the INL +0.94/-0.89 LSB. The total power consumption was 250 nW from a 0.75 V supply voltage.

Session A3L-F: Digital Circuits and Systems II

Chair: Sameer Sonkusale, *Tufts University*
Co-Chair: Jose Delgado-Frias, *Washington State University*
Time: Monday, August 7, 2017, 14:40 - 16:20
Location: Paige Hall - Crane Room

Firmware Functional Validation using a Colored Petri Net Model 389
Rongyang Liu (Washington State University), José G. Delgado-Frias (Washington State University), Doug Boyce (Washington State University), Rahul Khanna (Intel Corporation)

Unified Extensible Firmware Interface (UEFI) requires a functional validation during system testing which is becoming more complex and time-consuming. We have proposed a novel technique which can automatically generate Colored Petri Net (CPN) from the UEFI firmware source code and use CPN simulation to keep track of the UEFI execution step-by-step at run-time. CPN simulations indicate where the execution departs from a normal path which helps to determine the root cause of the problem. A case study on the functional validation of UEFI USB Bus driver of a commercial embedded platform is used to demonstrate the proposed validation technique.

The Effects of Radiation-Induced Soft Errors on Hardware Implementations of Object-Tracking Algorithms 393
Hao Qiu (Vanderbilt University), Richard A. Peters (Vanderbilt University), William H. Robinson (Vanderbilt University), Daniel B. Limbrick (North Carolina Agricultural and Technical State University)

Hardware implementations of Object-Tracking Algorithms, like most integrated circuits, are susceptible to radiation-induced soft errors. This work evaluated the reliability of a FPGA implementation of object-tracking algorithms via fault emulation experiments conducted at the register-transfer level (RTL). Faults were injected to the main sub-modules within the object-tracking system. The results show that RTL faults can cause observable errors in the system outputs. The level of degradation is related to the fault injection location as well as the type of fault.

Improving Alias Rejection in Comb Decimation Filters for Odd Decimation Factors 397
Gordana Jovanovic Dolecek (INAOE), Jose Carmona Suarez (INAOE)

This paper presents a two-stage comb decimation filter for odd decimation factors, which are factors of three. The first stage is a comb decimated by one third of the overall decimation factor, while the second stage is a comb, decimated by three. The aliasing rejection is improved by cascading a simple multiplierless filter in the second stage. As a consequence, the aliasing rejection is improved in all folding bands but third, sixth, ninth, etc. Mathematical background for the choice of the filter in the second stage is provided. The comb filters in both stages can be implemented either in recursive or nonrecursive forms. The comparisons with some methods, recently proposed in literature, show the benefit of the proposed method.

Session A3L-G: Processor and Memory

Chair: Mingoo Seok, *Columbia University*
Co-Chair: Sudhanshu Khanna, *Texas Instruments*
Time: Monday, August 7, 2017, 14:40 - 16:20
Location: Paige Hall - Terrace Room

A Content Addressable Memory with Multi-Vdd Scheme for Low Power Tunable Operation 401
Siddhartha Joshi (Northwestern University), Dawei Li (Northwestern University), Seda Ogrenci-Memik (Northwestern University), Grzegorz Deptuch (Fermi National Accelerator Laboratory), James Hoff (Fermi National Accelerator Laboratory), Sergo Jindariani (Fermi National Accelerator Laboratory), Tiehui Liu (Fermi National Accelerator Laboratory), Jamieson Olsen (Fermi National Accelerator Laboratory), Nhan Tran (Fermi National Accelerator Laboratory)

This paper reports on a content addressable memory (CAM) employing a multi-Vdd scheme for low power pattern recognition applications. The complete design, simulation and testing of the chip is presented along with an exploration of the multi-Vdd design space. The proposed design, operating at an optimal operating point in a triple-Vdd configuration, increases the delay range by 2.4 times and consumes 25.3% less power when compared to a conventional single-Vdd design operating over the same voltage range. Measurement results from a 246 kb test chip fabricated in 130nm Global Foundries Low Power CMOS technology are presented to validate the model and analysis.

gMRAM: Gain-Cell Magnetoresistive Random Access Memory for High Density Embedded Storage and in-Situ Computing 405
Mohammad Kazemi (University of Rochester), Mark F. Bocko (University of Rochester)

High density embedded memories have been demanded increasingly in a wide variety of applications to enhance the performance and reduce the power dissipation. In this paper, a memory cell, referred to as the gain-cell magnetoresistive random access memory (gMRAM), is introduced. The gMRAM significantly reduces the cell area per bit as compared to state-of-the-art embedded memories and possesses natural basis for in-situ computing. A gMRAM cell simultaneously retains two bits, a nonvolatile bit using a magnetic tunnel junction (MTJ) and a dynamic bit using the access transistor of the MTJ. The two bits are independently and nondestructively accessible for read and write. Simulation results from an 8 Kb gMRAM array using a 14nm standard CMOS technology demonstrate a 750 ps / 475 ps access time for dynamic read/write, while the nonvolatile bit can be read from or written to the same cell with a, respectively, 750 ps and 3.5 ns access time. The gMRAM cell area per bit is 3x (2x) smaller than a SRAM (3T eDRAM) cell in the same technology.

Interleaved Logic-in-Memory Architecture for Energy-Efficient Fine-Grained Data Processing 409
Kai Yang (University of Florida), Robert Karam (University of Florida), Swarup Bhunia (University of Florida)

We propose a novel interleaved logic-in-memory architecture, referred to as MISK, which leverages fine-grained integration of logic functions within SRAM arrays for in-situ information processing. It can greatly improve the performance for data-intensive applications by reducing the number of data transfer accesses. Results are compared to an unmodified OpenRISC CPU, demonstrating an average 1.9x latency reduction and 1.6x increase in energy efficiency, while contributing only 9% additional area overhead compared to a MISK-free CPU.

Variability Tolerant Reading of Nanomagnetic Energy Minimizing Co-Processor 413
Kawsher A. Roxy (University of South Florida), Sanjukta Bhanja (University of South Florida)

A recently proposed novel nanomagnetic co-processor harnesses the quadratic Hamiltonian of a system of coupled nanomagnets in order to solve quadratic optimization problems. The key principle here is "Let physics do the computation" in the sense that the relaxation physics of a grid of nanomagnets directly solve the optimization problem. More interestingly, our preliminary research suggests that the performance of this co-processor is independent of problem size. Relaxed magnetic states of the co-processor translate the output of the original problem. Since the framework of this co-processor is similar to that of STT-MRAM memories, we can leverage the heterogeneous integration with CMOS technologies for access, control and reading the cells. This paper focuses on an efficient reading of the magnetic cells and also addresses the effects of resistance variations. Based on the framework, the read mechanism should be able to distinguish between the inplane single domain and vortex domain states. Unlike STT-MRAM, the circular magnets do not have shape anisotropy but, here we show that with an additional pre-amplifier circuit, we are able to improve sense margin by at least 73\%.

High Resolution, Self-Compensated, Sense Amplifier for FRAM Technology 417
Robert A. Glazewski (Texas Instruments Inc.), Stefano Poli (Texas Instruments Inc.), Kurt Schwartz (Texas Instruments Inc.), Scott L. Leisen (Texas Instruments Inc.), Bill Kraus (Texas Instruments Inc.), Stephen K. Heinrich-Barna (Texas Instruments Inc.)

Ferroelectric RAM (FRAM) is a non-volatile memory with fast, low power, high endurance, read and write operations. Hence, this technology remains an attractive choice for embedded system solutions. In this paper, we analyze Si data that initiated the effort to design a compensated Sense Amplifier (SA) with improved input offset-sigma. We evaluate the cost vs benefit tradeoffs associated with this metal-cap based approach to offset compensation. Lastly, we present design improvements which will preserve the benefits of SA with compensation while reducing the cost. In this work we propose a self-compensated and high resolution SA, in 130nm FRAM technology, which will enable a more accurate and consistent delineation of smaller signal margins.

Session A4L-A: Special Session: Emerging Neuromorphic Circuits for Enabling Deep Neural Networks

Chair: Rashmi Jha, *University of Cincinnati*
Co-Chair: Swaroop Ghosh, *Pennsylvania State University*
Time: Monday, August 7, 2017, 16:40 - 18:20
Location: Braker Hall 001

Analog CMOS-Based Resistive Processing Unit for Deep Neural Network Training 422
Seyoung Kim (IBM Thomas J. Watson Research Center), Tayfun Gokmen (IBM Thomas J. Watson Research Center), Hyung-Min Lee (Korea University), Wilfried E. Haensch (IBM Thomas J. Watson Research Center)

Recently we have shown that an architecture based on resistive processing unit (RPU) devices has potential to achieve significant acceleration in deep neural network (DNN) training compared to today's software-based DNN implementations running on CPU/GPU. However, currently available device candidates based on non-volatile memory technologies do not satisfy all the requirements to realize the RPU concept. Here, we propose an analog CMOS-based RPU design (CMOS RPU) which can store and process data locally and can be operated in a massively parallel manner. We analyze various properties of the CMOS RPU to evaluate the functionality and feasibility for acceleration of DNN training.

Spiking Neural Networks – Algorithms, Hardware Implementations and Applications 426
Shruti R. Kulkarni (New Jersey Institute of Technology), Anakha V. Babu (New Jersey Institute of Technology), Bipin Rajendran (New Jersey Institute of Technology)

Spiking Neural Networks (SNNs) are the third generation of artificial neural networks that closely mimic the time encoding and information processing aspects of the human brain. It has been postulated that these networks are more efficient for realizing cognitive computing systems compared to second generation networks that are widely used in machine learning algorithms today. In this paper, we review the learning algorithms, hardware demonstrations and potential applications of SNN based learning systems.

Novel Spiking Neural Network Utilizing Short-Term and Long-Term Dynamics of 3-Terminal Resistive Crossbar Arrays 432
Sam Wenke (University of Cincinnati), Andrew Rush (University of Cincinnati), Tony Bailey (University of Cincinnati), Rashmi Jha (University of Cincinnati)

A spiking neuron and 3-terminal Resistive RAM (RRAM) model are proposed and simulated as a neural network. The system is analyzed as a complex network of spiking neurons connected by synapses to demonstrate a biologically-inspired associative memory. In recent years, Machine Learning and Artificial Intelligence have become popular fields due to readily available high performance computing systems such as GPUs. Contrary to CPU and GPU machines, biologically-inspired neu- romorphic hardware systems represent a distributed, in-memory computing alternative to solving complex problems. In this paper, we describe and simulate a process of training a crossbar of generalized 3-terminal RRAM devices to store and classify digits represented by matrices of analog currents.

Session A4L-B: Non-Linear Analog Systems

Chair: Jennifer Kitchen, *Arizona State University*
Co-Chair: Ayman Fayed, *Ohio State University*
Time: Monday, August 7, 2017, 16:40 - 18:20
Location: Eaton Hall 201

A Highly Sensitive RF-to-DC Power Converter with an Extended Dynamic Range 436
Abdullah Almansouri (King Abdullah University of Science and Technology), Mahmoud Ouda (King Abdullah University of Science and Technology), Khaled N. Salama (King Abdullah University of Science and Technology)

This paper proposes a highly sensitive RF-to-DC power converter with an extended dynamic range that is designed to operate at the medical band 433 MHz and simulated using 0.18 µm CMOS technology. Compared to the conventional fully cross-coupled rectifier, the proposed design offers 3.2× the dynamic range. It is also highly sensitive and requires -18 dBm of input power to produce a 1 V-output voltage when operating with a 100 kΩ load. Furthermore, the proposed design offers an open circuit sensitivity of -23.4 dBm and a peak power conversion efficiency of 67%.

A Buck Converter with Optimized Dynamic Response using Lag-Lead Active Voltage Positioning 440
Yongjie Jiang (Iowa State University), Ayman Fayed (Ohio State University)

This paper proposes a lag-lead Active Voltage Positioning (AVP) technique that can be used in buck converters to minimize their output voltage transients during dynamic events, such as load pulses. The proposed technique is based on optimizing the output impedance of the converter across a wide range of frequencies, and therefore, output voltage transients in response to both narrow and wide load pulses can be minimized without increasing the converter's main control loop bandwidth or the output capacitance. The proposed technique is verified with a 5-MHz buck converter design in 0.18-µm CMOS, where compared to conventional lag-only AVP designs, over 70% and 60% reduction in output voltage transients are achieved for wide and narrow load pulses respectively.

High Power Factor Wireless Power Transfer Front-End Circuit for Heterogeneous Systems 444
Philex Ming-Yan Fan (University of Cambridge), Hashem Zare-Hoseini (Huawei Technologies Co., Ltd), David G. Hasko (University of Cambridge), Arokia Nathan (University of Cambridge)

This paper investigates a high power factor switch-based wireless power transfer front-end circuit for heterogeneous systems. This circuit uses an integrated switching rectifier, implemented in 0.18um 1.8V/5V CMOS process. An integrated pair of phase synchronizers is used to align the waveshape of a wirelessly-coupled sinusoidal voltage source in the receiving coil to the corresponding conducting current. Using this approach, the power factor can be increased above 0.9 without requiring any wireless or wired feedback to the transmitter. The integrated switching rectifier can also provide: ac-dc rectification; facilitate the deployment of multi-receiver to single-transmitter wireless power transfer; and have the capability for voltage up and down conversion of the peak amplitude of the sinusoidal voltage source by use of a pulse-width modulation controller. From measured results, the output voltage can be stepped down from 1.65V to 1.08V and stepped up from 1.5V to 1.68V. Also, the measured power factor is 0.9 when the conducting current is managed at continuous conduction mode.

An Ultra-High Bandwidth Sub-Ranging ADC with Programmable Dynamic Range in 32nm CMOS SOI 448
Jen-Chieh Hsueh (Ohio State University), Vanessa Chen (Ohio State University), Jean-Oliver Plouchart (IBM Thomas J. Watson Research Center)

A 7GS/s 6b sub-ranging ADC is implemented in 32nm CMOS SOI with reconfigurable comparators, and adjustable input differential pairs are exploited to change converter characteristics for hardware-based cybersecurity. To achieve low-power consumption at high-speed operation with small-size transistors, an on-chip calibration to reduce process mismatches is utilized in the design. The presented ADC achieves an SNDR of 33.06 dB at Nyquist frequency and consumes only 15mW with a figure-of-merit of 58.3 fJ/conv-step.

Distortion and Its Suppression in Low-Power Delta-Sigma Modulator 452
Hiroki Ishikuro (Keio University)

In this paper, effects of amplifier distortion in DT sigma-delta modulator are discussed. A second order modulator with single-bit quantizer is modeled and dead-zone effect of ring amplifiers in integrators is simulated by using MATLAB. For the evaluation of dead-zone effect on modulator distortion, test chip was fabricated in 65nm CMOS. SNDR of 62dB and 1MHz signal bandwidth was experimentally demonstrated at sampling frequency of 102.4MHz and power consumption of 1mW.

Session A4L-C: Power Management II

Chair: Sudhir Kudva, *Nvidia*
Time: Monday, August 7, 2017, 16:40 - 18:20
Location: Eaton Hall 202

Design of Zero-Voltage-Ripple Buck DC-DC Converter 456
Dalvir K. Saini (Wright State University), Agasthya Ayachit (Wright State University), Thomas Salvatierra (Wright State University), Marian K. Kazimierczuk (Wright State University)

This paper presents the design of a zero-voltage-ripple (ZVR) buck dc-dc converter. The circuit uses an auto-transformer for ripple cancellation in the output voltage. The principle of operation is discussed in brief. The relationship between the currents through the magnetizing inductance and the auto-transformer windings is developed. The auxiliary inductance for ripple cancellation in series with the secondary winding is determined. The expression for the auxiliary inductance is derived. A laboratory prototype of a buck converter with supply voltage 12 V, output voltage voltage 5 V, switching frequency 500 kHz, and output power 10 W was built. Simulation and experimental results are provided validating the theoretical predictions.

Audio-Susceptibility of Inner Loop of True-Average Current-Mode Controlled Buck DC-DC Converter 460
Dalvir K. Saini (Wright State University), Marian K. Kazimierczuk (Wright State University)

The audio-susceptibility of the average current-mode controlled buck dc-dc converter in continuous-conduction mode is presented in this paper. The average current-mode control scheme used in this paper regulates the true average component of the sensed inductor current and is not affected by a high inductor current ripple at low duty ratios. The principle of negative feedback for converters with the average current-mode control is discussed in brief. The input voltage-to-inductor current disturbance transfer function is derived using the averaged, linear small-signal model. The loop gain transfer function has been analyzed to satisfy the closed-loop requirements. The closed-inner-loop input voltage-to-inductor current transfer function and the closed-inner-loop input-to-output voltage transfer functions are determined. An example buck converter is used and the characteristics are analyzed in detail. Simulation results are presented for the designed buck converter validating the theoretical predictions.

Modeling PWM DC-to-DC Power Converters using Graphs 464
Richard Marquez (Universidad Tecnológica de la Mixteca), Marco Antonio Contreras-Ordaz (Universidad Tecnológica de la Mixteca), José Luis Carrasco-Pacheco (Universidad Tecnológica de la Mixteca)

In this paper, we illustrate, through examples, a novel graph-based modeling technique of two-state (on-off) PWM power converters. %by using directed graphs. Differential equations of power converters are derived by inspection, based on the construction of two incident matrices, $\J(u)$ and $\beta(u)$, from appropriate digraphs. We associate to each circuit (on, $u=1$, or off, $u=0$, circuits) a digraph and identify current loops (inductor-capacitor, voltage source-inductor, current source-capacitor) in a natural way. Effectively, $\beta(u)$ and $\J(u)$ represents, resp., the core of energy injection and energy transfers inside a converter. These digraphs and incident matrices serve to obtain also classical dual models, evaluate semiconductor stresses, compute models for power converters with multiple states (active independent switches), and synthesize DC-to DC power converters. The proposed modeling method can be seen as a sort of modified nodal analysis based on graphs.

A Dual-Input High-Efficiency Li-ion Battery Charger with Current-Mode Smooth Transition and Ripple Reduction Circuits 468
Chung-Cheng Su (National Chiao Tung University), Yen-Wei Liu (National Chiao Tung University), Chung-Chih Hung (National Chiao Tung University)

A Li-ion battery charger with dual input source capability and high efficiency is proposed in this work. An internal source determination circuit could choose the sufficient energy source for charging system. A new approach of smooth transition to avoid oscillation between charging mode switching is used through current-mode-like smooth transition circuit. Pulse frequency modulation with adaptive off-time control is applied to the charger to reduce the requirement of compensation design. The charging current is controlled not only by the current loop but also through the ripple reduction circuit to suppress the increasing charging current ripple as the battery voltage rises.

Considering Effects of Parasitic Coupling to Ground in a Switching Power Amplifier 472
M. Bosworth (Florida State University), J. Langston (Florida State University), M. Steurer (Florida State University)

The future naval surface combatant will be an all-electric medium-voltage dc integrated power and energy system; capable of supporting future dynamic loads. Adoption of this system will introduce harmonic content and undesirable effects. The 5~MW PHIL testbed at the FSU-CAPS is used to interface actual power equipment, device(s) under test, to a real-time simulated environment through power amplifiers and/or actuators. To support future PHIL endeavors, it is necessary to better understand and mitigate impacts of high switching frequencies presented to the DUTs by the amplifiers of the testbed.

Session A4L-D: Signal Processing I

Chair: Stephen Adamshick, *WNEU*
Time: Monday, August 7, 2017, 16:40 - 18:20
Location: Eaton Hall 203

A Closed-Form Approach for Contiguous and Non-Contiguous Harmonic Elimination with Application to a Three-Level Switching Waveform 475
Sraddhanjoli Bhadra (University of Arkansas at Little Rock), Hirak Patangia (University of Arkansas at Little Rock)

An analytical approach is proposed for solving transcendental equations which are encountered in harmonic elimination. The disadvantage of numerical approach is choice of initial values that guarantee all possible solutions. The non-linear polynomials derived through Chebyshev expansion have been reformulated and their solution leads to a polynomial, the solution of which provides the switching angles. As an application, the complete solution for unipolar switching pattern eliminating up to ninth harmonic in single-phase and up to thirteenth harmonic in three-phase has been presented. Contrary to two solutions for triplen system in existing literature, three solutions have been found which shows the effectiveness of the closed-form solution.

A Discrete Fractional Hankel Transform based on the Eigen Decomposition of a Symmetric Kernel Matrix of the Discrete Hankel Transform 479
Magdy Tawfik Hanna (Fayoum University)

Recently a discrete Hankel transform (DHT) has been introduced using a symmetric involutary kernel matrix T. Although Namias contributed the fractional Hankel transform (FRHT) in 1980, no discrete counterpart has appeared till now. Here a definition is proposed for a discrete fractional Hankel transform (DFRHT) based on the eigen decomposition of the diagonalizable matrix T. Being an involutary matrix, T has only two distinct eigenvalues, namely 1 and -1. Being a real symmetric matrix, T has two orthogonal eigen spaces corresponding to its two distinct eigenvalues. Simple explicit expressions are derived for the orthogonal projection matrices of T on its eigen spaces by applying spectral decomposition. Expressions are derived for the dimensions of the two eigen spaces in terms of the trace of matrix T. The proposed DFRHT has the nice properties of unitarity, index additivity and reduction to the DHT in the nonfractional case. Orthonormal bases are generated for the two eigen spaces by the singular value decomposition of the orthogonal projection matrices.

Embedded FFT Hardware Algorithm Development using Automated Bi-Dimensional Scalable Folding 483
Felipe Minotta (Recinto Universitario de Mayagüez), Manuel Jiménez (Recinto Universitario de Mayagüez), Domingo Rodriguez (Recinto Universitario de Mayagüez)

This paper presents an original and unique embedded FFT hardware algorithm development process based on a systematic and scalable procedure for generating permutation-based address patterns for any power-of-2 transform size algorithm and any folding factor in a Kronecker Pease FFT hardware implementation. This is coupled by a procedure to perform automatic code generation of Kronecker FFT cores. The paper presents important results about twiddle address pattern generation and data switch multiplexing techniques. The paper also presents analyses and comparisons of the architecture design performance in terms of clock latency, accuracy, and hardware resources for benchmarking implementation efforts.

Design of a Low Cost DC / AC Inverter for Integration of Renewable Energy Sources into the Smart Grid 487
Joseph Tompkins (Western New England University), Matthew Musiak (Western New England University), Neeraj Magotra (Western New England University)

the Sun has the potential to provide 89,300 tera Watts of power to our planet. Our ability to convert even a fraction of this energy for human use makes a significant impact on current energy generation and consumption trends. World-wide we now add more renewable energy capacity every year than (combined) fossil fuel energy capacity. Solar panels provide a reliable, renewable, non-polluting energy source by converting the Sun's energy to electricity. The biggest challenge faced in this effort to 'mainstream' solar energy is system cost. The system presented in this paper addresses this by integrating readily available, low-to-moderately priced components into the inverter design. In order to reduce cost the system utilizes a motor control unit, in a novel way, as a switching device. Reliability of these systems is also an issue in the field and the system described in this paper addresses this issue by ensuring the use of components that have proven track records in industry and digital control allows for robustness, flexibility and scalability of the design.

Session A4L-E: Biomedical Circuits II

Chair: Matthew Johnston, *Oregon State University*
Time: Monday, August 7, 2017, 16:40 - 18:20
Location: Eaton Hall 206

Towards a Robust Data Link for Intraoral Tongue Drive System using Triple Bands and Adaptive Matching 491
Fanpeng Kong (Georgia Institute of Technology), S. Abdollah Mirbozorgi (Georgia Institute of Technology), Byunghun Lee (Georgia Institute of Technology), Maysam Ghovanloo (Georgia Institute of Technology)

This paper presents the steps we have taken towards implementing a reliable and robust data link that is necessary for an intraoral Tongue Drive System (iTDS), which is a wireless and wearable assistive technology. The iTDS detects the user's intention from a set of user-defined commands (defined based on tongue gestures) to control wheelchair, phone, PC, etc. To deal with potential sources of RF interference, three operating bands, at 27 MHz, 433 MHz, and 915 MHz have been integrated. Additionally, an adaptive matching network is incorporated in the transmitter to deal with the dynamic oral environment.

Smart Bandages for Chronic Wound Monitoring and On-Demand Drug Delivery 495
Meera Punjiya (Tufts University), Pooria Mostafalu (Tufts University), Sameer Sonkusale (Tufts University)

We review two generations of smart bandages and sensors developed in our group. These devices are capable of monitoring and treating chronic wounds through O2, pH and strain measurement and on-demand drug delivery. First we seek to close the gap between patient and caregivers through continuous monitoring of wound healing status with oxygenation measurements coupled with wireless data acquisition and transmission. Next we demonstrate on-demand drug delivery with this same platform using thermoresponsive particles. Currently, we focus efforts on 2D mapping of wound pH. Here, pH sensors are fabricated on thread using simple, cleanroom free processes and are embedded into bandages. We demonstrate these sensors for pH measurement with wireless data transmission and integration with a custom CMOS potentiostat.

A CMOS Integrated fdNIRS and tDCS System for Simultaneous Brain Stimulation and Monitoring 499
Yun Miao (Tufts University), Valencia Joyner Koomson (Tufts University)

A CMOS integrated frequency domain near infrared spectroscopy (fdNIRS) and transcranial direct current stimulation (tDCS) is designed for simultaneous brain stimulation and monitoring. The combination of optical sensing and electrical stimulation solves the incompatibility between EEG and tDCS in both time and spatial domains. The dual-channel fdNIRS achieved a sub nW sensitivity when working with an APD with 40A/W responsivity and 1.77mm2 active area. The on-chip 5-bit current stimulator can support a stimulating current between 0.6mA and 2.2mA with 1% accuracy, which meets the requirements of tDCS. The chip is fabricated in a standard 130nm CMOS process and occupies an area of 2.25mm2

A Microwatt Front End and Asynchronous ADC for Sparse Biopotential Acquisition 503
Jaime Jimenez (Brown University), Shanshan Dai (Brown University), Jacob K. Rosenstein (Brown University)

We present the design and implementation of a monolithic microwatt analog front end and asynchronous level-crossing ADC for efficient capture of sparse biopotentials. The low-noise differential AC-coupled front-end provides +40dB gain, and the signal is digitized by an asynchronous level-crossing ADC which encodes the signal slope into a stream of pulses. For temporally-sparse signals such as single-unit extracellular neural spike recordings, this pulse encoding system provides both power savings and intrinsic data compression as compared to traditional Nyquist sampling. The circuit occupies 0.0088 mm2 in 0.18 µm CMOS and consumes 750nA from a 1.8V supply.

Signal-to-Noise Ratio Enhancement using Graphene-Based Passive Microelectrode Arrays 507
Sepideh Rastegar (Boise State University), Justin Stadlbauer (Boise State University), Kiyo Fujimoto (Boise State University), Kari McLaughlin (Boise State University), David Estrada (Boise State University), Kurtis D. Cantley (Boise State University)

This work is aimed toward the goal of investigating the influence of different materials on the signal-to-noise ratio of passive neural microelectrode arrays. The microelectrode arrays are fabricated using gold, indium tin oxide, and chemical vapor deposited graphene. Signal is applied to microelectrode arrays, and response is measured on an oscilloscope from a microprobe. The time domain response signal is transformed into a frequency spectrum, and Signal to Noise Ratio is calculated from the ratio of power spectral density of the signal to the power spectral density of baseline noise at the frequency of the applied signal. We observed as the magnitude or the frequency of the input voltage signal gets larger, graphene-based microelectrode arrays increase the signal-to-noise ratio significantly compared to microelectrode arrays made of indium tin oxide and gold.

Session A4L-F: Computer Aided Design

Chair: Juan Montiel-Nelson, *University of Las Palmas de Gran Canaria*
Co-Chair: Hector Solar, *CEIT*
Time: Monday, August 7, 2017, 16:40 - 18:20
Location: Paige Hall - Crane Room

Simulation of Switching Circuits using Transfer Functions 511
David Kebo Houngninou (Southern Methodist University), Mitchell A. Thornton (Southern Methodist University)

The concept of a transfer function model for digital circuits is devised wherein the input stimulus and the output response are represented by an element in a finite-dimensioned Hilbert vector space. This work describes the use of our past results to implement and evaluate a prototype simulation tool. The prototype parses a structural netlist in Verilog and constructs the transfer matrix for the netlist in the form of a BDD.

Obstacle-Aware Symmetrical Clock Tree Construction 515
Meng Liu (Chinese Academy of Sciences), Zhiwei Zhang (Chinese Academy of Sciences), Wenqin Sun (Chinese Academy of Sciences), Donglin Wang (Chinese Academy of Sciences)

Our obstacle-aware symmetrical clock tree algorithm is proposed to achieve better results in constraints of benchmark circuits. We also have considered multi-fanout matching, merging, embedding and buffer insertion situation. This clock tree structure makes it have the ability to resist OCV, while the logic level greatly reduced. By using this tree as a top-level clock design, designers can easily build the entire regular CDN structure like clock mesh or spines.

Formal Modeling and Verification for Pre-Charge Half Buffer Gates and Circuits 519
Ashiq A. Sakib (North Dakota State University), Scott C. Smith (North Dakota State University), Sudarshan K. Srinivasan (North Dakota State University)

A formal modeling and verification methodology for Pre-Charge Half Buffer (PCHB) gates and circuits is presented. PCHB gates have hysteresis and incorporate a handshaking protocol. Thus, we model gates as transition systems and provide correctness property templates that capture safety and liveness. The methodology is demonstrated using several circuits.

Transistor Placement Strategies for Non-Series-Parallel Cells 523
Maicon S. Cardoso (Universidade Federal de Pelotas), Gustavo H. Smaniotto (Universidade Federal de Pelotas), João J. da S. Machado (Universidade Federal de Pelotas), Matheus T. Moreira (Pontifícia Universidade Católica do Rio Grande do Sul), Leomar S. da Rosa Junior (Universidade Federal de Pelotas), Felipe de S. Marques (Universidade Federal de Pelotas)

Recent papers have demonstrated that non-series-parallel topologies can deliver arrangements with fewer transistors when compared to the widely used series-parallel approach. However, due to its topology particularities, this paradigm represents a challenge for the physical design, especially concerning the transistor placement. In this scenario, we present an analysis of two placement strategies: the first is based on a continuous active area approach, while the last is based on a continuous polysilicon gates paradigm. In order to evaluate both placement policies regarding geometrical and electrical aspects, we have performed experiments in a well-known benchmark. The continuous polysilicon gates strategy presented optimizations in the cell area, wirelength, input capacitance, leakage, internal and switching power, while the continuous active area strategy showed better results concerning propagation and transition delay. These results can be used as a guide to an adaptive placement methodology implemented in automatic layout design tools to deal with non-series-parallel arrangements.

Session A4L-G: Wireline Communication Circuits and Systems

Chair: Sleiman Bou-Sleiman, *Intel Corporation*
Co-Chair: Michael Green, *University of California-Irvine*
Time: Monday, August 7, 2017, 16:40 - 18:20
Location: Paige Hall - Terrace Room

A 25Gb/s Serial-Link Repeater with Receiver Equalization and Transmitter De-Emphasis in 0.13µm SiGe BiCMOS 527
Shuai Yuan (Tsinghua University), Liji Wu (Tsinghua University), Ziqiang Wang (Tsinghua University), Chun Zhang (Tsinghua University), Zhihua Wang (Tsinghua University), Hanjun Jiang (Tsinghua University)

A serial-link repeater chip with a single stage continuous-time linear equalizer (CTLE) and a 3-tap feed-forward equalizer (FFE) is realized in a 0.13µm SiGe BiCMOS technology. The CTLE with the negative capacitance circuits is implemented to achieve a larger high-frequency boosting at the receiver side. By utilizing the LC-based delay elements, the FFE accomplishes the transmitter de-emphasis without retiming clocks. The measurement results show that the repeater can at least compensate for a Nyquist channel loss of 23.5dB when operating at the data rate of 25Gb/s. The total power consumption is 230mW from a 3.3V power supply.

Data-Transition Adaptive Decision Feedback Equalizer for 2/4PAM Serial Links 531
Yue Li (Ryerson University), Fei Yuan (Ryerson University)

Conventional decision feedback equalizers (DFEs) suffer from the fundamental drawback of shrinking rather than increasing data eyes when consecutive 1s or 0s are present in data. To combat this drawback, a new data-transition adaptive DFE is proposed. The proposed DFE takes into account the dependence of post-cursors on the polarity of data and searches for optimal tap coefficients using a sign-sign least-mean-square (SS-LMS) with consideration of the state transition of data. To validate the effectiveness of the proposed algorithm, both data-state DFE and data-transition DFE are employed to equalize impaired channels with known characteristics. Simulation results demonstrate that the proposed data-transition DFE outperforms data-state DFE equalization with improved vertical eye-opening, reduced jitter, and shorten adaptation.

An Adaptive Edge Decision Feedback Equalizer with 4PAM Signalling 535
Matthew Dolan (Ryerson University), Fei Yuan (Ryerson University)

This paper presents an adaptive edge decision feedback equalizer (DFE) with 4PAM signaling. Optimal DFE tap coefficients and threshold voltages for data recovery are obtained adaptively using sign-sign least-mean-square (SS-LMS) algorithms that minimize data jitter. Clock and data recovery is carried out using a dual phase/frequency-locked loop. A 10 Gbps 4PAM serial link has been designed in a 65 nm CMOS technology and analyzed using Spectre from Cadence Design Systems with BSIM4 models. Simulation results demonstrate that the proposed adaptive edge DFE is capable of opening completely closed data eyes at the far end of a backplane channel with -25 dB boud-rate attenuation with 46.5\% and 56\% horizontal and vertical eye-openings, respectively while consuming 66 mW power.

A 40-80 Gb/s PAM4 Wireline Transmitter in 65nm CMOS Technology 539
Fangxu Lv (Tsinghua University / Air Force Engineering University), Xuqiang Zheng (Tsinghua University), Shuai Yuan (Tsinghua University), Ziqiang Wang (Tsinghua University), Yajun He (Tsinghua University), Chun Zhang (Tsinghua University), Zhihua Wang (Tsinghua University), Jianye Wang (Air Force Engineering University)

This paper presents a 40-80 Gb/s quarter rate PAM4 wireline transmitter. The transmitter incorporates a 2-tap feed-forward equalizer (FFE) based on multiple-multiplex (MUX) and a parallel PRBS7 generator. The transmitter is achieved in 65nm CMOS technology and supplied with 1.2V. The simulation results show that the proposed transmitter can work at 40-80 Gb/s with 4-level pulse amplitude modulation (PAM4) and consumes 173mW at 80 Gb/s.

Tuesday, August 8, 2017

Session B1L-A: Analog Circuits and Systems III

Chair: Jeremy Holleman, *University of Tennessee*
Time: Tuesday, August 8, 2017, 10:20 - 12:00
Location: Braker Hall 001

Resource Sharing in Feed Forward Neural Networks for Energy Efficiency 543
Abdullah M. Zyarah (Rochester Institute of Technology), Dhireesha Kudithipudi (Rochester Institute of Technology)

Exploiting resource reusability and low precision in neural networks is a promising approach to achieve energy efficient computational platforms. This research presents two generalizable approaches to reuse resources in feed-forward neural networks and demonstrated on extreme learning machines. In the first approach, coalescing, a single stack of neuronal units perform both feature extraction and classification tasks through shared resources. In the second approach, folding, the neurons in a high-dimension feedforward layer are folded to execute multiple-tasks. The folding technique can also be combined with low precision modules. The proposed design techniques are validated for a classification task on binary (Australian credit and Diabetes corpus) and multi-class dataset. The total power consumption is measured to be 3.65 mW on TSMC 65nm technology node, while yielding an accuracy of 91.7\% for MNIST.

A Mixed-Signal Approach to Memristive Neuromorphic System Design 547
Gangotree Chakma (University of Tennessee), Sagarvarma Sayyaparaju (University of Tennessee), Ryan Weiss (University of Tennessee), Garrett S. Rose (University of Tennessee)

In this paper we present a memristive neuromorphic system for higher power and area efficiency. The system is based on a mixed signal approach considering the digital nature of the peripheral and control logics and the integration being analog. So, the system is connected digitally outside but the core is purely analog. This mixed signal approach provides the advantage of implementing neural networks with spiking events in a synchronous way. Moreover, the use of nano-scale memristive device saves the area and power of the system and some considerations about the the device have also been proposed in the paper to make the system more energy efficient.

A Fast Convergent and Energy Efficient Offset Calibration Technique for Dynamic Comparators 551
Mohsen Judy (University of Tennessee), Jeremy Holleman (University of Tennessee)

A novel offset calibration technique with fast convergence rate for high-speed dynamic comparators is presented. The circuit utilizes a multi-rate charge pump circuitry to speed up the calibration process while maintaining the precision which leads to better energy efficiency. The circuit is designed in a 0.13µm CMOS process. Based on Monte-Carlo simulation results the comparator achieves 183.1µV residual offset within an average convergence time of 82 ns. Based on measurement results the comparator dissipates 5.1µW from a 1 V power supply at 250 MHz clock frequency, achieving a FOM of 10.2 fJ/conv.

Fractional-Order Oscillator Design using Unity-Gain Voltage Buffers and OTAs 555
Aslihan Kartci (Brno University of Technology), Norbert Herencsar (Brno University of Technology), Jaroslav Koton (Brno University of Technology), Lubomir Brancik (Brno University of Technology), Kamil Vrba (Brno University of Technology), Georgia Tsirimokou (University of Patras), Costas Psychalinos (University of Patras)

In this study, a new voltage-mode fractional-order oscillator using two unity-gain voltage buffers, two operational transconductance amplifiers, one resistor, and two capacitors is presented. The design procedure of integer-order as well as fractional-order oscillator employing in total 20 MOS transistors is discussed. Effects of fractional-order capacitors on amplitude, phase, condition of oscillation, and frequency of oscillation are shown. Various case examples are given while SPICE simulations using TSMC 0.35 µm level-3 CMOS process parameters with ±1.65 V supply voltages verify their operation and compare with theoretical ones.

Session B1L-B: Security Tool Chain

Chair: Qiaoyan Yu, *University of New Hampshire*
Time: Tuesday, August 8, 2017, 10:20 - 12:00
Location: Eaton Hall 201

ATAVE: A Framework for Automatic Timing Attack Vulnerability Evaluation 559
Jungmin Park (University of Florida), Massimiliano Corba (Charles Stark Draper Laboratory), Antonio E. de la Serna (Charles Stark Draper Laboratory), Richard L. Vigeant (Charles Stark Draper Laboratory), Mark Tehranipoor (University of Florida), Swarup Bhunia (University of Florida)

Timing leakage can be exploited to break a cryptographic system. Even though timing attacks have been well-researched for the past decade, recent system implementations remain highly vulnerable to these attacks. There is a critical need to develop a framework for automatic evaluation of vulnerability of a design against these attacks, so that integrated circuit designers can understand the vulnerability and take appropriate actions to counter them. In this paper, we proposed a novel CAD tool framework for automatic timing attack vulnerability evaluation, referred to as ATAVE, with associated algorithms and metrics. RSA implementation using Montgomery multiplication with square-and-multiply algorithm is efficiently analyzed using ATAVE.

High Level Synthesis using Vivado HLS for Optimizations of SHA-3 563
H.S. Jacinto (Boise State University), Luka Daoud (Boise State University), Nader Rafla (Boise State University)

The SHA-3 hashing algorithm is the most recently developed hash function, and the most secure. Implementation of the SHA-3 in hardware description language is time demanding and tedious to debug. On the other hand, High-Level Synthesis (HLS) tools offer potential solutions to the hardware design. In this paper, we explore the SHA-3 and its implementation onto FPGA. SHA-3 was initially coded in C language and then synthesized with HLS. The HLS tool enabled us to quickly analyze our design to make suitable optimizations which led to increased throughput of the SHA-3 up to 2000 Mbps. After pipelining the synthesized hardware design, it was capable of hashing a block of 1088 bits in 70 clock cycles

Golden Reference Matching for Gate-Level Netlist Functionality Identification 567
Thao Le (University of Arkansas), Jia Di (University of Arkansas)

Outsourcing designs to 3rd party vendors is a common practice in integrated circuit (IC) manufacture industry. While bringing advantages like reduced cost and shortened time-to-market of a new system, this practice as the same time raises security threats in the IPs from 3rd party vendors. These IPs may contain hardware Trojans capable of compromising the product's confidentiality, integrity, and/or availability. Different from prior work focusing on RTL designs, this paper introduces a framework of golden reference matching for gate-level netlists. Promising results have been achieved on several benchmark circuits in functionality matching and Trojan detection.

Combinational Hardware Trojan Detection using Logic Implications 571
Noah Cornell (University of St. Thomas), Kundan Nepal (University of St. Thomas)

This paper provides a proof-of-concept demonstration of the potential benefit of using logical implications for detection of combinational hardware trojans. Using logic simulation, valid logic implications are selected and added to to the checker circuitry to detect payload delivery by a combinational hardware trojan. Using combinational circuits from the ISCAS benchmark suite, and a modest hardware budget for the checker, simulation results show that the probability of a trojan escaping detection using our approach was only 16%.

A Solitary Protection Measure against Scan Chain, Fault Injection, and Power Analysis Attacks on AES 575
Tonmoy Dhar (University of Illinois at Chicago), Swarup Bhunia (University of Florida), Amit Ranjan Trivedi (University of Illinois at Chicago)

Hardware implementation of cryptographic algorithms are prone to security vulnerabilities. Scan-chain-based attack (SBA), fault-injection attack (FIA), and power analysis attack (PAA) are three popular cryptanalysis techniques in exploiting vulnerabilities of crypto-chips. Employing multiple strategies for counteracting the attacks results in significant resource overheads. In this paper, we present a novel and solitary approach to prevent either type of attacks on the hardware implementation of Advanced Encryption Standard (AES). With a two-third increase in resource overhead and negligible increase in timing overhead compared to the regular AES datapath, the proposed technique makes the system resilient against SBA, FIA and PAA.

Session B1L-C: Nyquist-Rate Data Converters

Chair: Subhanshu Gupta, *Washington State University*
Time: Tuesday, August 8, 2017, 10:20 - 12:00
Location: Eaton Hall 202

High Speed ADCs for Wireline Applications 579
Mohammad Sadegh Jalali (Rambus), Masum Hossain (Rambus), Kenneth Dyer (Rambus), Saman Sadr (Rambus)

This paper presents an overview of high speed ADCs for wireline applications. In the first part of the paper, the need for an ADC-based wireline link is justified, which is then followed by a discussion on the architecture of an ADC-based transceiver. We conclude this paper by discussing the challenges and trade-offs of designing high speed ADCs for wireline applications.

A 10-Bit 400 MS/s Asynchronous SAR ADC using Dual-DAC Architecture for Speed Enhancement 583
Qingjun Fan (University of Houston), Jinghong Chen (University of Houston)

This paper presents a high-speed and power-efficient successive-approximation-register (SAR) analog-to-digital converter (ADC). A dual-DAC architecture is proposed to enhance the conversion rate by decreasing the worst-case logic delay and thus the time needed for each conversion cycle. A 1-bit redundancy is introduced to absorb the decision errors caused by the mismatch between the two DACs and to relax the DAC settling requirement. In addition, an addition-only digital error correction technique is utilized to convert the non-binary codes into binary ones. A 10-bit SAR ADC is designed in a 28-nm FDSOI CMOS technology. The ADC achieves a signal-to-noise-plus-distortion ratio (SNDR) of 59.69 dB at the Nyquist input frequency, while consuming 1.53 mW from a 1.0 V power supply at 400 MS/s. The resulting figure-of-merit (FOM) is 4.86 fJ/conv.-step.

Blind SAR ADC Capacitor Mismatch Calibration 587
Armia Salib (University College Dublin), Mark F. Flanagan (University College Dublin), Barry Cardiff (University College Dublin)

This paper presents an all-digital background blind calibration technique for the capacitor mismatch problem in SAR ADCs. It utilizes the redundancy offered using a sub-radix-2 DAC architecture to blindly estimate the mismatch and the assigned weight for each comparator decision. The weights are estimated by building partial histogram windows for the comparator decision vectors. To remove the dependency on the input signal's probability density function, the histogram windows are normalized with respect to their peaks. Matlab simulation results show that an ENOB within 0.12bit of the optimal is attained using the proposed algorithm.

An 8b 1.39GS/s 0.85V Two-Step ADC with Background Comparator Offset Calibration 591
Sudipta Sarkar (University of Texas at Dallas), Benwei Xu (University of Texas at Dallas), Brian Elies (University of Texas at Dallas), Yun Chiu (University of Texas at Dallas)

An 8b, 1.3/1.39GS/s, 7/8.1mW two-step ADC is presented that introduces a single reference comparator based background comparator offset calibration technique. This work employs a dual-residue based inter-stage redundancy scheme to relax residue amplifier specifications (and enable high-speed operation at 0.85V supply) in a two-step ADC. Comparator offset calibration is implemented through body biasing with an area efficient 8b offset calibration DAC. A prototype in 28nm CMOS achieves 6.8 ENOB and 50fJ/c-s at DC and 6.3 ENOB and 68fJ/c-s at Nyquist, at a sample rate of 1.3GS/s. The measured SNDR/SFDR improve from 29.2/40.7dB to 42.6/57.7dB after calibration. The active area is 0.05mm2

Systematic and Random Mismatch Characterization in Device Arrays 595
Nanqi Liu (Iowa State University), Chris Lash (Texas Instruments Inc.), Jim Todsen (Texas Instruments Inc.), Degang Chen (Iowa State University)

A general methodology of device array mismatch characterization is introduced, analyzed and verified. Instead of measuring each device's parameter individually, the device array is configured as a data converter and the mismatch information is extracted from the differential linearity (DNL) of the converter. Systematic and random mismatch are characterized separately using the proposed decomposition method with robustness to additive random noise. An 8-bit high precision resistor array is fabricated in Globalfoundries 0.13µm TaN thin film resistor process. Measurement results show that systematic mismatch contributes to a large portion of the total mismatch when the matching requirement comes down to 0.01% level.

Session B1L-D: Signal Processing II

Chair: Ruolin Zhou, *WNEU*
Time: Tuesday, August 8, 2017, 10:20 - 12:00
Location: Eaton Hall 203

Four Layers Image Representation for Prediction of Lung Cancer Genetic Mutations based on 2DPCA 599
Moataz M. Abdelwahab (Egypt-Japan University of Science and Technology),
Shimaa A. Abdelrahman (Egypt-Japan University of Science and Technology)

Genetic mutations are the first warning to the onset of lung cancer. The ability to early predict these mutations could open the door for a targeted treatment options for lung cancer patients. Three top candidate genes previously reported to have the highest frequency of lung cancer mutations. Each gene is encoded as a symbolic sequence of four letters. A novel method for gene representation is introduced in this paper, where each letter in gene sequence is represented by a layer image. The final four layers are integrated with Two Dimensional Principle Component Analysis (2DPCA) to build an algorithm for prediction of lung cancer. Furthermore, the algorithm is capable to identify the substitution type in somatic mutations of lung cancer with high accuracy. The high dimensionality and computational complexity of prediction are reduced by employing 2DPCA, which allows a high-dimensional space to be represented in a low-dimensional one. Experimental results confirm that, the proposed algorithm achieved accuracy of 98.55% in early prediction of lung cancer and accuracy of 88.18% in identification of the substitution type in gene sequence.

State Space Design Cycle and Hardware in the Loop Testing and Verification 603
Kourosh Rahnamai (Western New England University), Justin Rowlands (Western New England University)

Advances in real-time hardware in the loop (HIL) boards and software has provided an excellent opportunity to implement and test control algorithms rapidly on real systems [1-7]. Hardware in the loop development allows for rapid development, testing and verification of control systems. This paper, using a servo system as an example, clearly explores modern control systems design cycle, which includes real-time verification of the controller. This methodology illustrates design cycle from system specification, system constraints to controller design, HIL testing and verification of the developed controller. This rapid prototyping strategy to develop and test controllers can be used in industry as well as academia. In an academic environment, it helps student relate, better understand and implement theoretical concepts on real systems. Experiments described in this paper use a real-time hardware in the loop platform, which consists of a DC-servo control system, MATLAB, Simulink, dSPACE real-time hardware and ControlDesk software. This paper shows how this type of platform can is be used to verify system models and test designed state space controllers.

A Robust Auditory System for Ego-Noise Suppression based on Active Acoustic Metamaterials in Small-Size Robots 607
Xihan Gu (Fudan University), Yun Chen (Fudan University), Xiaofeng Wu (Fudan University),
Yuan Wang (University of California-Berkeley)

We propose a auditory system based on microphone array composed of three parts: noise suppression, sound source localization (SSL) and beamforming. In this case, our research mainly focuses on the issues of reliability and real-time on auditory system algorithms. A 2-stage SSL algorithm is adopted in our system to reduce the complexity. Furthermore, the matrix inversion can be processed in parallel with signal sampling, which means very low latency between the output and the input. With this auditory system, then we can refine and reconfigure the active acoustic metamaterials (AAMMs) to suppress the ego-noise.

A Hidden Markov Model-Based Blind Detector for Multiplicative Watermarking 611
Marzieh Amini (Concordia University), Hamidreza Sadreazami (Concordia University),
M. Omair Ahmad (Concordia University), M.N.S. Swamy (Concordia University)

Nowadays, transmission of data via Internet has made illegal data distribution a major problem in digital world. Watermarking is known as a possible solution to protect digital data. In this work, we propose a blind detector for multiplicative watermarking of images in the wavelet domain. To this end, the vector-based hidden Markov model (HMM) is employed as a prior model for the wavelet coefficients of the host image. This model is known to provide an accurate fit to the distribution of the wavelet coefficients by capturing both their heavy-tailed marginal statistics and their inter-subbands and cross-orientations dependencies. Analytical expressions for the proposed watermark detector such as the mean and variance of the log-likelihood ratio test are derived and used to evaluate its performance. The performance of the proposed detector is shown to outperform that of the other detectors by providing higher detection rate and better imperceptibility of the embedded watermark. It is also shown that the proposed vector-based HMM detector under various attacks such as compression, rotation, filtering and noise, is more robust than other existing detectors.

Matrix Quadrature Filterbanks for Image Processing 615
Jian-ao Lian (Prairie View A&M University), Yonghui Wang (Prairie View A&M University)

An innovative approach is presented to establish bidimensional linear-phase matrix quadrature filterbanks (MQF) directly from their matrix identities. It is well-known that two-channel quadrature filterbanks (QMF) have been successfully applied to signal and image processing. Bidimensional QMF filterbanks directly deduced from tensor-products of 1D QMF filterbanks is easy, straightforward, and convenient. They possess both the finite impulse response and the perfect reconstruction properties. However, some additional desirable features are missing. Direct consideration from matrices yields more freedoms for the design of the new ingenuous MQF. A new MQF is designed and is applied to image compression, and the rate-distortion performance shows that the proposed matrix wavelet has promising potential applications in image processing.

Session B1L-E: Biochips and Bioengineering

Chair: Jacob Rosenstein, *Brown University*
Co-Chair: Ebrahim Ghafar-Zadeh, *York University*
Time: Tuesday, August 8, 2017, 10:20 - 12:00
Location: Eaton Hall 206

Flexible Glucose Sensors and Fuel Cells for Bioelectronic Implants 619
T. Thorsen (Massachusetts Institute of Technology), I. Weaver (Massachusetts Institute of Technology), E. Holihan (Massachusetts Institute of Technology), R. Cabrera (Massachusetts Institute of Technology), R. Sarpeshkar (Dartmouth College)

Microfabrication techniques were developed to create flexible 24 µm thick glucose sensors on polyimide substrates. Measurements of the sensor performance, recorded as voltage potential, were carried out for a range of glucose concentrations (0 – 8 mM) in physiological saline (0.1 mM NaCl, p7.4). The sensors show rapid response times (seconds to stable potential) and good sensitivity over physiological ranges. Additionally, we demonstrate that the sensors can operate as fuel cells, generating peak power levels up to 0.94 uW/cm2. Such flexible devices, which can be rolled up to increase surface area within a fixed volume, may enable ultra-low-power bio-electronic implants for glucose sensing or glucose energy harvesting in the future.

Analysis of Multi-Channel Microfluidics for Serial Dilution in Lab-on-CMOS Platforms 623
Andrew J. Mason (Michigan State University), Hao Wan (Michigan State University)

Lab-on-CMOS platforms provide a means to integrate microfluidics with biochips composed of various bio-probes immobilized on the surface of CMOS instrumentation chips. This paper outlines recent developments in lab-on-CMOS technologies and presents an analysis of the challenges to achieving accurate serial dilution of test samples over sensing elements in lab-on-CMOS platforms. Based on this analysis, sensing chambers, channel placements, mixers, and microchannel geometries were optimized to achieve rapid fluid exchange and well-controlled dilution ratios. Utilizing an analogous electric circuit model, the design of a four-channel microfluidic device is presented along with simulation results validating the capability of the device to achieve accurate serial dilution in four different sensing chambers. The resulting device enables simultaneous measurement of samples with different concentrations for rapid sensor or sample calibration in lab-on-CMOS applications.

Characterization of an Active Micro-Electrode Array with Spike Detection and Asynchronous Readout 627
Bathiya Senevirathna (University of Maryland-College Park), Alexander Castro (University of Maryland-College Park), Timir Datta-Chaudhuri (University of Maryland-College Park), Elisabeth Smela (University of Maryland-College Park), Pamela Abshire (University of Maryland-College Park)

We present performance characterization of a bio-potential recording system with an asynchronous readout architecture. The signal processing chain consists of a low-noise bio-potential amplifier, spike detection circuitry, and an address event representation (AER) communication protocol. Each stage of the recording system was tested individually, and the systems' detection specificity and sensitivity were evaluated. For input spike amplitudes of 560 µV, a detection rate of 81 % was obtained with a false positive rate of 7 %.

Wireless Coil Array Sensors for Monitoring Hermetic Failure of Millimeter-Sized Biomedical Implants 631
Pyungwoo Yeon (Georgia Institute of Technology), Agrata Kumar (Georgia Institute of Technology), Maysam Ghovanloo (Georgia Institute of Technology)

This paper presents an automated hermetic failure monitoring system design for multiple millimeter-sized biomedical implants using an inductive link array. 1 × 1 mm^2 sized passive implants, wrapped with power receiving and data transmitting inductor-capacitor (LC) tank, and coated with parylene-C and polydimethylsiloxane (PDMS) were utilized for packaging failure monitoring, which can result in phase-dip disappearance or phase-dip frequency shift. The presented system can wirelessly monitor the phase-dip in the frequency and time domains through the readout coil array, as they are coupled with the LC sensors embedded in the implants. The amplitude of the phase-dip signal at ~1.5 mm sensing distance is 0.25 degrees and the standard deviation from the phase-dip center frequency is 135 kHz, which represents only 0.345% variation around the 116.3 MHz resonance frequency of the LC sensor.

A New Cell-on-Chip Impedometric Interface: Design, Implementation and Experimental Results 635
Giancarlo Ayala (York University), Ebrahim Ghafar-Zadeh (York University), Georg Zoidl (York University), Sebastian Magierowski (York University)

This paper presents a new approach towards the design and implementation of high-throughput impedimetric screening for life science applications. Herein, we propose a new cell-on-chip model for cellular analysis. A low complexity platform was developed to demonstrate the advantages of this model for cellular analysis. This low cost platform consists of an array of optically transparent electrodes incorporated with polymeric miniaturized chambers. Herein, we demonstrate and discuss the experimental results to prove the functionality and applicability of the proposed model. Based on these preliminary results, a reconfigurable high-throughput impedimetric platform can be developed for chemical and biological analysis.

Session B1L-F: Reconfigurable Circuits and FPGA Applications

Chair: Manuel Jimenez, *University of Puerto Rico Mayaguez*
Co-Chair: Jabulani Nyathi, *EWU Engineering and Design*
Time: Tuesday, August 8, 2017, 10:20 - 12:00
Location: Paige Hall - Crane Room

A Memory Optimized Mersenne-Twister Random Number Generator 639
Naman Saraf (University of Minnesota), Kia Bazargan (University of Minnesota)

Random number generators (RNGs) are an integral component of numerous stochastic simulation methods, with applications in diverse scientific disciplines. Recently, stochastic simulation methods are being increasingly implemented on FPGAs for improved performance. Consequently, efficient RNG implementations are essential to successfully realize stochastic simulation methods on FPGAs. We present a memory optimized architecture of the prominent Mersenne-Twister RNG (MT-RNG) for efficient implementation on FPGAs. Our approach leverages the different memory constructs available on an FPGA device to reduce the memory requirements of our architecture by upto 50% over existing designs in published literature. Furthermore, we perform an out-of-order computation of random numbers to reduce the hardware area of our MT-RNG implementation, and compare the hardware metrics of our proposed architecture with the existing implementations on different FPGA platforms.

An FPGA-Based Algorithm Development Framework for Estimating the Accuracy of Embedded DSP Signal Transforms 643
Sylmarie Dávila-Montero (Universidad de Puerto Rico), Keisha Castillo-Torres (Universidad de Puerto Rico), Violeta Reyes-Rodríguez (Universidad de Puerto Rico), Manuel Jiménez (Universidad de Puerto Rico), Domingo Rodríguez (Universidad de Puerto Rico)

This work addresses the problem of estimating the accuracy of a certain class of digital signal processing algorithms, known as linear signal transforms, when implemented on field programmable gate array (FPGA) hardware computational structure (HCS) units. A solution is provided through the formulation of a hardware development framework which uses complex multipliers and complex addition units as its basic functional primitives to arrive at an estimation formulation of embedded signal processing operations.

Statistical Accuracy Analysis of Complex Floating Point Multipliers 647
Violeta Reyes-Rodríguez (Recinto Universitario de Mayagüez), Manuel Jiménez (Recinto Universitario de Mayagüez), Keisha Castillo-Torres (Recinto Universitario de Mayagüez), Sylmarie Dávila-Montero (Recinto Universitario de Mayagüez), Domingo Rodríguez (Recinto Universitario de Mayagüez)

Scalar addition and multiplication generally obey commutative and distributive laws. However, in their hardware implementation, error propagation and accumulation do not necessarily follow the same rules. In this paper we present a statistical analysis of the accuracy in complex multiplication approaches for IEEE 754 single precision operands. Several approaches were evaluated using a dual approach that included an error analysis of the multiplication operator architectures and a statistical analysis of VHDL operator designs, implemented on a Xilinx Virtex 7 FPGA. Multiple experiments were carried for systematically assessing architectural, synthesis, and hardware performance characteristics of the target designs, comparing weaknesses and strengths of each architecture.

Hardware Implementation of the Baillie-PSW Primality Test 651
Carla Purdy (University of Cincinnati), Yasaswy Kasarabada (University of Cincinnati), George Purdy (University of Cincinnati)

Today's commonly used cryptographic algorithms, such as RSA, require large primes. Prime number generation in hardware improves confidence and security. Here we generate primes using the Baillie-PSW primality test; no known Baillie-PSW pseudoprime exists. Our main contribution is the implementation in Verilog of the Baillie-PSW test on an Altera Cyclone IV GX FPGA. This is the first hardware implementation of this test. Input is an odd random number; the next immediate probable prime (of length 1024 bits, the current standard) is returned. We analyze performance and resource usage of our implementation, which is a step towards a custom ASIC implementation.

Precision Medicine and FPGA Technology: Challenges and Opportunities 655
Brian Hill (Omics Data Automation Inc / University of California, Los Angeles), Jaclyn Smith (Omics Data Automation Inc), Gans Srinivasa (Omics Data Automation Inc), Kemal Sonmez (Omics Data Automation Inc / Oregon Health Sciences University), Ashish Sirasao (Xilinx, Inc), Amit Gupta (Xilinx, Inc), Madhubanti Mukherjee (Xilinx, Inc)

As genomic medicine becomes part of standard clinical care, Precision Medicine faces a daunting computational challenge in scaling up to support the genomic and image processing and analytics workloads required for millions of patients, especially in oncology clinics. Computational solutions based on heterogeneous hardware solutions such as FPGAs have the potential to enable the rollout of personalized care for large numbers of patients. We review several clinical use cases to shed light on how FPGA based solutions can lead to large performance gains and tackle the computational bottlenecks of precision medicine. The biggest barrier to FPGA adoption is their accessibility and the steep learning curve that it represents for many bioinformatics and precision medicine codebase development groups. We describe new standard libraries and development environments that will facilitate FPGA-based development and show how they enable performance improvements with modest effort investment.

Session B1L-G: Communication Hardware and Coding

Chair: Michael Green, *University of California-Irvine*
Co-Chair: Sleiman Bou-Sleiman, *Intel Corporation*
Time: Tuesday, August 8, 2017, 10:20 - 12:00
Location: Paige Hall - Terrace Room

Fast Convergence and Low Complexity Stochastic Turbo Decoder 659
Zhenbing Zhang (University of Electronic Science and Technology of China), Jianhao Hu (University of Electronic Science and Technology of China), Jienan Chen (University of Electronic Science and Technology of China), Kaining Han (University of Electronic Science and Technology of China)

Stochastic turbo decoder is a new scheme for turbo codes. But the long decoding latency and high complexity are two main challenges for fully parallel stochastic turbo decoders. In this paper, we proposed a novel stochastic turbo decoder scheme with two high accuracy stochastic operator modules, including no-scaling stochastic addition and stochastic normalization operator, which can improve the decoding convergence speed and decrease the computation complexity, simultaneously.

A Robust 2×2 CMOS Receiver Array for Meter-Scale Point-to-Point OOK VLC Links 663
Bassem Fahs (Rensselaer Polytechnic Institute), Asif J. Chowdhury (Rensselaer Polytechnic Institute), Javad Ghasemi (University of New Mexico), Payman Zarkesh-Ha (University of New Mexico), Mona M. Hella (Rensselaer Polytechnic Institute)

This paper presents a fully integrated 2×2 optical receiver array for Point-to-Point (P2P) On-Off-Keying (OOK) visible-light communication (VLC) links. The 2×2 PD-array design constraints and cross-talk issues are discussed. Each receiver exhibits a low input referred noise density of 5 pA/√Hz to meet the sensitivity requirements of free-space optical wireless links in the visible spectrum. The VLC receiver is tested as a part of an optical setup at 2.7 m and 6.7 m distances from a 680-nm laser-diode source. A measured 2.3 Gb/s per-channel data-rate with a VLC-compliant bit-error-rate is achieved through the use of high bandwidth circuit design techniques and a programmable integrated equalizer function. The receiver is implemented in AMS 0.35 µm technology. Each single receiver draws 65 mA from a 3.3 V DC voltage supply. The complete array size is 2.0 mm × 1.6 mm.

An Efficient and Scalable Hardware Architecture for Singular Value Decomposition towards Massive MIMO Communications 667
Mingda Zhou (Worcester Polytechnic Institute), Youjian Liu (University of Colorado at Boulder), Tian Xia (University of Vermont), Xinming Huang (Worcester Polytechnic Institute)

Massive multiple input multiple output (MIMO) technology plays an important role in next generation wireless communication systems. Modified Brent-Luk-Van Loan array and some other parallel hardware implementations are developed for channel matrix factorization. With massive MIMO, however, these implementations consume far more hardware resources than expected. In this paper, we propose a hardware-efficient architecture that performs singular value decomposition for complex matrices of arbitrary order and consumes very small amount of hardware resources. Though the usage of hardware resources decreases, the proposed architecture still provides competitive factorization speed.

Self-Powered System-on-Chip for Substrate Computing and Ultrasonic Communications 671
Yarub Alazzawi (Washington University in St. Louis), Shantanu Chakrabartty (Washington University in St. Louis)

Substrate computing refers to a paradigm where sensing, computing, communications, energy scavenging and energy storage functions are seamlessly integrated within a substrate. The substrate could be a part of an aircraft wing or a chassis of the car and the computing, communications and energy scavenging functions could be implemented using self-powered devices embedded inside the substrate. In this paper we present the design of a CMOS transceiver that could be used for through-substrate communications using ultrasonic pulses. The transceiver comprises of three piezoelectric interfaces, one of which is used for harvesting and regulating energy from mechanical vibrations in the substrate and the other two interfaces are used for transmitting and receiving ultrasonic pulses. We present measurement results using prototypes of the transceiver fabricated in a 0.5-µm CMOS process integrated with piezoelectric transducers that are attached to a segment of an aluminum wing. The results demonstrate the energy- harvesting, regulation functionalities along with the bi-directional telemetry functions needed to implement a complete transceiver for substrate computing.

Session B2P-H: Converter Circuit Techniques I

Chair: Vishal Saxena, *University of Idaho*
Time: Tuesday, August 8, 2017, 13:00 - 14:20
Location: Ballou Hall - Coolidge Room

A High Resolution Time-to-Digital Converter (TDC) based on Self-Calibrated Digital-to-Time Converter (DTC) 675
Tingbing Ouyang (Peking University), Bo Wang (Peking University), Lizhao Gao (Peking University), Jiangtao Gu (Peking University), Chao Zhang (Peking University)

Based on the parallel DTCs as delay cells, a 4-bit TDC with adjustable 0.7ps~1.4ps resolution and 11ps~22ps dynamic range is proposed in this paper. In this design, an extremely high resolution DTC is presented, achieving 15.6fs delay per LSB. By utilizing 16 DTCs which are adjusted to have the same time interval among two neighboring DTCs, a highly linear TDC is realized. To avoid the manual tuning, a self-calibration method is proposed, which allows for the calibration after the tape-out. The method utilizes a ruler DTC (RDTC) as the input signal of TDC to calibrate it. After self-calibration, the resolution of TDC is equal to the RDTC's delay step, so the resolution becomes adjustable by altering the RDTC's delay step. Setting the resolution at 1ps, the integral nonlinearity (INL) is 0.07LSB, the power consumption is 1.37mW at 50MHz with a 1.2V operating voltage and it occupies a core area of 0.018 mm2 in 0.13um CMOS process.

Low-Power All-Digital ΔΣ TDC with Bi-Directional Gated Delay Line Time Integrator 679
Young Jun Park (Ryerson University), Fei Yuan (Ryerson University)

This paper presents a low-power time integrator and its applications in an all-digital first-order $\Delta\Sigma$ time-to-digital converter (TDC). The time integrator is realized using a bi-directional gated delay line (BD-GDL) with time variable to be integrated as the gating signal. The integration of the time variable is obtained via the accumulation of the charge of the load capacitor and the logic state of gated delay stages. Issues affecting the performance of the time integrator and TDC are examined. An all-digital first-order $\Delta\Sigma$ TDC utilizing the time integrator was designed in an IBM 130 nm 1.2 V CMOS technology. A sinusoid time input of 430 ps amplitude and 231 kHz frequency with oversampling ratio 54 was digitized by the modulator. The TDC provides first-order noise-shaping and a SNR of 39.98 dB over the signal band $36 \sim 231$ kHz consuming 46 μW.

Noise-Shaping Time-Interleaved ADC based on a Single Ring Oscillator and a Sampling Array 683
A. Quintero (Universidad Carlos III de Madrid), C. Perez (Universidad Carlos III de Madrid), E. Gutierrez (Universidad Carlos III de Madrid), L. Hernandez (Universidad Carlos III de Madrid), S. Paton (Universidad Carlos III de Madrid)

An alternative architecture to conventional VCO-based analog-to-digital converters (VCO-ADCs) is proposed in this paper. The new architecture allows to enhance the resolution of the converter without the need of extending noise shaping order. Instead, the oversampling ratio is increased by sampling the outputs of the VCO through an array of digital delay lines. The output of this array is decoded with a modified array of XOR gates that makes higher VCO oscillation frequency possible. This allows to process the output data as samples of a highly oversampled sequence. We analyze the sensitivity to time delay mismatch in the elements of the delay line. A robust behavior is observed due to the error averaging through the sampling array elements. The proposed architecture achieves more than 10 ENOB for analog bandwidths (ABW) higher than 100 MHz using feasible clock rates and scalable and mostly digital circuitry.

2nd-Order VCO-Based CT ΔΣ ADC Architecture 687
Vaishak Prathap (State University of New York at Buffalo), Sanjeev Tannirkulam Chandrasekaran (State University of New York at Buffalo), Arindam Sanyal (State University of New York at Buffalo)

This paper proposes a novel architecture for purely voltage controlled oscillator (VCO) based continuous-time (CT) second-order ΔΣ analog-to-digital converter (ADC) without using bulky, passive components. The proposed technique does not require any VCO nonlinearity calibration and is robust against excess loop delay and static and dynamic errors in the multi-element digital-to-analog converter (DAC). Behavioral simulations have been performed to validate the proposed architecture.

Session B2P-J: Emerging Circuit Technology and Systems

Chair: Aatmesh Shrivastava, *Northeastern University*
Time: Tuesday, August 8, 2017, 13:00 - 14:20
Location: Ballou Hall - Coolidge Room

Time-Domain Ramped Gate Sensing for Embedded Multi-Level Flash in Automotive Applications 691
Sebastian Kiesel (Technische Universität München), Thomas Kern (Infineon Technologies AG), Bernhard Wicht (Leibniz University Hannover)

In this paper a time-domain voltage sensing scheme for embedded multilevel-cell flash memory is proposed. It uses a dynamic voltage ramp at the array's wordlines to linearize its timing transfer characteristic and hence to increase the robustness against cell threshold shifts. In contrast to existing stepped gate sensing schemes, the presented approach retains parallel sensing capability, which makes it good candidate for a low latency memory application. A common gate sense amplifier design in 28 nm CMOS with improved biasing scheme is introduced. Its more selective slope detection decreases its bias current and thereby enlarges the maximum sensing window by 30 %.

Memristor based 8-Bit Iterative Full Adder with Space-Time Notation and Sneak-Path Protection 695
Kamela C. Rahman (Portland State University), Md. Masoodur Rahman Khan (Ahsanullah University of Science and Technology), M.A. Perkowski (Portland State University)

Memristor technology is receiving an increased attention as a potential solution to meet the scaling demands in integrated circuit design. Memristor provides advantages like high-density, low-power, non-volatility and good scalability. In this paper, an 8-bit iterative full adder design is proposed that uses space-time based circuit notation. Stateful logic is performed with memristive nanowire crossbar. The proposed design provides good protection against sneak-path current. The 8-bit full adder design requires only 165 micro pulses to perform its operation.

Area Efficient Soft Error Tolerant RISC Pipeline: Leveraging Data Encoding and Inherent ALU Redundancy 699
Syed Rafay Hasan (Tennessee Technological University), Phani Tangellapalli (Tennessee Technological University)

This paper proposes novel soft error detection and mitigation technique in reduced instruction set computer (RISC) based pipeline processors. We leveraged the data encoding techniques (re-computing with rotated operands (RERO)) in conjunction with back pressure controlling mechanism in pipeline architecture. In order to alleviate the performance degradation due to potential stalling, we exploited the inherent ALU redundancy in conjunction with data encoding. Synthesis results on Stratix II FPGA from Altera suggested that if 5% of the instructions are subject to soft error then for 2.25 additional stall cycles (on average) our proposed solution provides better execution time even if the clock cycle time increases up to 11% because of additional hardware. Area wise our technique requires up to 3 times lesser area compared to other contemporary techniques and provides soft error tolerance in combinational blocks along with intermediate registers.

Error Free Sense Amplifier Circuit Design for STT-MRAM Nonvolatile Memory 703
Lohith Kumar Vemula (University of Missouri-Kansas City), Nahid M. Hossain (University of Missouri-Kansas City), Masud H. Chowdhury (University of Missouri-Kansas City)

The spin transfer torque magnetic random access (STT-MRAM) is suitable for embedded memories and also for the second level cache memory in the mobile CPU's. The most capable NVM component is STT-MRAM, which enhances the performance by 3.3 nS access time. It has strong radiation hardness, higher integrity and maximum endurance compared to SRAM. The power consumption of STT-MRAM is decreased by an order of magnitude by reducing the writing current. In this article, a new error free sense amplifier circuit is proposed. The detail analysis of the sense amplifier circuit is provided here. Finally, the performance of the proposed the sense amplifier is compared with existing sense amplifiers.

Local NOR and Global NAND Match-Line Architecture for High Performance CAM 707
Sung-gi Ahn (Sungkyunkwan University), Kee-won Kwon (Sungkyunkwan University)

Locally NOR and globally NAND match-line architecture and sensing circuits applicable to the high performance content addressable memory(CAM) is proposed. Local match-lines are segments of large capacitive match-line and designed as NOR-type maximizing search speed. Current and voltage control circuits are also implemented to reduce dynamic power consumption of local match-line. NAND global match-line reduces average power consumption by rarely switching its value. Search time is achieved 0.44ns which is enhanced 73.7% and average power consumption is also slightly reduced compared to the conventional.

A Hybrid Voltage-Mode Hysteretic Boost Converter with High Efficiency across a Wide Load Range 711
Punith R. Surkanti (New Mexico State University), Manikanta Ponnam (New Mexico State University), Sri Harsh Pakala (New Mexico State University), Paul M. Furth (New Mexico State University), Z.M. Saifullah (New Mexico State University)

A hybrid voltage-mode hysteretic boost converter is introduced in this work. The implemented control topology is inherently self stabilized due to the introduction of a current-limiting loop. A full range current sensor and a hysteretic comparator are used to realize the current-limiting loop. A zero current detector (ZCD) is also implemented to enable discontinuous conduction mode (DCM). The hybrid voltage-mode hysteretic boost converter is designed in a 0.5um CMOS process for an input voltage range of 3.2 - 4.2V. The converter can regulate to an output voltage of 5V while driving a load range of 20 - 200mA. A minimum efficiency of 93% is achieved across the operating load range with an input voltage of 3.6V.

Design of Adiabatic MTJ-CMOS Hybrid Circuits 715
Fazel Sharifi (New Mexico State University), Z.M. Saifullah (New Mexico State University), Abdel-Hameed Badawy (New Mexico State University)

Low-power designs are a necessity with the increasing demand of portable devices which are battery operated. In many of such devices the operational speed is not as important as battery life. Logic-in-memory structures using nano-devices and adiabatic designs are two methods to reduce the static and dynamic power consumption respectively. Magnetic tunnel junction (MTJ) is an emerging technology which has many advantages when used in logic-in-memory structures in conjunction with CMOS. In this paper, we introduce a novel adiabatic hybrid MTJ/CMOS structure which is used to design AND/NAND, XOR/XNOR and 1-bit full adder circuits. We simulate the designs using HSPICE with 32nm CMOS technology and compared it with a non-adiabatic hybrid MTJ/CMOS circuits. The proposed adiabatic MTJ/CMOS full adder design has more than 7 times lower power consumption compared to the previous MTJ/CMOS full adder.

Emerging STT-MRAM Circuit and Architecture Co-Design in 45nm Technology 719
Lohith Kumar Vemula (University of Missouri-Kansas City), Nahid M. Hossain (University of Missouri-Kansas City), Masud H. Chowdhury (University of Missouri-Kansas City)

The spin transfer torque magnetic random access (STT-MRAM) is suitable for embedded memories and also for the second level cache memory in the mobile CPU's. The most capable Nonvolatile memory (NVM) component is STT-MRAM. There is a demand to improve efficient circuit and architecture to compete with the existing NVM technologies. Low energy consumption is achieved to write and read into MTJ. This provides the Circuit and Architecture Co-design of STT-MRAM. Our contributions are: One bit STT-MRAM circuit design and SPICE simulation, Monte Carlo simulation of access transistor, 8x8 array/architecture of STT-MRAM is implemented by the single cell.

A 20Gbaud/s PAM-4 65nm CMOS Optical Receiver using 3D Solenoid based Bandwidth Enhancement 723
Stefano Facchin (Tyndall National Institute / University College Cork), Shiyu Zhou (Tyndall National Institute / University College Cork), Mark Power (Tyndall National Institute / University College Cork), Anil Jain (Tyndall National Institute / University College Cork), Carmelo Scarcella (Politecnico di Milano), Cleitus Antony (Tyndall National Institute / University College Cork), Paul Townsend (Tyndall National Institute / University College Cork), Peter Ossieur (Tyndall National Institute / University College Cork)

The following paper presents a linear optical receiver designed in CMOS 65nm technology and integrated with a Silicon Photonic chip for PAM-4 operation in short reach optical interconnects. The transimpedance amplifier in the receiver features a triple inductively peaked regulated cascode with bulk biasing for enhanced bandwidth and low group delay variation. Measurement results show clear eye diagrams at high baud rates such as 20 GBaud/s with a low power consumption.

Session B2P-K: Analog and Mixed-Signal Circuits III

Chair: Jacob Rosenstein, *Brown University*
Co-Chair: Benoit Gosselin, *Laval University*
Time: Tuesday, August 8, 2017, 13:00 - 14:20
Location: Ballou Hall - Coolidge Room

Coupled Oscillators with Shared Bias Current 727
Dakota Crisp (Southeast Missouri State University), Benjamin Cahill (Southeast Missouri State University), Yumin Zhang (Southeast Missouri State University)

In this paper a circuit with double-coupled oscillators is investigated by experiment, simulation and theoretical analysis. Without the external coupling, the two oscillators will compete for bias current, and the one with higher oscillation frequency grabs most of the bias current, and the other one is starved to death. With external coupling, a waveform with a beat pattern is generated. In general, a good agreement is achieved from these different approaches.

Area Efficient Low Power Crystal Oscillator with Automatic Amplitude Control 731
Saravanan Kathiah (Indian Institute of Technology Madras), Sankaran Aniruddhan (Indian Institute of Technology Madras)

A CMOS Crystal Oscillator with automatic amplitude control (AAC) is presented which occupies low area and consumes lower current when compared to existing state of the art designs. Amplitude control loop based implementations of low frequency crystal oscillators usually achieves low-power operation at the expense of die area. The proposed design aims at reducing the overall area by replacing the bulky RC loop filter with a switched capacitor filter operating on the clock generated by the oscillator itself. The circuit is reduced to its basic form after removing redundant branches and devices consuming high voltage headroom, thereby minimizing power dissipation and maximizing operational supply range. The implementation and comparisons are done for 32 kHz in TSMC 65nm CMOS process. The crystal oscillator core consumes 82nA, occupies 12500um^2 and works reliably over PVT variation

Low-Noise Optical Receiver Front-End using Narrow-Bandwidth TIA and Cascaded Linear Equalizer 735
Diaa Abd-elrahman (Concordia University), Glenn Cowan (Concordia University), Odile Liboiron-Ladouceur (McGill University)

In this paper, the sensitivity of the optical receiver is revisited. An analytical expression that reveals the dependency of the sensitivity on both the data rate (f_{bit}) and the bandwidth shrinkage factor (n) is derived. The proposed sensitivity model provides guidelines for selecting the front-end topology. Based on that model, a three-stage front-end is implemented in 65 nm CMOS technology and 18 Gb/s data rate is targeted. The proposed front-end consists of a narrow-bandwidth TIA followed by a two-stage continuous time linear equalize (CTLE). For a total input capacitance (C_T) of 200 fF, the proposed front-end achieves simulated transimpedance gain of 65.2 dBΩ with 9.7 GHz bandwidth and sensitivity of –21.1 dBm, while consuming only 3.4 mW from a single voltage supply of 1V. A net 1.5x enhancement in the sensitivity and 49% reduction in power dissipation are obtained when compared with a conventional front-end achieving the same bandwidth.

A Tunable Immitance Simulator with a Voltage Differential Current Conveyor 739
Bilgin Metin (Bogazici University), Mesut Atasoyu (Istanbul Technical University), Emre Arslan (Marmara University), Norbert Herencsar (Brno University of Technology), Oguzhan Cicekoglu (Bogazici University)

In this paper, an electronically tunable immitance circuit is proposed. The presented circuit can be configured as a tunable grounded inductor or capacitor multiplier. The proposed circuit empolys a single active element called Voltage Differential Current Conveyor, and a resistor and a capacitor. The presented circuit does not require element matching constraints. It is linearly tunable over four decades of frequency using bias current control. Simulation results are included to verify theory.

Passive 3rd Order Delta-Sigma ADC with VCO-Based Quantizer 743
Mahmoud Sadollahi (Oregon State University), Gabor C. Temes (Oregon State University)

A passive delta-sigma ADC with a voltage-controlled-oscillator (VCO) quantizer is presented. By employing the VCO quantizer, a single-bit quantizer is replaced with a multi-bit quantizer while an extra order of noise-shaping was provided. The proposed architecture does not need very large capacitors as compared to the conventional passive delta-sigma ADC. Furthermore, it also does not require external dynamic element (DEM) matching, because the VCO has an inherent DEM. Since there is attenuation in the passive integrators, the input signal range to the VCO is small and within the linear range of the VCO, therefore the nonlinearity of the VCO does not matter. Both conventional second order passive delta-sigma and the proposed structure has been simulated for comparison. The simulation results verify the effectiveness of the proposed structure.

Continuous-Time Delta-Sigma Modulator with Maximally Flat Signal Transfer Function using Minimum Number of DACs 747
Changsok Han (University of Florida), Arun Javvaji (University of Florida), Nima Maghari (University of Florida)

This paper presents a design methodology to achieve maximally flat signal transfer function (STF) in continuoustime delta-sigma modulators (CTDSMs). A 4th order CTDSM with a chain of feedback (CIFB) structure is used to achieve maximally flat STF, while the required number of digital-toanalog converters (DACs) in the traditional CIFB structure is minimized. Therefore, both high in-band dynamic range and low power/area can be achieved by using the proposed scheme. Detailed Cadence and Matlab simulations are provided to prove the operation of the proposed scheme.

An Ultra-High Q Inductorless Narrowband Filter based on the Voltage Divider Phase Shift Method 751
David J. Comer (Brigham Young University)

An active narrowband filter with Q values reaching several thousand is reported. The nested voltage division phase shift method is used. These filters can function at very low frequencies or at very high frequencies. Such values of Q have never been achieved except in crystal filters and have never been achieved at the low frequencies at which this filter can operate.

Fractional Harmonic Distortion Calculation using Simplified "Reconciliation" Model for a MOST Operating in Moderate Inversion 755
I.M. Filanovsky (University of Alberta), L.B. Oliveira (Universidade Nova de Lisboa), N.T. Tchamov (Technical University of Tampere)

The paper describes evaluation of the first, second and (with most attention to) third harmonics of the drain current in a MOS transistor operating in moderate inversion. The dependence of this current on the gate-source voltage is approximated using a simplified "reconciliation" model developed by Y. Tsividis. Then, the drain current components depending exponentially on normalized signal voltage are calculated using modified Bessel functions. This approach indicates that the third harmonic has two "sweet spots" (zero values) but the location of that one corresponding to moderate inversion changes with the signal amplitude. This change makes impossible application of this point for circuit linearization. The second "sweet spot" is corresponding to the strong inversion, and may be used for this purpose. The results of proposed calculation method are compared with that using the traditional approach, for example, Taylor series expansion of the drain current expression for small signal. The traditional method misses the above described, for moderate inversion, detrimental effect of signal amplitude or even loses completely the presence of these spots.

A Gm-C Complex IF Filter using Fully Differential Transconductor for Dual-Mode GNSS Receiver 759
Jing Zhao (Wuhan University), Yichuang Sun (University of Hertfordshire), Jingnan Liu (Wuhan University)

A fourth-order Butterworth active Gm-C complex IF filter for dual-mode GNSS receiver is presented. This filter operates at center frequency of 7.161MHz and in bandwidth of 4MHz with pass-band gain of over 10dB and image rejection of over 35dB, which meets requirements of BD2 and Galileo Systems. The proposed CMOS fully differential transconductor has wide tuning range, high linearity and low power dissipation. The theoretical and simulation results are in good agreement.

A 0.5V Fully Differential Transimpedance Amplifier in 65-nm CMOS Technology 763
Hugo García-Vázquez (Université de Mons), Fortunato Carlos Dualibe (Université de Mons), Grigory Popov (Université de Mons)

This paper proposes a novel fully differential ultra-low voltage transimpedance amplifier (TIA) based on a CMOS translinear circuit. Following a simple bias strategy, its transimpedance gain can be adjusted to the desired accuracy either by means of an external resistor or using internal voltage and current references. To a first order approach, the transresistance results independent from technological parameters. The amplifier does not need a common mode feedback circuit (CMFB) to set the quiescent output voltages. The circuit was sized and simulated in a 65-nm CMOS process to comply with a 10kΩ transimpedance gain and 1MHz@1pF bandwidth. For a 0.5V supply voltage the total power consumption is 78.5µW.

Digital LDO with Analog-Assisted Dynamic Reference Correction for Fast and Accurate Load Regulation 767
Abhirup Lahiri (STMicroelectronics), Shrestha Bansal (Indraprastha Institute of Information Technology Delhi), Nitin Bansal (STMicroelectronics), Mohammad S. Hashmi (Indraprastha Institute of Information Technology Delhi)

Digital LDOs (DLDO) have recently attracted circuit designers for their low voltage operating capability and load current scalability. In this work, we propose to improve the DC load regulation and transient performance by using a dual-loop architecture. The proposed regulator uses a fast control loop for improved transient response and an analog assisted dynamic reference correction loop for improved DC load regulation. The design achieved a DC load regulation of 0.005mV/mA and a settling time of 139ns while regulating loads up to 200mA. The proposed DLDO is designed in 28nm FD-SOI technology with a 0.027mm2 active area.

Split-Transistor Compensation: Analytical Model 771
Venkat Harish Nammi (New Mexico State University), Paul M. Furth (New Mexico State University)

Split-transistor compensation (STC) is introduced as a new compensation technique applicable to power management of Internet-of-Things (IoT) devices. An extension of the splitlength compensation (SLC) technique, STC significantly reduces the area of the required on-chip compensation capacitor, while maintaining the two major benefits of SLC: reduced minimum supply voltage and no additional power consumption. We develop equations to model split-transistor behavior in a compensation network and verify the proposed analytical model via simulations using foundry transistor models.

Session B2P-L: Communications

Chair: Sleiman Bou-Sleiman, *Intel Corporation*
Time: Tuesday, August 8, 2017, 13:00 - 14:20
Location: Ballou Hall - Coolidge Room

Adaptive 4PAM Decision Feedback Equalizer with Reduced Number of Slicers 775
Yushi Zhou (Lakehead University), Fei Yuan (Ryerson University)

This paper presents a comparative study of dual-adaptive DFE for 4PAM serial links with a reduced number of error slicers. Two set of SS-LMS DFE, one for optimal DFE tap coefficients and the other for optimal reference for error generation are employed. The data-dependent nonlinear characteristics of channels and their effect on the choice of the reference for error generation are investigated. We show that the data-dependent nonlinear characteristics of channels give rise to unequal voltage spacing between adjacent data symbols. We further show that the performance of DFE with only one reference is affected by the choice of the reference for error generation with the reference corresponding to $D_2D_1=11$ yielding the best performance. The theoretical findings are verified using the simulation results of a 2 Gbps serial link over a 10-inch FR4 channel designed in an IBM 130 nm CMOS technology.

A High-Throughput Clock-Less Architecture for Soft-Output Viterbi Detection 779
Arnab Dey (Indian Institute of Science), Sebin Jose (Indian Institute of Science), Kuruvilla Varghese (Indian Institute of Science), Shayan Garani Srinivasa (Indian Institute of Science)

Viterbi detectors are widely used in data recording channels in the timing loop as well as in the digital back end before error-correction decoding to detect data in the presence of inter-symbol interference (ISI) and noise. Further, soft reliability values assist in the decoding of outer codes. The state-of-the-art implementations of the Viterbi algorithm are synchronous which consider the 'worst-case' propagation delays of the combinational blocks for the purpose of timing analysis. This can be avoided by using asynchronous circuits that offer 'average case' latencies without a clock distribution network which is one of the most power-consuming units in the existing integrated circuits. In this paper, we present a high-throughput clock-less architecture for a soft-output Viterbi detector. In 180-nm technology node, we obtain a 66.7% reduction in the power consumption for our asynchronous design in comparison to a synchronous version of the detector with throughput requirements of the order of 1.5 Gb/s. Simulation results in 65-nm technology results in 44.2% reduction in power consumption sustaining a throughput of 2.4 Gb/s.

A Low Complexity SCMA Detector based on Stochastic Computation 783
Kaining Han (University of Electronic Science and Technology of China), Jianhao Hu (University of Electronic Science and Technology of China), Jienan Chen (University of Electronic Science and Technology of China), Gerald E. Sobelman (University of Minnesota)

Sparse Code Multiple Access (SCMA) is a promising multiple access technology candidate for 5G wireless communication systems. The high detection complexity is its bottleneck. Stochastic computation is an ultra-low complexity digital signal processing technique in which probabilities are represented and processed with streams of random bits. In this paper, we propose a novel low complexity stochastic iterative detection approach for SCMA detection based on stochastic computation. We refer it as stochastic SCMA detector. Analysis and simulation results show that the proposed stochastic SCMA detector has only 36% hardware complexity compared to previous state-of-the-art soft input soft output (SISO) SCMA detector with satisfied BER performance.

Session B2P-M: RF and Wireless Circuits and Systems

Chair: Mona Hella, *Rensselaer Polytechnic Institute*
Co-Chair: Joseph Bardin, *University Mass Amherst*
Time: Tuesday, August 8, 2017, 13:00 - 14:20
Location: Ballou Hall - Coolidge Room

A Wideband Simplified Transformer-Based VCO with Digital Amplitude Calibration 787
Xinchi Gao (Shanghai Jiao Tong University), Licheng Xu (Shanghai Jiao Tong University), Jing Jin (Shanghai Jiao Tong University), Naifeng Jing (Shanghai Jiao Tong University), Jianjun Zhou (Shanghai Jiao Tong University)

A wideband transformer-based CMOS VCO with simplified topology and digital amplitude calibration is proposed. Owing to the digital amplitude calibration, the immunity to process, temperature and voltage supply variations is improved and a considerable reduction of power consumption is observed. The simplified topology will optimize the phase noise performance by reducing active devices. It achieves a phase noise of -118.2 dBc/Hz at 1 MHz offset at the highest frequency and draws 31 mA. The tuning range is 68.8% at 9.15 GHz center frequency, while the figure-of-merit including the tuning range is -202.2.

An 8.5-12.5GHz Wideband LC PLL with Dual VCO Cores for Multi-Protocol SerDes 791
Yajun He (Tsinghua University), Ziqiang Wang (Tsinghua University), Han Liu (Tsinghua University), Fangxu Lv (Tsinghua University), Shuai Yuan (Tsinghua University), Chun Zhang (Tsinghua University), Zhihua Wang (Tsinghua University), Hanjun Jiang (Tsinghua University)

This paper presents a wideband LC PLL designed for multi-protocol serial link applications. Dual LC voltage controlled oscillator (VCO) cores are used to cover a wide frequency range while keep a high Q factor of the LC tank, and multi-ratio dividers are used to satisfy the multi-protocol requirements. Each LC VCO adopts a 4-bit switch capacitor to increase the frequency tuning range and decrease the VCO gain. Meanwhile, the phase frequency detector (PFD), charge pump, and loop filter (LPF) are fully differential to suppress the ground and substrate noise. The PLL is implemented in SMIC 40nm CMOS technology and covers an area of 0.32mm2. The two VCOs' free running phase noise at 1MHz are -108.1dBc/Hz and -105.7dBc/Hz respectively. The whole power of the PLL under 1.1V supply is 19.52mW, comprising 4.56mW of the VCO and 14.96mW of the other parts.

Power-Bandwidth Trade-Off Analysis of Multi-Stage Inverter-Type Transimpedance Amplifier for Optical Communication 795
Akitaka Hiratsuka (Kyoto University), Akira Tsuchiya (University of Shiga Prefecture), Hidetoshi Onodera (Kyoto University)

This paper discusses an analytical method for performance estimation of multi-stage transimpedance amplifier (TIA). For high speed and energy efficient optical communication, multi-stage TIA are commonly used. However, it is not clear how to decide design parameters. Additionally, the number of stages is also a design parameter. We propose an analytical performance estimation to achieve the highest bandwidth or the highest energy efficiency and clear the design parameters. Our method shows trade-offs between the power and the bandwidth under various number of stages.

An LC Voltage-Controlled Oscillator with Supply Sensitivity Compensation Method 799
Mohammad Radfar (University of California-Irvine), Michael M. Green (University of California-Irvine)

The mechanism by which the frequency of an LC VCO is sensitive to the power supply is analyzed. It is shown that variations in both the common-mode and differential-mode components can give rise to periodic jitter in the presence of supply variations due to capacitive nonlinearities. A new compensation method that reduces this sensitivity is presented. Simulations are shown verifying that this method can reduce the periodic jitter by more than 80%.

Future Directions for GaN in 5G and Satellite Communications 803
Kelvin Yuk (University of California, Davis), G.R. Branner (University of California, Davis), Can Cui (University of California, Davis)

GaN will play a strong role in advanced RF and microwave applications including 5G and satellite communications. The specifications of these systems will push next-gen GaN devices towards mm-wave operation. The challenges and opportunities for commercial deployment of GaN are identified and a variety of circuit designs are presented. A 5G high-linearity power amplifier MMIC in 0.20um GaN with Pout=36dBm at 51.1% PAE and a Sat-com Ku-band mixer in 0.25um GaN with conversion loss <10.1dB and IIP3=36.4dBm are demonstrated.

Session B3L-A: Analog and Mixed-Signal Circuits I

Chair: Oguzhan Cicekoglu, *Bogazici University*
Time: Tuesday, August 8, 2017, 14:40 - 16:20
Location: Braker Hall 001

Passive Sensors for Flexible Hybrid-Printed Electronics' Systems: An IC Designer View 807
Christian Fayomi (Université du Québec à Montréal), Herve Achigui Facpong (Kionix Inc.), Judith Mueller (Synapse IC LLC), Gordon W. Roberts (McGill University)

Printed electronics have gained increased interest over the past years and printed sensors, which promise mechanically flexible multifunctional electronics over large areas, are raising remarkable attention. Numerous low cost printing technologies have been developed on different flexible/stretchable substrate including textile. This paper presents a brief summary of various passive sensors (humidity, temperature, and pH) printed on diverse flexible substrates from an integrated circuits and systems' design standpoint and for use in flexible hybrid-printed electronics' systems. A description of possible application domain of flexible sensors is provided

An Improved Ring Amplifier with Process- and Supply Voltage-Insensitive Dead-Zone 811
Yuefeng Cao (Fudan University), Yongzhen Chen (Fudan University), Tianli Zhang (Fudan University), Fan Ye (Fudan University), Junyan Ren (Fudan University)

Conventional ring amplifier suffers from stability problem, the problem is exacerbated when process, voltage and temperature (PVT) variations are taken into considerations. Prior works are mainly focused on stability problem, the influence of PVT on transient response were barely discussed. In this paper the influence of process variations on stability and transient response is analyzed, a process- and supply voltage-robust ring amplifier is presented. The mechanism of the proposed process- and voltage-insensitive dead-zone is analyzed. Simulations showed that the proposed ring amplifier stays stable and maintains good transient performance over different process corners, the stability with supply voltage variations is also improved.

A Super Class-AB OTA with High Output Current and No Open Loop Gain Degradation 815
Shirin Pourashraf (New Mexico State University), Jaime Ramirez-Angulo (New Mexico State University), Antonio J. Lopez-Martin (Universidad de Navarra), Ramon González-Carvajal (Universidad de Sevilla)

A scheme to achieve simultaneously extremely high slew rate improvement and avoiding open loop gain degradation in one stage super class-AB op-amps is introduced. It overcomes the serious shortcoming of super class-AB OTAs that show very high output current enhancement factors at the expense of degrading the open loop gain. The proposed scheme uses dynamically biased cascode transistors to avoid gain and slew rate degradation. Experimental results of a fabricated super class-AB OTA in 180 nm CMOS technology with open loop gain of 67 dB, a factor two improvement in GBW and a current enhancement factor of 270 verify the proposed scheme.

Session B3L-B: System Security Architecture

Chair: Massi Corba, *Draper Laboratory*
Time: Tuesday, August 8, 2017, 14:40 - 16:20
Location: Eaton Hall 201

Exploiting Hardware Obfuscation Methods to Prevent and Detect Hardware Trojans 819
Qiaoyan Yu (University of New Hampshire), Jaya Dofe (University of New Hampshire), Zhiming Zhang (University of New Hampshire)

Integrated circuits are suffering potential security attacks from the globalized semiconductor supply chain. Among various hardware attacks, hardware Trojan insertion has emerged as a major security concerns. Adversary modifies the original circuit to accomplish the malicious intentions through hardware Trojans. Hardware obfuscation has been demonstrated as a promising technique to strengthen hardware implementation against hardware Trojan insertion in the late stage of the supply chain. This work reviews the state-of-the-art hardware obfuscation methods, with the special emphasis on the corresponding efforts made for hardware Trojan prevention and detection. Furthermore, we summarize the evaluation metrics utilized in literature to assess the effectiveness of hardware obfuscation methods. Future directions for hardware obfuscation against hardware Trojans are discussed in this work, as well.

Advancing the State-of-the-Art in Hardware Trojans Design 823
Syed Kamran Haider (University of Connecticut), Chenglu Jin (University of Connecticut), Marten van Dijk (University of Connecticut)

Electronic Design Automation (EDA) industry heavily reuses third party IP cores which are vulnerable to insertion of Hardware Trojans (HTs) at design time by third party IP core providers. State of the art research has shown that existing HT detection techniques, which claim to detect all publicly available HT benchmarks, can still be defeated by carefully designing new sophisticated HTs. The reason being that these techniques consider the HT landscape to be limited only to the publicly known HT benchmarks. However the adversary is not limited to these HTs and may devise new HT design principles to bypass these countermeasures. In this paper, we discover certain crucial properties of trigger activated HTs which lead to the definition of an exponentially large class of Deterministic Hardware Trojans H_D that an adversary can (but is not limited to) design. The discovered properties serve as HT design principles which help us understand the tremendous ways available to an adversary to design a HT, and show that the existing publicly known HT benchmarks are just the tip of the iceberg on this huge landscape.

Janus: An Uncertain Cache Architecture to Cope with Side Channel Attacks 827
Hossein Hosseinzadeh (Boston University), Mihailo Isakov (Boston University), Mostafa Darabi (Boston University), Ahmad Patooghy (Boston University), Michel A. Kinsy (Boston University)

Side channel attacks are a major class of attacks to crypto-systems. Attackers collect and analyze timing behavior, I/O data, or power consumption in these systems to undermine their effectiveness in protecting sensitive information. In this work, we propose a new cache architecture, called Janus, to enable crypto-systems to introduce randomization and uncertainty in their runtime timing behavior and power utilization profile. In the proposed cache architecture, each data block is equipped with an on-off flag to enable/disable the data block. The Janus architecture has two special instructions in its instruction set to support the on-off flag.

Session B3L-C: Energy Harvesting Circuits and Systems

Chair: Thomas Vandervelde, *Tufts University*
Time: Tuesday, August 8, 2017, 14:40 - 16:20
Location: Eaton Hall 202

A Circuit for Simultaneous Optical Data Reception and Energy Harvesting 831
Xiaozhe Fan (Purdue University), Walter D. Leon-Salas (Purdue University)

A circuit for simultaneous optical data reception and energy harvesting using a photovoltaic cell is presented. This circuit is based on a DC-DC boost converter modified to also work as an optical communications receiver. The circuit is able to boost the low voltage of a typical silicon photovoltaic cell to a level that can be used to drive an electronic circuit. The data receiver portion of the circuit comprises a current-sense resistor, two amplification stages and a comparator. Measurements results using a laser diode as the light source show that a bit error rate of 1.25E-3 at 160 kbps is achieved for binary PAM with logic 0 represented by a 5 mW laser beam and a logic 1 with no light. The power delivered by the circuit to a 50 kOhms load is 359.6 uW when the laser beam is modulated at 160 kbps. The conversion efficiency of the converter is 73.4% and efficiency of the employed solar cell is 15.6%.

A Fully Integrated Charge Pump using Parasitics to Increase the Usable Capacitance by 25% and the Efficiency by up to 18% with Poly-Poly Capacitors 835
Hossein Ghafarian (Albert-Ludwigs-Universität Freiburg / Technische Universität Berlin), Christian Moranz (Albert-Ludwigs-Universität Freiburg), Mahdi Rajabzadeh (Albert-Ludwigs-Universität Freiburg), Joachim Leicht (Albert-Ludwigs-Universität Freiburg), Y. Manoli (Albert-Ludwigs-Universität Freiburg / Hahn-Schickard)

A novel advanced layout of an integrated capacitor is used to improve the efficiency of a voltage double charge pump. The architecture of the charge pump is explained and implemented with three different types of capacitors, comparing their overall efficiency. The importance of stray capacitance of the integrated capacitors in charge pump efficiency is studied and with use of the stray capacitance and junction capacitors of an advanced layout of a double poly is presented. The measurement results show an improved efficiency up to 18% achieving a total maximum efficiency of 77.9% in comparison to the same architecture using a simple double poly capacitor.

A 0.13 µm CMOS Power Conditioning Circuit for Piezoelectric Vibration Energy Harvesters 839
Abdul Hafiz Alameh (École de Technologie Supérieure), Frederic Nabki (École de Technologie Supérieure)

Piezoelectric harvesters have been subject to a growing interest in recent years as they can provide a clean source of energy. To extract the power from the harvester, power conditioning circuits are required. In this article, a circuit is proposed to meet the requirements of relatively high efficiency, very low-voltage operation, good load regulation and sufficient DC output voltage. A combined cross-coupled rectifier and a switched capacitor DC-DC converter is designed and simulated in a CMOS 0.13 µm technology to provide a stable DC supply (1.2 V) to power integrated autonomous sensor systems.

Optimization of GaSb Thermophotovoltaic Diodes with Metallic Photonic Crystal Front-Surface Filters 843
Abigail S. Licht (Tufts University), Corey S. Shemelya (Tufts University / University of Kaiserslautern), Dante F. DeMeo (Tufts University), Emily S. Carlson (Tufts University), Thomas E. Vandervelde (Tufts University)

In this paper we report on the optimization of gallium antimonide thermophotovoltaic diodes with front-surface metallic photonic crystals. The device structure was simulated with Atlas-Silvaco where diode optimization was achieved by varying the constituent layer thicknesses and adding back-side field layers. An intrinsic region was added to the device structure to take advantage of the shifted photogenerated profile due to the metallic photonic crystals. The optimized TPV diode structure are being grown by molecular beam epitaxy and fabricated with the MPhCs to further explore the effect of these structures.

Passive Cooling of Solar Cells with a Comprehensive Photonic Approach 847
Wei Li (Stanford University), Yu Shi (Stanford University), Kaifeng Chen (Stanford University), Linxiao Zhu (Stanford University), Shanhui Fan (Stanford University)

We present a comprehensive photonic approach for passive cooling of solar cells by simultaneously performing radiative cooling while also selectively utilizing the sunlight. We design a photonic cooler made of multilayer dielectric stack that can strongly radiate heat through its thermal radiation while also significantly reflecting the solar spectrum in sub-band gap and ultraviolet regime. We show that applying this photonic cooler on solar panel can cool the solar cell by over 5.7K in a typical terrestrial operating condition. Our technique points to an optimal photonic approach for passive cooling of solar cells and can be readily implemented as a retrofit for current photovoltaic modules to improve both efficiency and reliability.

Session B3L-D: Signal Processing III

Chair: Neeraj Magotra, *WNEU*
Time: Tuesday, August 8, 2017, 14:40 - 16:20
Location: Eaton Hall 203

Parameter Identification of a Double Barrier Memristive Device 851
Enver Solan (Ruhr-Universität Bochum), Karlheinz Ochs (Ruhr-Universität Bochum)

Memristive systems are nonlinear resistors with memory. Most of them are realized as resistive switching devices in nanotechnology. One example, with appropriate properties especially in neuromorphic applications, is the double barrier memristive device (DBMD). A continuous resistance range makes the DBMD suitable for replacing the synapses in neuromorphic circuits. Structural and functional descriptions based on physical insights can help in order to get a parametric concentrated model of the device for both reproducible investigations as well as emulations. Achieving physically meaningful values for model parameters in order to fit the measured data is not trivial. We propose a parameter identification method based on an optimization problem. Because of very fast and efficient algorithms, the wave digital method has been utilized in the objective function. As an example, a reduced model of the DBMD with optimized parameters for fitting the measured data is shown.

A Consistent Modeling of Passive Memcapacitive Systems 855
Karlheinz Ochs (Ruhr-Universität Bochum), Enver Solan (Ruhr-Universität Bochum)

Memelements - circuit elements with memory - serve novel applications in several technical disciplines. Due to similar functionalities to synapses, they are especially suitable for neuromorphic circuits. Physical and chemical phenomena in nanoscale lead to the unique information storage characteristic of these elements. Fabrication of devices with memory considering a particular desired functionality is still difficult to achieve. Therefore, simulation models based on a consistent modeling approach are needed. A consistent model in this context should consider important energetic properties of the real device, e.g. passivity. We propose a novel circuit theoretic approach for a consistent modeling of lossless memcapacitive devices. They can be interpreted as nonlinear capacitances with memory. A comparison with existing modeling approaches of such elements underlines benefits as well as the necessity of a consistent model. The strategy introduced here is more general and independent of the underlying model. Beside simulations, it can also be utilized in emulations regarding real-time capable implementations.

Compressive Sensing-Based DOA Estimation using the Dantzig Selector 859
Amgad A. Salama (Concordia University), M. Omair Ahmad (Concordia University), M.N.S. Swamy (Concordia University)

In this paper, a new compressive sensing (CS)-based direction of arrival (DOA) estimation technique using the Dantzig selector is proposed. The proposed scheme can identify more source signals than the number of sensors used, without requiring an a priori knowledge of the number of source signals to be estimated and without any constraint or assumption about the nature of the signal sources using a fewer number of snapshots. The performance of the proposed scheme is compared to that of the Zhang penalty-based algorithm and the MVDR A-LASSO DOA estimation technique. The computational complexity of the proposed algorithm is substantially lower than that of the Zhang penalty-based method or MVDR A-LASSO.

A Spectral Entropy-Based Measure for Performance Evaluation of a First-Order Differential Microphone Array 863
Ali Sarafnia (Concordia University), M. Omair Ahmad (Concordia University), M.N.S. Swamy (Concordia University)

For differential microphone arrays, most of the performance evaluation measures that are used in the context of noise reduction are based on the energy of the signal. In this paper, we propose a spectral entropy-based measure, which quantifies the ratio of the spectral information contained in the desired and actual outputs of the microphone array, and can evaluate the performance in terms of the average of lost/gain information. At the same time, the value of the spectral entropy-based measure shows whether a speech signal is noisy or if some information has been lost. The proposed measure provides some advantages over the energy-based measures, such as the array gain. Moreover, the performance of a first-order-differential microphone array designed based on the maximum value of the array gain is evaluated using the proposed spectral entropy-based measure.

Session B3L-E: Sensor Circuits and Systems I

Chair: Nicole McFarlane, *University of Tennessee, Knoxville*
Co-Chair: Gymama Slaughter, *University of Maryland, Baltimore County*
Time: Tuesday, August 8, 2017, 14:40 - 16:20
Location: Eaton Hall 206

Near Breakdown Spectral Responsivity of Perimeter-Gated Single-Photon Avalanche Diodes 867
Marc Dandin (Kiskeya Microsystems LLC), Pamela Abshire (University of Maryland-College Park)

This paper investigates the near-breakdown spectral responsivity of perimeter-gated single-photon avalanche diodes (SPADs). We report, for the first time, the effects of perimeter gating on spectral responsivity. Further, we describe a detailed experimental procedure for measuring spectral response. Our investigation reveals that perimeter gating strongly influences spectral responsivity by broadening the response over the visible range, confirming that perimeter gating activates the volumetric junction of the measured devices.

Equivalent Circuit Analysis with Experimental Verification for Barrel-Stave Flextensional Transducers and Arrays 871
Zhengyao He (Northwestern Polytechnical University), Xiuchun Li (Northwestern Polytechnical University)

The equivalent circuit model parameters of the barrel-stave flextensional transducer and array are calculated using the circuit principle together with the finite element, boundary element method and the measured results. The electro-acoustic characteristics of the transducers and arrays are analyzed by the obtained equivalent circuit model. The resonant frequencies and admittance curves of the transducers and arrays are calculated and verified by the experimental results in the anechoic water tank. The equivalent circuit model can be used to direct the design of the barrel-stave flextensional transducers and arrays.

A Low Noise Front-End Amplifier for Pyroelectric Transducer based Respiration Monitoring System 875
I. Mahbub (University of Tennessee), S. Shamsir (University of Tennessee), S.K. Islam (University of Tennessee), S.A. Pullano (Università degli studi Magna Græcia di Catanzaro), A.S. Fiorillo (Università degli studi Magna Græcia di Catanzaro)

This paper reports a low-power low-noise folded-cascode OTA based charge amplifier designed to be used as the front-end amplifier for a pyroelectric transducer based respiration monitoring system. The charge amplifier is designed in 0.5µm standard CMOS process and consumes only 5.4 µW of power with 1.8V supply voltage. The operational transconductance amplifier (OTA) adopts a pseudo-resistor based diode-connected MOSFET in the feedback configuration to achieve a 1 mHz low corner frequency. Measurement results show an input referred noise of only 5.017 µVRMS over the frequency range of 125 mHz to 10 kHz. Test results also include the recording of the respiratory signal acquired by the pyroelectric transducer and the charge amplifier.

Self-Powered Continuous Time-Temperature Monitoring for Cold-Chain Management 879
Liang Zhou (Washington University in St. Louis), Shantanu Chakrabartty (Washington University in St. Louis)

Temperature management of the food supply-chain is important for ensuring compliance and the quality of perishable products like vaccines and fish. While conventional strategies have relied on using monitors attached to packaging containers, self-powered time-temperature monitoring is attractive because the technology can be embedded with passive RFID tags and can be integrated with every food or medical package. In this paper we propose a self-powered sensor that can monitor the time-temperature information without the need for any external powering. The sensor exploits the physics of Fowler-Nordheim (FN) tunneling where electrons are thermally excited and are continuously integrated on a floating-gate. The steady-state FN integrator's response depends on the temperature and corresponds to a temporal curve that is unique to a specific ambient temperature. Deviation from the set ambient temperature results in the deviation from its reference response curve hence can be captured by the sensor. Measured results from sensors prototyped in a 0.5 µm CMOS process show a temperature sensitivity of 1.5mV/C over a monitoring duration of 100 hours.

Sensitivity Improvement of a Photoresistive Image Sensor with Novel Programmable Dual Element Readout and Calibration Method 883
Cagatay Ozmen (University of Massachusetts-Lowell), Aydin Dirican (University of Massachusetts-Lowell), Hieu Nguyen (University of Massachusetts-Lowell), Martin Margala (University of Massachusetts-Lowell)

This paper describes a readout integrated circuit (ROIC) for a nanoscale photoresistive image sensor with a novel dual element readout and calibration method. The dual element readout increases detector signal sensitivity and sensor dynamic range. It works on the assumption that adjacent nanoscale detectors have similar illumination levels. A novel on-chip two point calibration method is also proposed. This image sensor and ROIC system is intended to be used as an endoscope camera which demands strict silicon area and low power consumption requirements.

Session B3L-F: Hardware-Software Co-Design Techniques

Chair: Mark Hempstead, *Tufts University*
Co-Chair: Jose Delgado-Frias, *Washington State University*
Time: Tuesday, August 8, 2017, 14:40 - 16:20
Location: Paige Hall - Crane Room

Non-Volatile Logic SoC with Software-Hardware Co-Design and Integrated Supply Supervisor for Energy Harvesting Applications 887
Michael Zwerg (Texas Instruments Inc.), Sudhanshu Khanna (Texas Instruments Inc.), Steven Bartling (Texas Instruments Inc.)

The industry trend is going to more complex software even on embedded systems. A few examples are graphical display, complex protocol stacks like RF or RTOS. This kind of software does require several thousand CPU cycles on device startup to initialize the variable frame work before the application can start with the intended task. With energy harvesting systems the long startup does phase a certain penalty on power consumption and response time. Non Volatile Logic (NVL) allows building a compute system, that will only go through the initialization cycle once in a lifetime, even if the power supply is interrupted.

Slowing the None-Critical Path to Improve Carry Look-Ahead Adder Power Dissipation 890
Jabulani Nyathi (Eastern Washington University), Abubaker Mutumba (Energy Northwest)

In this paper we use a 4-bit carry look-ahead adder to highlight the contribution by false-starts (glitches) to overall dynamic power dissipation. These false starts occur in the generation of the sum outputs and are due to delays in generating and propagating the carry signals. We employ sub-threshold transistor operation in the none critical path and reduce power dissipation by 40%. Post layout simulations in a 90 nm technology node have been performed and for 1.8 % increase in transistor count we improve power dissipation by 40 %. It is easy to overlook the amount of power dissipation due to false-starts because input and output latches that are typically employed in most synchronous digital systems/circuits mask these glitches. By sampling the signals after they settle at the desired steady state values we can avoid sending the glitches through latches to the sum outputs. This does not however eliminate the power dissipated by the circuit.

Software-Guided Greybox Design Methodology with Integrated Power and Clock Management 894
Tianyu Jia (Northwestern University), Yuanbo Fan (Northwestern University), Russ Joseph (Northwestern University), Jie Gu (Northwestern University)

In this paper, we propose a cross-layer integrated microprocessor design methodology where instructions in software programs drive the design down to the gate level netlists. Based on in-depth exploration of the dynamic timing behavior of each instruction in the program, a fully integrated design approach is proposed with ultra-dynamic clock and power management circuits and software driven design optimization approach. A cross-layer simulation environment is also introduced enabling the collaborative co-design among compiler, architecture and circuits. The proposed design methodology helps bridge the gap between software and hardware development in a conventional development cycle. Our test vehicle using ARM based processor demonstrates substantial improvement on speed and power efficiency using the proposed design methodology.

Combining Architectural Fault-Injection and Neutron Beam Testing Approaches Toward Better Understanding of GPU Soft-Error Resilience 898
Fritz G. Previlon (Northeastern University), Babatunde Egbantan (Northeastern University), Devesh Tiwari (Northeastern University), Paolo Rech (Universidade Federal do Rio Grande do Sul), David R. Kaeli (Northeastern University)

Transient faults continue to be a critical concern in a range of computing domains including: High-Performance Computing (HPC), scientific computing, and the automotive industry. While radiation-induced faults have been well studied and understood in microprocessors, their impact on computations on Graphic Processing Units (GPU) has received less attention. GPUs are now being used in a large number of HPC and automotive markets. Mitigating the effects of transient faults requires a thorough understanding of the interaction between applications, system software, and the underlying hardware. Developing this understanding is quite challenging mainly due to our limited ability to capture and study cross-layer reliability interactions. In this paper, we consider the combination of neutron beam testing experiments with architectural fault injection experiments to gain a deeper understanding of the relationship between the vulnerability of GPUs and the underlying workload characteristics of applications targeted for GPU devices.

Methods and Infrastructure in the Era of Accelerator-Centric Architectures 902
Brandon Reagen (Harvard University), Yakun Sophia Shao (Nvidia Corporation), Sam Xi (Harvard University), Gu-Yeon Wei (Harvard University), David Brooks (Harvard University)

This invited paper presents tools and methods for accelerator and accelerator-centric SoC design. To alleviate the cost of individual accelerator design the Aladdin simulator is presented. For studying accelerator-rich SoCs and memory systems we present gem5-Aladdin. Finally, we conclude with an example of how Aladdin can be used to heavily optimize accelerators for important applications by discussing the Minerva framework for optimizing DNN accelerators, which heavily relies on the Aladdin modeling framework.

Session B3L-G: Emerging Techniques – RF to Optical

Chair: Joseph Bardin, *University Mass Amherst*
Time: Tuesday, August 8, 2017, 14:40 - 16:20
Location: Paige Hall - Terrace Room

Nano-Optical Systems in CMOS 906
Lingyu Hong (Princeton University), Xuyang Lu (Princeton University), Kaushik Sengupta (Princeton University)

Integrated optical systems-on-chip (SOCs) with onchip optical passives in the visible and near-IR range can have a tremendous impact in miniaturizing complex optical instrumentation to enable a new class of ultra-compact, low-cost optical sensors and imagers for a wide variety of emerging applications. In this paper, we present a design methodology where complex optical nano-optical passive structures can be incorporated in CMOS exploiting optical field interaction with sub-wavelength copper-based metal interconnect layers. Co-designed with embedded detection and electronic circuitry, this integrated approach can potentially open the door to a new class of optical SOCs. In this paper, we illustrate this approach with three design examples: the first fully integrated fluorescence-based CMOS bio-molecular sensor with integrated nanoplasmonic filters, the first optical spectrometer in CMOS in visible and near-IR, and the first optical CMOS physically unclonable function (PUF) exploiting process-sensitive photonic crystals, all realized in a 65-nm bulk digital process.

Hybrid PLL System for Spin Torque Oscillators Utilizing Custom ICs in 0.18 µm BiCMOS 910
Martin Kreißig (Technische Universität Dresden), Steffen Wittrock (Université Paris-Sud / Université Paris Saclay), Florian Protze (Technische Universität Dresden), Romain Lebrun (Université Paris-Sud / Université Paris Saclay), Karla J. Merazzo (CEA-SPINTEC), Marie-Claire Cyrille (CEA-LETI MINATEC), Ricardo Ferreira (International Iberian Nanotechnology Laboratory), Paolo Bortolotti (Université Paris-Sud / Université Paris Saclay), Ursula Ebels (CEA-SPINTEC), Vincent Cros (Université Paris-Sud / Université Paris Saclay), Frank Ellinger (Technische Universität Dresden)

This work presents a hybrid and highly adaptive phase locked loop (PLL) system for spin torque oscillators (STO). PLL operation is successfully demonstrated in the lower ultra high frequency (UHF) band using a vortex based STO revealing an in-band phase noise of less than -80 dBc/Hz and PLL bandwidth of 2.5 MHz. The system is highly reconfigurable e.g. in terms of the frequency divider ratio N, RF gain and loop gain which makes it compatible with a large range of STOs. To the best knowledge of the authors this PLL system utilizing a STO exhibits the smallest system size and power consumption among the reported STO-PLLs.

Broadband Noise and Distortion Cancelling Low Noise Amplifier 914
Ahmad Qassem Dawoud (Ain Shams University), Mohamed El-Nozahi (Ain Shams University), Hani F. Ragai (Ain Shams University)

In this paper, a new broadband low noise amplifier (LNA) is proposed. The LNA utilizes a composite NMOS/PMOS cross-coupled transistor pair and a difference amplifier to increase the linearity while reducing the noise figure. The introduced approach provides partial cancellation of distortion and noise generated by the input transistors, hence, degrading the overall distortion. The LNA is implemented by using the UMC 130 nm CMOS technology node. The post simulation shows that a conversion gain equals 16.2 dB across 0.05−3.1 GHz frequency range, an IIP3 is +9.2 dBm, and minimum and maximum noise figure are 1.4 dB and 2 dB, respectively. The LNA consumes 32.4 mW from 1.8 V supply and occupies an area of 0.075 mm^2.

Session B4L-A: Analog and Mixed-Signal Circuits II

Chair: Frédéric Nabki, *ETS Montreal*
Time: Tuesday, August 8, 2017, 16:40 - 18:20
Location: Braker Hall 001

Sub-ps Resolution Programmable Delays Implemented in a Xilinx FPGA 918
Safa Berrima (Polytechnique Montreal), Yves Blaquière (École de Technologie Supérieure), Yvon Savaria (Polytechnique Montreal)

In this paper, a novel way to finely tune a net delay on Xilinx Field Programmable Gate arrays (FPGAs) is proposed. It consists of adding floating interconnects (nodes) to the net on which the delay is to be tuned, connected to any input pin of a switch matrix along the net. Adding nodes is made with a TCL script applied to an already placed and routed design However, such nodes, also called antennas, typically cause fatal errors during the design flow and normally prevent the tools from generating the bit stream. To overcome this issue, a breadth-first search algorithm connecting each node to a load is proposed in this work. Experimental results conducted on a ZYNQ7z010-3clg400 Xilinx FPGA using the Vivado Design suite showed that it is possible to add small delay steps to the net with a resolution under a picosecond and a covered range proportional to the number of added nodes reaching 48.6 ps for a net with 15 added nodes.

CMOS Programmable Time Control Circuit Design for Phased Array UWB Ground Penetrating Radar Antenna Beamforming 922
Nicholas J. Reilly (University of Vermont), Guoan Wang (University of South Carolina), Tian Xia (University of Vermont)

In this paper, a programmable precise time delay generator suitable for a beam forming impulse ground penetrating radar (GPR) is presented. The design is based on a phase locked loop (PLL) circuit that is implemented utilizing Global Foundries 7HV 0.18µm CMOS process. The precise time control realizes the true time delay, which allows for developing an ultrawide band (UWB) phased array GPR system with beam steering capabilities. The simulation results show that the system is capable of generating delays from 100ps to 500ps in 25ps increments, and the corresponding beam angle ranges from 9.6° to 56.4° with a resolution of 2.75°.

10 Gb/s Optical Receiver with Continuous-Time Feed-Forward Equalization 926
Marjan Madani (Concordia University), Glenn E.R. Cowan (Concordia University)

This paper presents a CMOS 65 nm optical receiver design based on a continuous-time feed-forward equalizer (CT-FFE). A low-bandwidth front-end approach increases the mid-band gain and improves sensitivity. However, the inter-symbol interference (ISI) that is introduced must be removed using equalization. The proposed CT-FFE topology mitigates the challenges of sampling present in discrete-time FFEs. In this work, a continuous-time delay is realized with a 1st order, general pole/zero filter. The combination of a low-bandwidth inductorless transimpedance amplifier (TIA), CT-FFE and decision circuits dissipates 13.15 mW from a 1-V supply. The front-end has an equivalent gain of 2500Ω using a 2.7kΩ feedback resistor. It has an input referred noise of 0.32µArms, leading to an estimated noise-limited sensitivity of 4.48 µAp-p in the presence of a pad/photodiode capacitance of 100 fF. A reference design based on a conventional TIA and one-stage Cherry-Hooper amplifier achieved the sensitivity of 5.6 µAp-p and with power dissipation of 29.2 mW.

Signal Conditioning Circuit with Ultra-High Sensitivity and Ultra-Low Power Consumption for MEMS 930
Parisa Vejdani (École de Technologie Supérieure), Anoir Bouchami (Université du Québec à Montréal), Frederic Nabki (École de Technologie Supérieure)

A signal conditioning circuit with ultra-high sensitivity and ultra-low power consumption is presented for the capacitive and voltage mode microelectromechanical systems (MEMS) transducers. Two different amplifiers are chopped with two different frequencies to remove their flicker noise. A low voltage high current amplifier is implemented in the 1st stage, which improves the power consumption and noise floor. The 2nd stage is composed of two parallel paths that improve SNR and provide two gain settings. The circuit is designed in a 0.13 µm CMOS technology with 0.4 V and 1.2 V supplies. The simulated power consumption is of 8.3 µW for a gain of 60 dB and 6.1 µW for a gain of 57 dB. The bandwidth is 10.5 kHz, the input-referred noise is 12.1 nV/√Hz and capacitance noise

Session B4L-B: Trust and Authenticity

Chair: Michel Kinsy, *Boston University*
Co-Chair: Jonathan Frey, *Draper Laboratory*
Time: Tuesday, August 8, 2017, 16:40 - 18:20
Location: Eaton Hall 201

Predicting Hard and Soft-Responses and Identifying Stable Challenges of MUX PUFs using ANNs 934
S.V. Sandeep Avvaru (University of Minnesota), Chen Zhou (University of Minnesota), Chris H. Kim (University of Minnesota), Keshab K. Parhi (University of Minnesota)

In this paper, we present artificial neural network (ANN) models to predict hard and soft-responses of three configurations of arbiter based physical unclonable functions (PUFs): standard, feed-forward (FF) and modified feed-forward (MFF). The models are trained using data extracted from 32-stage arbiter PUF circuits fabricated using IBM 32 nm HKMG process. The contributions of this paper are two-fold. First, we evaluate the unpredictability of the PUFs by predicting hard responses using ANNs and comparing these with ground truth. Second, ANNs are trained to predict soft-responses and a probability based thresholding scheme is used to define stability. The obtained soft-response models are used to identify unstable responses.

A Reliable and Compact Physical Unclonable Function based on Unstable Bits Recycling Scheme 938
Baiyi Huang (George Washington University), Xiaojin Zhao (Shenzhen University), Yuan Cao (Hohai University), Tingbing Ouyang (Peking University)

Physically unclonable functions (PUFs) facilitate many security applications such as secure key generation, device authentication, counterfeiting detection and prevention. This paper presents an area efficient PUF with high reliability. We exploit the process variation of a single load transistor for the current mirror working at the subthreshold region, which is converted to a unique digital signature of the chip. Different from the previous reliability enhancement technologies that discard the unstable bits, the proposed PUF is capable of labelling and recycling the unstable PUF bits, leading to significantly increased reliability. The simulation results based on 65 nm 1.2 V CMOS technology have validated the proposed design, which exhibits a reliability of 97.12% and a uniqueness of 50.06%, with the working temperature varying from -40 °C to 120 °C and the supply voltage's fluctuation equal to ±10%. Moreover, the power consumption of the core PUF is only 8.2 µW at a throughput of 80 Mb/s, which corresponds to 102.5 fJ per response bit.

Analysis of a Novel Stage Configurable ROPUF Design 942
Muhtadi Choudhury (University of Toledo), Nitin Pundir (University of Toledo), Mohammed Niamat (University of Toledo), Muslim Mustapa (Universiti Malaysia Perlis)

Silicon based Physical Unclonable Function (SPUF), a chip level identifier that utilizes the inherent irregular manufacturing process variations, can be extended to Ring Oscillator PUFs (ROPUFs). The ROPUF structure, although promising for FPGA based platforms, is not area efficient in terms of response bit per RO circuit implementation. This paper introduces an area efficient Stage Configurable ROPUF (SCROPUF) design based on XOR gates and a functional block which significantly increases the output frequency comparison pairs. The design is implemented on six Xilinx Artix-7 FPGAs. In this work, the output frequency data from 125 SCROs is evaluated with regard to the following quality factors: uniqueness, uniformity, and bit-aliasing along with the NIST statistical tests for randomness. Also, the average static intra-chip variation is shown to be higher than the noise component signifying higher reliability of the design.

The Effect of Power Supply Ramp Time on SRAM PUFs 946
Abdelrahman T. Elshafiey (University of New Mexico), Payman Zarkesh-Ha (University of New Mexico), Joshua Trujillo (Honeywell)

In this paper, for the first time, it is demonstrated that the startup value of an SRAM PUF could be different depending on the SRAM power supply rising time. An analytical model has been developed to determine the range for the power supply ramp time that affects the SRAM PUF start-up value. It has been found that there are two regions of operation. The generated key could possibly be different from one region to another. An SRAM test chip was designed and fabricated using Tower Jazz's 180 nanometer Silicon Germanium (SiGe) Bipolar/CMOS (BiCMOS) process. Based on our measured data, using the appropriate rising time can decrease the number of flipping bits by 5%. Both simulation and silicon results confirms the analytical model.

Session B4L-C: Photo-Voltaic Devices and Systems

Chair: Joseph O'Connor, *Naval Postgraduate School*
Time: Tuesday, August 8, 2017, 16:40 - 18:20
Location: Eaton Hall 202

Advanced Space Power Technology 950
David Wilt (Air Force Research Laboratory), Kyle Montgomery (Air Force Research Laboratory), Geoffrey Bradshaw (Air Force Research Laboratory), John Merrill (Air Force Research Laboratory)

Photovoltaics continue to be the primary source of electrical power for most near-Sun space missions. The desire to enhance or enable new space missions through higher efficiency, increased specific power density, increased volumetric power density and improved radiation resistance, along with decreased costs, continues to push the development of novel solar cell and array technologies. To meet present and future space power requirements, advanced multijunction solar cells and novel cell technologies are being pursued. These efforts have resulted in a continual advancement in performance, but new paradigms will be required to continue that performance trend. Similarly, new array technologies are being investigated and developed to meet the ever increasing power system performance requirements.

InGaN-Based Solar Cells for Space Applications 954
Yuji Zhao (Arizona State University), Xuanqi Huang (Arizona State University), Houqiang Fu (Arizona State University), Hong Chen (Arizona State University), Zhijian Lu (Arizona State University), Jossue Montes (Arizona State University), Izak Baranowski (Arizona State University)

We demonstrated InGaN/GaN MQW solar cells based on novel nonpolar m-plane and semipolar (2021) plane bulk GaN substrates. Nonpolar m-plane InGaN/GaN MQW solar cell exhibits outstanding PV performance as a result of the improved collection efficiency from the reduced polarization-related effect. Furthermore, a monotonically increasing power conversion at elevated temperature up to 450°C, and broadening EQE spectrums with rising temperature, were observed on nonpolar m-plane InGaN MQW solar cells. Overall, nonpolar m-plane InGaN MQW solar cells exhibit improved PV performance and superior thermal performance, which are critical for high temperature space PV applications.

Photovoltaic Technology for Navy and Marine Corps Applications 958
Phillip Jenkins (U.S. Naval Research Laboratory), Robert Walters (U.S. Naval Research Laboratory)

Photovoltaic (PV) technology development is dominated by the largest application, utility-scale energy generation. Although military PV applications share some of the same attributes as those for utility-scale PV, the Navy PV technology development is focused on filling the gaps between what exists for utility energy generation and specific military applications. In this paper, we discuss the unique aspects of military PV requirements that lead to development of new PV technology for the Navy and Marine Corps.

Design and Simulation of a Novel Mechanically-Stacked Solar Cell 962
Joseph E. O'Connor (Naval Postgraduate School), Sherif Michael (Naval Postgraduate School)

A novel 2-Terminal, 3-Cell, Mechanical-Stack (2T3CMS) is designed and simulated in Silvaco Atlas to overcome instrinsic limitations of state-of-the-art designs. Indium-Gallium-Phosphide, Gallium-Arsenide and Germanium back-contact solar cells are current-matched and connected in series to achieve 32.5 and 29.2 percent power conversion efficiency at AM1.5G and AM0 (300 K), respectively. Two-terminal operation permits a variety of series and/or parallel-connection topologies for module operation. Research is underway to improve efficiency through the use of optimal bandgap materials.

Session B4L-D: Signal and Image Processing: Theory and Methods

Chair: Wasfy Mikhael, *University of Central Florida*
Time: Tuesday, August 8, 2017, 16:40 - 18:20
Location: Eaton Hall 203

Palmprint Recognition based on Histograms of Sparse Codes 965
Waziha Kabir (Concordia University), M. Omair Ahmad (Concordia University), M.N.S. Swamy (Concordia University)

In this paper, we propose a novel palmprint recognition scheme using histograms of sparse codes (HSC) as feature for palmprint image. In the feature extraction stage, the HSC feature is obtained by computing sparse codes for a given dictionary from a palmprint image, which results in a feature image. In the feature encoding stage, a hash table is designed from the feature image using the binary hashing technique. Finally, the hash table is matched with the templates of hash tables for the purpose of identifying an individual. Extensive experiments are performed on three publicly-available palmprint databases. Experimental results show that the performance of the palmprint recognition system using the proposed scheme is superior to that of other schemes in terms of equal error rate (EER), genuine acceptance rate (GAR) at 11% false acceptance rate (FAR), and processing time.

A FPGA-Based Feature Extraction using Reconfigurable Rotated Wavelet Transform for Various Classification Schemes 969
Raunak M. Borwankar (Worcester Polytechnic Institute), Reinhold Ludwig (Worcester Polytechnic Institute)

A novel feature extraction approach using the rotated wavelet transform implemented on a FPGA is presented. The proposed algorithm overcomes the drawbacks of the 2D-DWT such as aliasing and checkerboard effects by generating a new oriented filter set. The RWF (oriented filter) is a 45 degree rotated version of the 1D-DWF. The number of hardware resources, and the power required to implement the 2D-RWT is comparable to the existing 2D-DWT implementations. The most important aspect of the proposed architecture is the fact that the computation time depends on the input image and not on the size of the employed filter.

Facial Recognition with PCA and Machine Learning Methods 973
Jiachen Chen (Pennsylvania State University), W. Kenneth Jenkins (Pennsylvania State University)

Facial recognition is a challenging problem in image processing and machine learning areas. Since widespread applications of facial recognition make it a valuable research topic, this work tries to develop some new facial recognition systems that have both high recognition accuracy and fast running speed. Efforts are made to design facial recognition systems by combining different algorithms. Comparisons and evaluations of recognition accuracy and running speed show that PCA + SVM achieves the best recognition result, which is over 95% for certain training data and eigenface sizes. Also, PCA + KNN achieves the balance between recognition accuracy and running speed.

Face Recognition System based on Features Extracted from Two Domains 977
Taif Alobaidi (University of Central Florida), Wasfy B. Mikhael (University of Central Florida)

A face recognition system which represents each image as a superposition of the dominant components in two, Wavelet and Cosine, transform domains is proposed. By the end of the Training mode, each pose in the gallery will have two final matrices. The Classification mode consists of the same sequence of steps as in the training. The Euclidean distance measure is used to compute the separation of test matrices and the training ones. As shown in the results, the system gives higher recognition rates compared with existing approaches. The other two design parameters were also lower.

Session B4L-E: Nanoelectronics

Chair: Helena Silva, *University of Connecticut*
Time: Tuesday, August 8, 2017, 16:40 - 18:20
Location: Eaton Hall 206

Optimization of Subthreshold Swing for Multilayer MoS2 Tunnel Transistor 981
Muhammad S. Ullah (Florida Polytechnic University), Masud H. Chowdhury (University of Missouri-Kansas City)

The subthreshold swing of metal-oxide-semiconductor field-effect transistor (MOSFET) is fundamentally limited by the thermal voltage (kT/q), which imposes restriction on achievable on-off current ratio or device gain. An alternative to break this thermionic limit of silicon CMOS devices is to adopt tunnel FET (TFET) technology that does not depend on thermal potential. We recently introduced a multilayer molybdenum disulfide (MoS2) based SOI-TFET device to utilize different switching mechanisms to achieve a steeper subthreshold slope (lower value of S) for ultra-low power applications. An analytical model of the subthreshold swing of the proposed device is derived based on its physics and geometry. The model shows that subthreshold swing value is not limited by the factor kT/q in the proposed MoS2 TFET. The design parameters to improve the subthreshold characteristics of the proposed device are studied. An optimization approach is presented based on theoretical study and simulation results.

On-Chip Thermal Management Method based on Phase Change Material 985
Jingyan Fu (North Dakota State University), Seyed Alireza Pourbakhsh (North Dakota State University), Xiaowei Chen (North Dakota State University), Mingli Li (North Dakota State University), Zhibin Lin (North Dakota State University), Ligang Hou (Beijing University of Technology), Frederik Haring (North Dakota State University), Na Gong (North Dakota State University), Jinhui Wang (North Dakota State University)

In this paper, a new package frame with PCM directly touching top of the chips inside the package cavity instead of using PCM-based heat sink is proposed to accelerate this heat dissipation process. The proposed model is verified by carrying out simulations and experiments. To obtain more precise experimental results, the extra tiny thermocouple and chip-level heat generators are utilized. The experimental results show that 2°C - 5°C temperature reductions under 300 mW - 800 mW input which proves the effectiveness of the proposed approach.

Behavioral Modeling and Characterization of Silicon Photonic Mach-Zehnder Modulator 989
Kehan Zhu (MultiPhy, Ltd.), Rui Wang (University of Idaho), Xinyu Wu (University of Idaho), Vishal Saxena (University of Idaho)

Compact behavioral models for silicon photonic Mach-Zehnder modulators (MZM) are developed for SPICE compatible electro-optical co-simulation. The model captures electro-optical interactions and dynamics, optical insertion loss and thermo-optical effect. Behavioral model simulation results and measurement results are shown to be a highly match. The model will be an indispensable part of the optical process design kit (PDK) which can be provided to the integrated circuit designers for hybrid simulation.

Read-Enhanced Spin Memories Augmented by Phase Transition Materials 993
Ahmedullah Aziz (Pennsylvania State University), Sumeet Kumar Gupta (Pennsylvania State University)

This manuscript presents a combined overview of the design approach, challenges and benefits of two proposed ways of designing PTM assisted spin memories. One of the approach that uses a PTM in parallel to MTJ in read path is only applicable for memories with separate read-write path. This approach can achieve over 1.7X better distinguishability in stored data and at least 20% increase in read stability. On the other hand, another design which uses PTM in series with MTJ can be used for a broader spectrum of cell topologies and achieves over 17X boost in cell tunneling magneto resistance 45% higher read stability 45%. No area penalties are associated with any of these techniques.

Session B4L-F: Oversampling Converters

Chair: Vishal Saxena, *University of Idaho*
Time: Tuesday, August 8, 2017, 16:40 - 18:20
Location: Paige Hall - Crane Room

Filtering ADCs for Wireless Receivers: A Survey 997
Qiwei Wang (University of Toronto), Antonio Liscidini (University of Toronto), Anthony Chan Carusone (University of Toronto)

Analog to digital converters (ADC) are used in wireless receivers to process signals in the presence of blockers. These blockers, usually much larger than the signal itself, necessitate the use of a filter upfront to reduce the dynamic range requirement of the ADC. A filtering ADC can be created by placing both the filter and the ADC in a global feedback loop, with improvement in noise and power efficiency. This paper reviews and analyzes two design methodologies for analog filtering ADCs, where the filter response is defined by analog circuits. Then, a digital filtering ADC architecture is discussed that takes advantage of the programmability of digital circuits

High-Speed Oversampled Continuous-Time Analog-to-Digital Converters 1001
Trevor Caldwell (Analog Devices, Inc.), Hajime Shibata (Analog Devices, Inc.)

Oversampled continuous-time analog-to-digital converters are on the verge of surpassing the bandwidth of their discrete-time counterparts due to their ability to operate at higher sampling rates, and through the innovative architectures that have led to a decrease in their oversampling ratios. This paper outlines several architectures that have led to these improvements, which include single-loop delta-sigma modulators, cascaded or MASH delta-sigma modulators, and pipeline data converters.

1-1 MASH ΔΣ Time-to-Digital Converter with Differential Cascode Time Integrator 1005
Young Jun Park (Ryerson University), Fei Yuan (Ryerson University)

This paper proposes a 1-1 MASH $\Delta\Sigma$ time-to-digital converter (TDC). A cascode time adder with a raised inverter threshold voltage is proposed to minimize the jitter caused by current mismatch. A differential time integrator consisting of two single-ended time integrators is proposed to minimize even-order harmonics. The detrimental effect of the nonidealities of the TDC is examined in detail. The TDC is designed in an IBM 130 nm 1.2V CMOS technology and analyzed using Spectre from Cadence Design Systems with BSIM4 device models. Simulation results demonstrate that the TDC yields 2nd-order noise-shaping, 1.9 ps time resolution over 48$\sim$415 kHz signal band while consuming 502 μW. Simulation results show that the TDC yields 2nd-order noise-shaping, 1.9 ps time resolution over 48$\sim$415 kHz signal band while consuming 502 μW.

High Speed Digital ELD Compensation with Hybrid Thermometer Coding in CT ΔΣ Modulators 1009
Hang Hu (Fudan University), Zemin Feng (Fudan University), Chixiao Chen (Fudan University), Fan Ye (Fudan University), Junyan Ren (Fudan University)

In this paper, a high speed digital excess loop delay (ELD) compensation scheme with hybrid thermometer coding is proposed. In this high speed compensation, the time constraint of the DAC feedback route is shifted to a time-abundant path. Also, method to deal with the overflow of quantizer's range is analyzed. Compared to other digital ELD compensations, this scheme features an efficient compensation with a low hardware cost and a high operation frequency. The digital ELD compensation scheme and the algorithm were verified in a design of 3-0 MASH delta-sigma modulator in TSMC 65nm LP CMOS process.

An Incremental Zoom Sturdy MASH ADC 1013
Ki-Hoon Seo (KAIST), Il-Hoon Jang (KAIST), Kyung-Jun Noh (KAIST), Seung-Tak Ryu (KAIST)

This paper introduces a speed-enhanced incremental ADC architecture for high-resolution low-power sensor applications, incorporating a third-order sturdy MASH modulator. Unlike previous sturdy MASH ADCs, owing to the properly modified loop filters in the 2-1 sturdy MASH, the quantization noise of the first noise-shaping loop could be cancelled out. The proposed ADC with a 4b coarse SAR ADC and a 2-1 sturdy MASH modulator is designed for a 0.35um CMOS process. Simulation result achieved an 18b resolution in conversion time of 606 us, consuming 161 uA current under a 3.3V supply.

Session B4L-G: Data Converter Techniques

Chair: Bibhudatta Sahoo, *University of Illinois*
Time: Tuesday, August 8, 2017, 16:40 - 18:20
Location: Paige Hall - Terrace Room

Incremental ADC with Parallel Counting 1017
Tao He (Oregon State University), Chia-Hung Chen (Oregon State University), Yi Zhang (Oregon State University), Gabor C. Temes (Oregon State University)

An incremental ADC (IADC) using parallel counting is proposed to achieve both high accuracy and power efficiency. By operating the IADC and the counting logic alternatively within two clock phases, the proposed scheme finishes a full conversion within fewer conversion cycles. The only additional circuitry for the parallel counting is a single comparator, much less than the add-ons in other multi-step topologies. Also, the parallel counting technique can be implemented with different IADC topologies.

VCO based Nyquist-Rate ADC with FVCO of Fs/2 1021
Chandrasekhar Radhakrishnan (University of Illinois at Urbana-Champaign), Bibhu Datta Sahoo (University of Illinois at Urbana-Champaign)

Relentless pursuit of Moore's law, while providing immense speed, power, and cost benefits in digital circuits, has thrown open many challenges in analog circuit design, especially analog-to-digital converter (ADC) design. Present day ADC's must be able to achieve an extremely high level of performance in terms of both resolution and bandwidth. High-resolution and high-bandwidth input modulated parallel ΔΣ-ADCs have been proposed earlier [1]. However, the large size of a conventional ΔΣ-ADC severely constrains the amount of parallelism. Voltage Controlled Oscillator (VCO) based 1 st-order noise-shaped ADCs being mostly digital in nature can exploit the scaling trend and can therefore be realized in a small area. Thus, using VCO based 1st-order noise-shaping, a large amount of parallelism can be achieved to enable the design of high-resolution, high- bandwidth ADCs. This work provides an intuitive explanation of input modulated parallel ADCs and proposes a 32-channel VCO based ADC operating at a sampling rate, Fs, of 200 MHz and achieving an SNR of 65-dB, with the VCOs in each channel oscillating at a meagre frequency, F vco = Fs/2 = 100 MHz.

Noise and Non-Linearity Analysis of a Charge-Injection-Cell-Based 10-Bit 50-MS/s SAR-ADC 1025
Marcel Runge (Technische Universität Berlin), Dario Schmock (Technische Universität Berlin), Friedel Gerfers (Technische Universität Berlin)

This paper presents a detailed noise and nonlinearity analysis of a 10-bit 1.2Vppd 50MS/s charge-injection based SAR-ADC designed in a 65nm low power process. In contrast to a conventional capacitor DAC, a charge-injection-cell-based DAC is more area efficient due to the reusable nature of the DAC cells. Based on extensive calculations and transistor level simulations, the charge-injection cell design tradeoffs are analyzed and optimized to maximize the overall ADC linearity and ADC input range. Extensive system level simulations in MATLAB evaluate the jitter sensitivity of the system. Combining the transistor-level and system level simulation, a detailed noise study of the 8.86-bit ENOB ADC completes the evaluation.

A Scheme for Wide Input Range Precision SAR ADC 1029
Baozhen Chen (Analog Devices, Inc.)

This paper presents a new scheme for enabling wide input voltage range for SAR (successive approximation register) ADCs. Precision ADC usually favors large input voltage range (>3V), while a push for higher throughput often call for the use of low voltage devices in fine lithography. There are elegant solutions to bridge the gap. Recently a new type of SAR ADCs using passive charge sharing technique or reservoir capacitor techniques emerges. Previous solutions of dealing with large input range cannot work with this newly developed SAR ADCs. This paper presents a new scheme to make a wide input voltage range possible for this type of ADCs. Simulation results confirmed it is an appealing and elegant solution. This scheme is not very exciting for traditional SAR ADCs. But it the only elegant solution for the pass charge sharing ADC as the author now knows.

Wednesday, August 9, 2017

Session C1L-A: Sensor Circuits and Systems II

Chair: Arjuna Madanayake, *University of Akron*
Co-Chair: Kye-Shin Lee, *University of Akron*
Time: Wednesday, August 9, 2017, 9:00 - 10:40
Location: Braker Hall 001

Simulatenous Glucose Sensing and Powering of Glucometer 1033
Tanmay Kulkarni (University of Maryland Baltimore County), Gymama Slaughter (University of Maryland Baltimore County)

Although recent research has theoretically demonstrated that enzymatic glucose biofuel cell can be used to power a contact lens-based glucose sensor, such a practical system does not exist. Here, we developed a novel closed loop system consisting of a charge pump circuit and a step up DC converter circuit that is powered by a single enzymatic glucose biofuel cell at physiological conditions. This system is capable of simultaneously sensing glucose with a sensitivity of 86.42 Hz/cm². M and producing a steady 3.25 VDC output supply to drive low power devices such as commercially available glucometer. Moreover, this system relies on a novel glucose sensing technique which involves the monitoring of the charge/discharge frequency of the transducer capacitor as opposed to the invasive technique currently employed by commercially available glucose monitoring systems that require the implementation of battery-operated potentiostat.

A Reconfigurable Time-to-Digital Converter based on Time Stretcher and Chain-Delay-Line for Electrical Bioimpedance Spectroscopy 1037
Soon-Jae Kweon (KAIST), Jeong-Ho Park (KAIST), Seongheon Shin (KAIST), Sang-Sun Yoo (Pyeongtaek University), Hyung-Joun Yoo (KAIST)

We propose a time-to-digital converter (TDC) with a reconfigurable time resolution from 0.1 ns to 244 ns using a low-speed reference clock of 32.768 MHz. This TDC combines a coarse counter with two parallel fine TDCs which measure front and back fractional times of the coarse counter. In order to obtain high precision without increasing the reference clock speed, the fractional times are stretched through time stretchers of two fine stages with tunable stretching factor and are quantized through fine counters and chain-delay-lines. The time resolution is tuned by controlling the counting clock speed or the stretching factor. The designed TDC in a 0.18-µm CMOS process quantizes a phase of impedance with less than 0.088° error for frequency range from 1 kHz to 2048 kHz. As the result, this TDC is suitable for phase quantizers in bioimpedance spectrometers.

A 4.4nW Lossless Sensor Data Compression Accelerator for 2.9x System Power Reduction in Wireless Body Sensors 1041
Jacob Breiholz (University of Virginia), Farah Yahya (University of Virginia), Christopher J. Lukas (University of Virginia), Xing Chen (University of Michigan), Kevin Leach (University of Virginia), David Wentzloff (University of Michigan), Benton H. Calhoun (University of Virginia)

This paper presents a lossless sensor data compression accelerator for power reduction in wireless body sensors. First, the performance of a low complexity compression algorithm that has previously been demonstrated only on environmental sensor data is assessed for electrocardiogram (ECG) and acceleration data. Second, the algorithm is implemented as a custom hardware accelerator on a health monitoring driven System on Chip (SoC) in a 130nm process. The accelerator is closely integrated with the transmitter interface to minimize its contribution to system power and reduce user overhead. The accelerator adds only 4.4 nW processing overhead and reduces the required transmitter duty cycle by 3.7x, reducing the system power by 2.9x, and allowing the entire system to consume just 2.62 µW when transmitting ECG data at a 360Hz sampling rate.

Integrated Neural Interfaces 1045
Ross M. Walker (University of Utah), Loren Rieth (University of Utah), Subramanian S. Iyer (University of California, Los Angeles), Adeel A. Bajwa (University of California, Los Angeles), Jason Silver (University of Utah), Taufiq Ahmed (University of Utah), Naila Tasneem (University of Utah), Mohit Sharma (University of Utah), A. Tye Gardner (University of Utah)

This manuscript proposes a modular "Chiplet" paradigm of integrated neural interfaces for heterogeneous physical integration of active electronics with neural recording and stimulation devices. The modularity offers flexibility in large-scale neural interface design, the ability to test system components individually before integration, relaxed tolerances for physical integration, and an avenue for sharing and reuse of integrated circuit technology without the need to redesign monolithic ASICs. The Chiplet approach leverages state-of-the-art silicon processing and assembly techniques that were developed in the semiconductor industry to provide an alternative path to system scaling that utilizes smaller chips.

Highly Linear Bridge-Based ISFET pH Sensor Readout Circuit 1049
Mohammadreza Asgari (University of Akron), Kye-shin Lee (University of Akron), Nathan Ida (University of Akron)

A highly linear bridge-based constant voltage and constant current ISFET pH sensor readout circuit is proposed. In this scheme, a compact and low power pH sensor readout circuit is realized by using only one opamp and three MOSFETs without degrading the accuracy. The proposed circuit is implemented using standard CMOS 0.18 µm technology that shows chemical sensitivity of -37mV/pH, power consumption of 450 nW, and occupies a core area of 70 µm × 35 µm. The sensor probe was measured in the range of pH 3 to pH 9 that is required in hydroponics.

Session C1L-B: Special Session: Internet of Things: Sensors to Cybersecurity

Chair: Neeraj Magotra, *WNEU*
Co-Chair: Amer Qouneh, *Western New England University*
Time: Wednesday, August 9, 2017, 9:00 - 10:40
Location: Eaton Hall 201

Study of Secure Boot with a FPGA-Based IoT Device 1053
Yuan Liu (Western New England University), Jed Briones (Western New England University), Ruolin Zhou (Western New England University), Neeraj Magotra (Western New England University)

In this paper, we employ Xilinx Zynq-7000 Series System-on-Chip (SoC) ZC-706 prototype board to design an IoT device. To defend against threats to FPGA design, we have studied Zynq-ZC706 to (1) encrypt FPGA bitstream to protect the IoT device from bitstream decoding; (2) encrypt system boot image to enhance system security; and (3) ensure the FPGA operates correctly as intended via authentication to avoid spoofing and Trojan Horse attacks.

Internet of Things: Solar Array Tracker 1057
Kyle Williams (Western New England University), Amer Qouneh (Western New England University)

Due to economies of scale and advancement in silicon technologies, powerful computing platforms are ushering a new era in computing and connectivity. These platforms are sometimes categorized under the umbrella of Internet of Things (IoT). In this paper, one such platform is used to design and build an Internet of Things solar tracker. The solar tracker predicts the sun position for maximum power output, controls servos that move the cell, monitors the output of the solar cell, collects and processes raw data to produce information that can be sent to a remote station for further analysis. Similar solar trackers can be installed at solar farms to help in energy harvesting and management. Solar trackers send processed information to a centralized location where further analysis provides energy utility companies with fine-grained energy harvesting and management. They help improve the overall efficiency of the system

Understanding ADC in Sensors in IoT and Adjusting PWM Duty Cycle using Potentiometer with EDUX1002G Oscilloscope and Keysight U3800A 1061
Doris Lau (Keysight Technologies)

With the emerging wireless technology, we can see the significance role of IoT in today's technology. Internet of Things is a concept of connecting everything to everywhere at all time. Essential properties of IoT, involves not only from database and gateway communication, but also involves sensor communication. This paper introduces a back to basic approach of understanding analog to digital conversion concept used in analog sensors, with analog digital converter of Keysight U3800A and displaying the output by the pulse width modulation output on Keysight U3800A by using EDUX1002G oscilloscope. This gives students an introduction to analog digital conversion concept used in sensors, by using Keysight IoT development kit, U3800A.

Internet of Things in Computer Engineering Curricula: Just Do It! 1065
Amer Qouneh (Western New England University), Neeraj Magotra (Western New England University)

The overwhelming interest in the Internet of Things (IoT) shown by the industry, academia, and hobbyists alike compel experts to declare that IoT could be the next disrupting technology since the Internet. This new paradigm has taken everyone in the computing field by storm, not because it is an unknown technology, but because of the vast opportunities that it promises to provide, and more importantly, the extent of social change that it is expected to cause. Since there is no consensus on the contents of an IoT curriculum or even a course, we describe our experience in offering an introductory course in IoT at Western New England University.

Energy-Efficient Neural Image Processing for Internet-of-Things Edge Devices 1069
Jong Hwan Ko (Georgia Institute of Technology), Yun Long (Georgia Institute of Technology), Mohammad Faisal Amir (Georgia Institute of Technology), Duckhwan Kim (Georgia Institute of Technology), Jaeha Kung (Georgia Institute of Technology), Taesik Na (Georgia Institute of Technology), Amit Ranjan Trivedi (University of Illinois at Chicago), Saibal Mukhopadhyay (Georgia Institute of Technology)

Enhancing energy/resource efficiency of neural networks is critical to support on-chip neural image processing at Internet-of-Things edge devices. This paper presents recent technology advancements towards energy-efficient neural image processing. 3D integration of image sensor and neural network improves power-efficiency with programmability and scalability. Computation energy of feed-forward and recurrent neural networks is reduced by dynamic control of approximation, and storage demand is reduced by image-based adaptive weight compression. Emerging devices such as tunnel FET and Resistive Random Access Memory are utilized to achieve higher computation efficiency than CMOS-based designs.

Session C1L-C: Photonics and Nanoelectronics

Chair: Vishal Saxena, *University of Idaho*
Time: Wednesday, August 9, 2017, 9:00 - 10:40
Location: Eaton Hall 202

Broad Area, Selective-Emitters for High Temperature Operation 1073
John Chivers (Tufts University), Thomas Vandervelde (Tufts University)

We have developed a high-temperature selective emitter made with alumina and titanium employing a Fabry-Perot cavity design. We additionally explore other material combinations to accommodate a range of frequency regions. Our goal is not only to develop a high performance emitter, but to establish guidelines for selecting materials and fabrication techniques for new device designs.

Current Feedback Neural Amplifier with Real Time Electrode Offset Suppression 1077
Khalid B. Mirza (Imperial College London), Nishanth Kulasekeram (Imperial College London), Christofer Toumazou (Imperial College London)

This paper describes a direct coupled neural amplifier with active electrode offset suppression in order to avoid large coupling capacitors and complex chopper circuits. It describes a novel feedback scheme, where a low pass current mode feedback is applied to a regulated telescopic cascode amplifer, at the cascode nodes by using a modified transconductance block. This solution leads to fully differential input-differential output direct coupled neural amplifier, achieving a DC offset suppression range of $\pm$200 mV, chip area area of 0.078 mm^{2} per channel and an input referred noise of 2.5 μV_{rms} over 1 Hz – 5kHz bandwidth.

On-Device STDP and Synaptic Normalization for Neuromemristive Spiking Neural Network 1081
Nicholas Soures (Rochester Institute of Technology), Lydia Hays (Rochester Institute of Technology), Eric Bohannon (Rochester Institute of Technology), Abdullah M. Zyarah (Rochester Institute of Technology), Dhireesha Kudithipudi (Rochester Institute of Technology)

Spiking Neural Networks offer low precision communication, robustness, and low power consumption and are attractive for autonomous applications. One of the well accepted learning rules for these networks is spike timing dependent plasticity which is governed by the pre- and postsynaptic spike timings. To stabilize the plasticity and avoid saturation in these learning rules, synaptic normalization is used. In this work, we propose the circuit to efficiently realize synaptic normalization in a neuromemristive system and how it improves the plasticity for unsupervised on-device learning. High-level modeling shows the efficacy of synaptic normalization in pattern recognition and feature extraction.

Integrated CMOS Spectrometer for Multi-Dimensional NMR Spectroscopy 1085
Dongwan Ha (Analog Devices, Inc.), Nan Sun (University of Texas at Austin), Jeffrey Paulsen (Schlumberger-Doll Research), Yiqiao Song (Schlumberger-Doll Research), Yiqiao Tang (Schlumberger-Doll Research), Sungjin Hong (Schlumberger-Doll Research), Donhee Ham (Harvard University)

This paper reviews our portable multi-dimensional nuclear magnetic resonance (NMR) spectroscopy system combining a 4-mm2 CMOS NMR spectrometer integrated circuit (IC) and a permanent magnet. The work was first reported in our paper published in 2014 Proceedings of National Academy of Sciences with emphases on overall system development and spectroscopy experimentations. Here we pay more attention to the IC design. The scalability of the integrated spectrometer can enable not only portable NMR spectroscopy in conjunction with small permanent magnets for in-field and online applications, but also parallel NMR spectroscopy for high-throughput applications.

A 40Gb/s PAM4 Optical DAC Silicon Microring Resonator Modulator Transmitter 1089
Ashkan Roshan-Zamir (Texas A&M University), Binhao Wang (Hewlett-Packard Enterprise), Kunzhi Yu (Texas A&M University), Shashank Telaprolu (Texas A&M University), Cheng Li (Hewlett-Packard Enterprise), M. Ashkan Seyedi (Hewlett-Packard Enterprise), Marco Fiorentino (Hewlett-Packard Enterprise), Raymond Beausoleil (Hewlett-Packard Enterprise), Samuel Palermo (Texas A&M University)

PAM4 modulation is currently being implemented in high-speed wireline communication standards in order to increase bandwidth density. This paper presents a transmitter which utilizes a low-area silicon microring resonator modulator with two separate phase shifter segments to realize high-speed PAM4 modulation with an optical DAC approach. The optical DAC is designed with an optimized MSB/LSB segment size ratio of 1.9:1 to generate a uniform four level output with independent MSB/LSB two-level NRZ drivers. Two differential high-swing segmented pulsed-cascode output stages drive the MSB/LSB segments with independent edge-rate and level controls that compensate for output level spacing and eye skew. The hybrid integrated prototype, with the optical DAC microring modulator fabricated in a 130nm silicon photonic process and the transmitter circuitry fabricated in a GP 65nm CMOS process, achieves 40Gb/s operation at 4.38mW/Gb/s when driving each differential terminal of the segmented depletion-mode microring modulator with 4.4Vppd swing.

Session C1L-D: Control Systems

Chair: Matthew Rhudy, *Penn State*
Co-Chair: Xu Chen, *University of Connecticut*
Time: Wednesday, August 9, 2017, 9:00 - 10:40
Location: Eaton Hall 203

2D System based Iterative Learning Control for Linear Singular Discrete-Time Systems 1093
S. Sh. Alaviani (Iowa State University)

In this paper, iterative learning control(ILC) based on two-dimensional(2D) system theory for a linear singular discrete-time system is considered. By applying the singular 2D linear Roesser's discrete model to describe the ILC process of the system, necessary and sufficient conditions for impulse-free convergence of the proposed ILC rules are given. Ultimately, two numerical examples are given to present the results established.

Security Challenges and Solutions for Closed-Loop Artificial Pancreas Systems 1097
Caterina Lazaro (Illinois Institute of Technology), Erdal Oruklu (Illinois Institute of Technology), Ali Cinar (Illinois Institute of Technology)

This work presents security solutions related to multi-sensor closed-loop artificial pancreas (AP) systems. The proposed AP system is built on a heterogeneous platform incorporating a smartphone, activity sensors, a glucose monitor, an insulin pump, a laptop hosting the multi-variable control algorithm and a cloud server. Developing a secure AP system is essential for mass adoption among diabetes patients. However, various communication interfaces and dynamics among the AP components result in multiple security vulnerabilities and intrusion points. We first identify the threats related to both AP data communication and AP data storage. Then, we propose several cryptography and authentication measures to address the threats related to the man-in-the-middle attacks.

Temporally Oversampled CMOS X-Ray Photon Counting Sensor for Low Dose Fluoroscopy 1101
Donald B. Hondongwa (Dartmouth College), Eric R. Fossum (Dartmouth College)

We present the concept of an x-ray quanta image sensor (XQIS) utilizing temporal oversampling and CMOS image sensor technology. The output of the XQIS is a binary bit frame with each bit representing the presence or absence of a detected x-ray photon. The bit frames are read out at very high rate (>1000fps) and a series or bit values are combined to form pixel values using digital frame integration. A system model analyzing the design parameter is presented and the component designs are evaluated in simulation.

Synthesis and Analysis of Fully Differential Filters using Two Port Networks 1105
B.J. Maundy (University of Calgary), A. Elwakil (University of Sharjah), A. Al-Ali (University of Calgary), L. Belostotski (University of Calgary)

In this paper we present a systematic method to synthesize and analyze fully differential input-output filters using two port networks. Transfer functions, input and output impedance can be evaluated for various impedances and transmission matrices varied to investigate the filters performance. Experimental and simulated results in Cadence are provided.

Session C1L-E: Neuromorphic Systems

Chair: Yang Yi, *University of Kansas*
Co-Chair: Yanzhi Wang, *Syracuse University*
Time: Wednesday, August 9, 2017, 9:00 - 10:40
Location: Eaton Hall 206

Leveraging Spintronic Devices for Ultra-Low Power In-Memory Computing: Logic and Neural Network 1109
Deliang Fan (University of Central Florida), Zhezhi He (University of Central Florida), Shaahin Angizi (University of Central Florida)

In this paper, we present that different spintronic devices based memory, including spin-orbit torque magnetic random access memory (SOT-MRAM), magnetic racetrack memory, magnetic skyrmion, could be leveraged to implement an energy efficient in-memory computing platform. Then, we employ SOT-MRAM and racetrack memory to develop an efficient in-memory data encryption engine that could encrypt data within memory. Furthermore, we also show that emerging magnetic skyrmion device could be leveraged to design a tunable skyrmion neuron cluster that approximate non-linear neuron activation function, which is promising to achieve two orders of lower energy consumption compared with CMOS counterparts.

Gate-All-Around FET based 6T SRAM Design using a Device-Circuit Co-Optimization Framework 1113
Luhao Wang (University of Southern California), Alireza Shafaei (University of Southern California), Massoud Pedram (University of Southern California)

Gate-all-around nanowire transistor is deemed as one of the most promising solutions that enables continued CMOS scaling. Compared with FinFET, it further suppresses short-channel effects by providing superior electrostatic control over the channel. Due to the unique device structure, gate-all-around nanowire transistor also allows more efficient layout design by exploiting 3-dimensional stacking configurations. In this paper, we investigate the 6T SRAM cell design for gate-all-around nanowire transistors using a device-circuit co-optimization framework. At the device level, TCAD simulation and current source modeling method are applied to extract the model. Layout designs with horizontal, lateral, vertical stacking device structures are explored. At the circuit level, read and write assist techniques are studied to relieve the negative impact of low on-currents on SRAM stabilities incurred by nanowire channels. Operating at 300 mV, assist techniques can increase the read static noise margin and the write static noise margin of 6T SRAM up to 82% and 92%, respectively.

High Efficient Reconfigurable PUF through Spin Hall-Induced Coupled-Oscillators 1117
Azadeh Famili (California State University, Fullerton), Yoonsuk Choi (California State University, Fullerton), Yu Bai (California State University, Fullerton)

In recent decades, hardware security has played a more and more important role. Among various types of hardware, the Physical Unclonable Function (PUF) has been considered as security primitives to generating keys in order to keep systems safe, authentic, informative, and identified. Recently, leveraging the physics of emerging devices to implement on PUF has long been envisioned. However, current emerging devices based PUF are unreliable due to environmental variations. In this paper, we propose High Efficient Reconfigurable PUF using Spin Hall- Induced Coupled-Oscillators, which embraces and exploits spin oscillation of spintronic devices instead of diminishing or circumventing them. Compared with conventional emerging devices based on PUF, our proposed PUF can generate more delay pairs, can be more reliable to environmental variations, faster, and low power. Comprehensive results demonstrate that the proposed PUF can sufficiently support our conclusion.

Memristor Crossbar-Based Ultra-Efficient Next-Generation Baseband Processors 1121
Geng Yuan (Syracuse University), Caiwen Ding (Syracuse University), Ruizhe Cai (Syracuse University), Xiaolong Ma (Syracuse University), Ziyi Zhao (Syracuse University), Ao Ren (Syracuse University), Bo Yuan (City University of New York), Yanzhi Wang (Syracuse University)

As one of the most promising future fundamental devices, memristor has its unique advantage on implementing low-power high-speed matrix multiplication. Taking advantage of high performance on basic matrix operation and flexibilitys of memristor crossbars, in this paper, we investigate both discrete Fourier transformation (DFT) and miltiple-input and multioutput (MIMO) detection unit in baseband processor. We reformulate the signal processing algorithms and model structures into a matrix-based framework, and present a memristor crossbar based DFT module design and MIMO detector module design. For both designs, experimental results show significant gains in speed and power efficiency compared with traditional CMOS-based designs.

A CMOS Synapse Design Implementing Tunable Asymmetric Spike Timing-Dependent Plasticity 1125
Robert C. Ivans (Boise State University), Kurtis D. Cantley (Boise State University), Justin L. Shumaker (US Army Research Laboratory)

A CMOS synapse design is presented which can perform tunable asymmetric spike timing-dependent learning in asynchronous spiking neural networks. The overall design consists of three primary subcircuit blocks, and the operation of each is described. Pair-based Spike Timing-Dependent Plasticity (STDP) of the entire synapse is then demonstrated through simulation using the Cadence Virtuoso platform. Tuning of the STDP curve learning window and rate of synaptic weight change is possible using various control parameters. With appropriate settings, it is shown the resulting learning rule closely matches that observed in biological systems.

Session C1L-F: RF and THz Systems

Chair: Mona Hella, *Rensselaer Polytechnic Institute*
Time: Wednesday, August 9, 2017, 9:00 - 10:40
Location: Paige Hall - Crane Room

Energy-Efficient Terahertz Electronics using Multi-Functional Electromagnetism and High-Parallelism Architecture 1129
Zhi Hu (Massachusetts Institute of Technology), Cheng Wang (Massachusetts Institute of Technology), Ruonan Han (Massachusetts Institute of Technology)

This paper describes two approaches to increase the energy efficiency of on-chip terahertz (THz) integrated circuits and systems. First, we present designs of multi-functional electromagnetic structures that utilize mode orthogonality and near-field interference to achieve simultaneous oscillation, harmonic generation, signal filtering and radiation. This leads to ultra-compact THz circuits with low passive loss. Our radiator arrays using such approach achieve 0.1mW and 3.3mW of total radiated power at 1.01THz and 0.32THz, respectively, representing the highest radiated power in silicon in their frequency ranges. Next, we also present a highly-parallel architecture for broadband spectral scanning, which breaks the long-standing efficiency-bandwidth tradeoff. Our CMOS spectrometer and its associated dual-frequency-comb gas sensing scheme achieve rapid and seamless coverage of 220 to 320-GHz band with 5.2-mW total radiated power (TX) and a minimum of 14.6-dB noise figure (RX). These approaches, leveraging the high integration capability of silicon circuits, are proved to be highly effective towards energy-efficient THz microsystems for new paradigms of sensing and communications.

Improving the Performance of All-Digital Transmitter based on Parallel Delta-Sigma Modulators through Propagation of State Registers 1133
Daniel C. Dinis (Universidade de Aveiro), Rui F. Cordeiro (Universidade de Aveiro), Arnaldo S.R. Oliveira (Universidade de Aveiro), José Vieira (Universidade de Aveiro), Tomás O. Silva (Universidade de Aveiro)

In this paper it will be shown that propagating specific state registers in a fully parallel Delta-Sigma Architecture can have a profound impact in enhancing the performance of these type of modulators without stringent requirements in terms of latency and resources usage. An FPGA-based transmitter was implemented and designed to validate the proposed architecture, and to demonstrate that flexible, high-speed and wideband modulators can be implemented with low-complexity and with a low resources usage.

A Robust Calibration and Supervised Machine Learning Reliability Framework for Digitally-Assisted Self-Healing RFICs 1138
Eric J. Wyers (Tarleton State University), Weiyi Qi (North Carolina State University), Paul D. Franzon (North Carolina State University)

A robust calibration and supervised machine learning reliability framework has been developed to aid the circuit designer in the design and implementation of reliable digitally-reconfigurable self-healing RFICs. For calibration algorithm performance and reliability validation, we advocate the use of surrogate modeling, a supervised machine learning technique, which offers a significant reduction in the required computational complexity relative to relying solely on the execution of expensive circuit simulations. A RF phase rotator test case is used to show the robustness and utility of the developed self-healing reliability framework.

Quadrature-Modulation Envelope-Pulse-Width-Modulation Transmission System using Quadrature Polarized Waves 1142
Ryo Sakai (Tokyo University of Science), Tomoaki Morita (Tokyo University of Science), Yohtaro Umeda (Tokyo University of Science), Yusuke Kozawa (Ibaraki University)

This paper presents quantitative evaluation of power efficiency decrease by not satisfying the zero current switching (ZCS) condition occurring in a bi-level quadrature-modulation (QM) envelope-pulse-width-modulation (EPWM) transmitter. The power efficiency is evaluated by changing Q factor of the series resonance circuit inserted in power amplifier (PA). As a result, the power efficiency decreases as the Q factor increases. In addition, QM EPWM transmission system using quadrature polarized waves is proposed to satisfy ZCS condition for high efficiency. Simulation shows that the proposed transmission system can demodulate both sigma and delta component and improve power efficiency of the PAs.

Theoretical Bounds on Time-Domain Resolution of Multilevel Carrier-Based Digital PWM Signals used in All-Digital Transmitters 1146
Omer Tanovic (Mitsubishi Electric Research Laboratories / Massachusetts Institute of Technology), Rui Ma (Mitsubishi Electric Research Laboratories), Koon Hoo Teo (Mitsubishi Electric Research Laboratories)

Pulse-width modulation (PWM) has been extensively used in switched converter systems, and recently in RF applications, due to an increased interest in all-digital transmitters. These architectures employ high efficiency switched-mode power amplifiers (SMPA), where PWM is commonly used to generate the PA driving signal. However, digitally implemented PWM introduces large amount of in-band distortion, which is traditionally explained by spectral aliasing. In this paper we derive a novel closed-form time-domain expression for the output signal of a multilevel carrier-based digital PWM, driven by an arbitrary bounded input signal. We show that the spectral aliasing effects are equivalent to amplitude quantization of the PWM input signal, and give theoretical bounds on the output signal resolution for a given PWM scheme. Parameters of this quantization process are determined, and their dependence on PWM design specifications is shown. Numerical simulations in MATLAB were used to verify derived analytical expressions.

Session C1L-G: Technologies for Smart Sensors

Chair: Fred Beyette, *University of Cincinnati*
Co-Chair: Stefano Gregori, *University of Guelph*
Time: Wednesday, August 9, 2017, 9:00 - 10:40
Location: Paige Hall - Terrace Room

Applications of Sensing Technology for Smart Cities 1150
Samira Shamsir (University of Tennessee), Ifana Mahbub (University of Tennessee), Syed K. Islam (University of Tennessee), Arifur Rahman (George Washington University)

The industrial revolution and rapid urbanization of human society have put a great strain on the resource consumption and environmental issues. The concept of a smart city with advanced technology can play a vital role to overcome these challenges and make life more sustainable and environment greener. Sensing technology has an intense impact in this regard starting from smart design of the infrastructure to autonomous control and monitoring of the overall system. This paper presents an overview of the state-of-the-art sensor technologies that can play a vital role in the design of a smart city. Although sensing technology can be implemented for a huge number of aspects, this paper is aimed to provide a brief review of sensing technology on some selected platforms such as environmental monitoring, agriculture, and food safety as well as in security. By discussing the emergence of the low-power smart sensor and the associated challenges, this paper attempts to provide a future research direction.

A Trapezoid CMOS Image Sensor with 2% Detection Accuracy for Traffic Monitoring 1154
Bingxing Wu (University of Idaho), Ahmed Abdel-Rahim (University of Idaho), Suat U. Ay (University of Idaho)

In this paper, a new multi-resolution CMOS imager sensor with trapezoid pixel array, called TZOID, is presented. It is particularly designed for traffic monitoring to detect the speed and location of upcoming vehicles, with 55 times less pixels than the rectangular pixel array designed imager that function as TZOID. The unique trapezoid sensor design also eliminates computationally expensive coordinate mapping to extract necessary information. The TZOID design simplifies the traffic monitoring camera system achieving lower communication bandwidth, low-power consumption and smaller frame memory. A prototype TZOID chip was fabricated in a 0.18µm CMOS process with a 40x152 multi-resolution trapezoid pixel array. ±2% accuracy of location, length and speed detection is achieved in laboratory tests.

Smart City Sensing and Communication Sub-Infrastructure 1159
M. Habibzadeh (State University of New York at Albany), W. Xiong (State University of New York at Albany), M. Zheleva (State University of New York at Albany), E.K. Stern (State University of New York at Albany), B.H. Nussbaum (State University of New York at Albany), T. Soyata (State University of New York at Albany)

In this paper, we conceptualize the deployment of smart city sensing nodes, which we term Smart Boxes, in a part of the city with no energy and communication infrastructure. We envision our proposed smart boxes incorporating a multi-source energy harvester, which allows them to act as an emergency cell phone network. To improve scalability, we use a Software Defined Radio (SDR) within the box. The contribution of this paper is to provide a proof-of-concept experimental demonstration of Smart Box LTE capabilities. Our experiments show that the box can serve three cellular users when powered by a 50—100 W energy harvester.

Energy Consumption in Long-Range Linear Wireless Sensor Networks using LoRaWan and ZigBee 1163
Abdullah Kurtoglu (University of Akron), Joan Carletta (University of Akron), Kye-Shin Lee (University of Akron)

This paper compares the energy consumption used for communication in the special case of a wireless sensor network that is deployed linearly over a long distance to monitor an asset such as power lines or pipelines. A model for energy consumption is developed based on a suitable network architecture for a linear wireless sensor network (WSN). Using the model, the energy consumption of networks based on two popular wireless communication protocols, LoRaWan and Zigbee, has been compared. The results show LoRaWan has significantly better energy efficiency than ZigBee for a linear WSN.

Physiological Health Assessment and Hazard Monitoring Patch for Firefighters 1168
Matthew T. Giovanetti (University of Cincinnati), Fred R. Beyette Jr. (University of Cincinnati)

The objective of this project is to create a novel device to monitor and report back with comprehensive physiological status and alerts of hazards encountered by the firefighter. The device would monitor the firefighter's physiological health including heart rate and blood oxygen level, carboxyhemoglobin, and hyperthermia. Not only will the device monitor the firefighter's physiological health, it will also monitor and report back on the temperature and humidity inside the firefighter's suit, and monitor for impacts, falls, impact from objects or contact with objects.

Session C2P-H: Converter Circuit Techniques II

Chair: Sadegh Jalali, *Rambus*
Time: Wednesday, August 9, 2017, 10:40 - 12:00
Location: Ballou Hall - Coolidge Room

Analysis and Compensation Technique Canceling Non-Linear Switch and Package Impedance Effects of a 3.2 GS/s TX-DAC 1172
Hossein Ghafarian (Technische Universität Berlin), Friedel Gerfers (Technische Universität Berlin)

This paper presents a static non-linearity correction technique applied on a 10-bit source series terminated digital-to-analog converter. The proposed technique proves for the first time, an undesired power supply and package resistance can be turned into a benefit by canceling non-linearity effects introduced by the MOSFET switches within the SST DAC cell. The presented analytical model proves the linearization effect of the supply resistance counteracting the nonlinear switch on-resistance, thanks to its degeneration effect. The obtained results from mathematical model were verified by circuit simulations confirming the linearisation potential of the supply resistance to improve the overall DAC integral non-linearity.

Practical Linear and Quadratic Gradient Errors Suppression Techniques in String DACs 1176
Nanqi Liu (Iowa State University), Chris Lash (Texas Instruments Inc.), Jim Todsen (Texas Instruments Inc.), Degang Chen (Iowa State University)

Gradient errors in device arrays cause mismatch between device parameters, which in turn degrade linearity performance of data converters realized with these arrays. A practical "outputs averaging" technique for string DACs is presented to release complex routing problems in gradient reduction patterns. An N-bit string is divided into multiple substrings and the substrings' outputs are averaged to reduce gradient errors induced nonlinearity. A novel layout methodology, called "periodic INL shift", is further developed to suppress quadratic gradient errors. Based on these two techniques, a practical structure with linear gradient cancellation and quadratic gradient reduction is proposed. MATLAB simulations are performed in an 8-bit string DAC and significant improvements on linearity performance are obtained.

A Compact 14-Bit 110 KS/s Two-Stage Incremental ΣΔ ADC for CMOS Image Sensors 1180
Francesco Giorgio (University of Oxford), Bhaskar Choubey (University of Oxford)

This paper presents a compact 14-bit two-stage Incremental-ΣΔ column-parallel ADC for use in CMOS Image Sensors. The ADC as well as a test array for a pixel matrix has been fabricated in a 110nm optical CMOS process with a 3.3V supply. The first ADC stage is 5 bit Incremental-ΣΔ, while the second stage is realized by reusing all circuit elements in a cyclic ADC configuration. This way the ADC column occupies an area of only 0.0029 mm2 and is layout with a fine pitch of 9.6 µm. At a speed of 110 KS/s it consumes 123 µW and achieves a DNL and INL of +0.65/-0.83 LSB and +0.9/-0.81 LSB respectively.

A 200MSPS Time-Interleaved 12-Bit ADC System with Digital Calibration 1184
Aditya Bommireddipalli (Texas A&M University), Dadian Zhou (Texas A&M University), Claudio Talarico (Gonzaga University), Jose Silva-Martinez (Texas A&M University), Aydin I. Karsilayan (Texas A&M University)

This paper proposes a time interleaved ADC architecture employing a digital background calibration technique based on evolutionary computation. The algorithm iteratively minimizes an error function (EF) which models the gain, offset and timing mismatches between the ADC channels. The system was implemented using off-the-shelf Analog to Digital Converters (ADCs) and a Field Programmable Gate Array (FPGA). Experimental results demonstrate that the proposed calibration technique allows an SNDR improvement of 26dB for just 32 iterations of calibration.

Session C2P-J: High Performance VLSI Circuits

Chair: Mark Hempstead, *Tufts University*
Co-Chair: Jose Delgado-Frias, *Washington State University*
Time: Wednesday, August 9, 2017, 10:40 - 12:00
Location: Ballou Hall - Coolidge Room

Energy-Efficient and High Performance 2-Phase Asynchronous Micropipelines 1188
Van Toan Nguyen (Hallym University), Minh Tung Dam (Hallym University), Jeong-Gun Lee (Hallym University)

Pipeline is a widely used circuit structure for high performance digital system designs. This paper presents designs of an energy-efficient and high performance 2-phase asynchronous micropipeline utilizing a one-shot pulse generator in its handshake controller, and its variant with more relaxation in timing constraints. The cycle time and energy consumption of the micropipelines are analyzed and assessed by HSPICE simulations. The simulations are carried out by using 90nm CMOS technology taken from a Predictive Technology Model (PTM). The simulation results show that our 2-phase bundled data protocols can achieve higher energy efficiency and higher performance than those of the micropipeline in [6].

A Comparison of Quasi-Delay-Insensitive Asynchronous Adder Designs Corresponding to Return-to-Zero and Return-to-One Handshaking 1192
P. Balasubramanian (Nanyang Technological University), C. Dang (Nanyang Technological University)

This paper makes a comparison between various quasi-delay-insensitive (QDI) asynchronous ripple carry adders (RCAs) realized using a delay-insensitive dual-rail code which correspond to 4-phase return-to-zero (RTZ) and 4-phase return-to-one (RTO) handshaking. The QDI RCAs considered are 32-bits in size and correspond to a variety of timing regimes viz. strong-indication, weak-indication, early output, and relative-timed, which are implemented using a 32/28nm CMOS process. The extensive comparisons show that, overall, QDI RCAs which correspond to the RTO protocol are optimized compared to their QDI RCA counterparts which correspond to the RTZ protocol in terms of area, power dissipation, latency, and cycle time.

Approximate Quasi-Delay-Insensitive Asynchronous Adders: Design and Analysis 1196
P. Balasubramanian (Nanyang Technological University), C. Dang (Nanyang Technological University), D.L. Maskell (Nanyang Technological University)

Approximate computing is gaining increasing interest among the VLSI design community due to its potential for enabling low power, high speed, and less area while delivering acceptably correct computation results for many digital signal processing applications. In this context, this paper considers for the first time asynchronous quasi-delay-insensitive (QDI) realizations of approximate adders which are compared with some existing accurate asynchronous QDI adders based on a 32/28nm CMOS technology. The simulation results and analysis show that approximate asynchronous computing is preferable over accurate asynchronous computing when the accuracy may be traded-off to achieve optimizations in the design metrics.

Time-Efficient and TSV-Aware 3D Gated Clock Tree Synthesis based on Self-Tuning Spectral Clustering 1200
Fan Yang (Waseda University), Minghao Lin (Waseda University), Heming Sun (Waseda University), Shinji Kimura (Waseda University)

3D gated clock tree synthesis (CTS) mainly consists of three steps: 1) abstract clock topology generation; 2) layer embedding for minimal TSV allocation and 3) clock tree routing with gate and buffer insertion. In this paper, a self-tuning spectral clustering based nearest-neighbor selection (SSC-NNS) algorithm with parallel structure is proposed to achieve high time efficiency in clock tree topology generation, with reduced runtime. In addition, a postorder traversal based layer embedding (PTLE) strategy is adopted for determining the embedding layer of internal nodes with minimal TSV usages. Experimental results show that the proposed method achieves 32\% and 82\% runtime reduction on ISPD2009 and IBM benchmarks respectively compared with the state-of-the-art 3D work. Besides, the TSV count is also reduced by 46\% on ISPD2009 benchmarks.

Session C2P-K: Analog and Mixed-Signal Circuits IV

Chair: Glenn Cowan, *Concordia University*
Co-Chair: Hashem Zare-Hoseini, *Huawei Technologies*
Time: Wednesday, August 9, 2017, 10:40 - 12:00
Location: Ballou Hall - Coolidge Room

Design of a Low-Complexity Wideband Analog True-Time-Delay 5-Beam Array in 65nm CMOS 1204
Arjuna Madanayake (University of Akron), Viduneth Ariyarathna (University of Akron), Nilan Udayanga (University of Akron), Leonid Belostotski (University of Calgary), Sirani K. Perera (Embry-Riddle Aeronautical University), Renato J. Cintra (Universidade Federal de Pernambuco)

Non-squinting wideband analog multi-beamformer is proposed using true time delay (TTD) element delay Vandermonde matrix (DVM). Efficient realization of the DVM is achieved by sparse factorization, which leads to low-complexity hardware implementations (i.e. less number of delay blocks). It is shown that the proposed approach saves 36 TTD elements in a 5-beam multi-beamformer (4-beams corresponding to the 4-point DVM plus the direct sum beam) giving rise to a 60% reduction of hardware in the design compared to the direct implementation. Proposed low-complexity 5-beam multi-beamformer uses all-pass filters as the delay element and measured S-parameters from a fabricated 65 nm CMOS all-pass filter is used to compute the array patterns of the proposed design in the 1.6 - 2.4 GHz range.

The Effect of Source Resistance on the Linearity of Nauta Structure OTA 1208
Long Pham (University of New South Wales), Astria Nur Irfansyah (University of New South Wales), Tara Julia Hamilton (Western Sydney University), Torsten Lehmann (University of New South Wales)

Nauta structure is one of advanced cores designed for high gain, large bandwidth amplifiers. For this reason, the structure was chosen to implement basic core amplifiers in many applications such as pipeline ADC, sigma-delta ADC and high quality filters. Therefore, it is a crucial task to do research about methods to improve the electrical characteristics of Nauta structure. In this paper, we propose a method to calibrate the resistance in the source terminal of self-coupled inverters so that it improves the linearity as well as the output voltage swing of a Nauta structure op-amp.

A Random Number Generation Method based on Discrete Time Chaotic Maps 1212
Osman Boyacı (Istanbul Technical University), Ahmet Cüneyd Tantuğ (Istanbul Technical University)

In this paper a random number generation method based on a piecewise linear one dimensional (PL1D) discrete time chaotic maps is proposed for applications in cryptography and steganography. Appropriate parameters are determined by examining the distribution of underlying chaotic signal and random number generator (RNG) is numerically verified by four fundamental statistical test of FIPS 140-2. Proposed design is practically realized on the field programmable analog and digital arrays (FPAA-FPGA). Finally it is experimentally verified that the presented RNG fulfills the NIST 800-22 randomness test without post processing.

A Time Multiplexed Network Architecture for Large-Scale Neuromorphic Computing 1216
Rezwan A. Rasul (University of Southern California), Pedram Teimouri (University of Southern California), Mike Shuo-Wei Chen (University of Southern California)

Large scale neuromorphic implementation presents challenge in communication between neurons due to large number of interconnects, leading to high energy consumption, processing time and physical wires. We propose a communication protocol based on time-division multiplexed method using just a single wire to minimize the cost of interconnect, and processing time. Both analytical and numerical results show that compared with the commonly used AER approach, the proposed technique leads to 40% lower energy consumption in interconnects and ~4 times processing time reduction for digit classification using MNIST dataset for a network of 1,024 neurons with a toggling factor of ~40%.

High Bandwidth Class-AB Amplifier with High Slew Rate and Fast Current Sensing for Envelope Tracking Applications 1220
Punith R. Surkanti (New Mexico State University), Aditya A. Patil (New Mexico State University), Sri Harsh Pakala (New Mexico State University), Paul M. Furth (New Mexico State University)

This work presents the design of a linear amplifier with a class-AB output stage specifically for envelope tracking(ET) applications. ET has become prevalent for improving power amplifier (PA) efficiency in low-power portable devices. The class-AB amplifier consists of a novel current-sense block for accurately sensing the currents in the push-pull output stage. The design is implemented in a 0.5-µm CMOS process and operates with a 5 V supply, 33 mA quiescent current and 79 MHz UGF at 4Ω load. It can drive load which vary from 4 to 20Ω with an RMS error of -33 dB using a 10 MHz envelope signal.

Design Techniques for In-Field Memristor Forming Circuits 1224
Sherif Amer (University of Tennessee), Garrett S. Rose (University of Tennessee), Karsten Beckmann (State University of New York Polytechnic Institute), Nathaniel C. Cady (State University of New York Polytechnic Institute)

This work presents circuit design techniques for in-field forming of metal-oxide memristor-based systems. The integration of a forming circuit in a memristor-based application hasn't been thoroughly studied. Two challenges exist for in-field forming which are the high forming voltages required and SPICE level modeling of the forming process. Both challenges are addressed in this work and circuit level solutions are provided. A method for incorporating forming in memristor models is proposed. Also, a circuit design is presented for proper isolation of peripheral circuitry during forming to avoid any malfunction

Session C2P-L: Digital Circuits and Systems III

Chair: Mark Hempstead, *Tufts University*
Time: Wednesday, August 9, 2017, 10:40 - 12:00
Location: Ballou Hall - Coolidge Room

A CODEC, Tiles to NoC Router Interface, for Next Generation FPGAs with Embedded NoCs 1228
Alaa Salaheldin (Cairo University), Hassan Mostafa (Cairo University), Ahmed M. Soliman (Cairo University)

Nowadays, SoC uses Network on Chip (NoC) to connect its increasing number of building blocks, in order to overcome the problems of conventional interconnects like large area, high power consumption and large delay. FPGAs, like SoCs, can use NoC to connect its increasing number of tiles, memories, DSP slices and embedded processors. One drawback of using NoC is that increasing its router ports will affect the area, power and frequency of the system significantly. For FPGAs to benefit from the NoC approach we have to find a solution to how to interface with large number of blocks without increasing the NoC router ports. In this paper we use a concentrator module or a Codec to connect between routers and FPGA basic building block (which is a Tile). Using this codec will reduce the effect of increasing tiles count on the area, power and frequency of the routing network of an FPGA. A 64-tiles network with codec would consume less than 15% area, less than 50% power consumption of a NoC-only network and operates with 2.5X frequency.

A High-Performance FPGA-Based LDPC Decoder for Solid-State Drives 1232
Yanhuan Liu (Tsinghua University), Chun Zhang (Tsinghua University), Pengcheng Song (Tsinghua University), Hanjun Jiang (Tsinghua University)

In order to improve the throughput of error correction decoding for high-performance SSDs, a semi-parallel LDPC decoding architecture is proposed in this research. The circuit of the LDPC decoder which can be dynamically configured with bit rate and code length is implemented using the scheduling control flow mode of single instruction multiple data instruction. The adaptive normalization factor is applied to achieve an average improvement of 35% in throughput with SNR of 6.08dB. The LDPC decoder is implemented on the Xilinx VC709 FPGA. With a rate-0.94 length-35840 quasi-cyclic LDPC code, the decoder achieves a throughput of 1.97 Gb/s.

A High Performance Multi-Port SRAM for Low Voltage Shared Memory Systems in 32 nm CMOS 1236
Samira Ataei (Oklahoma State University), Matthew Gaalswyk (Oklahoma State University), James E. Stine (Oklahoma State University)

A 4 kb fully differential 8-port SRAM bitcell array (6 read ports and 2 write ports) is presented in this paper. This 8-port SRAM provides simultaneous access, high system throughput and a great read static noise margin by isolating the read ports from storage nodes. At 0.4 V supply voltage, designed 8-port SRAM bitcell shows 123, 137 and 123 mV static noise margin during read, write and standby modes, respectively. 4 kb 8-port SRAM array is evaluated for leakage and dynamic power consumption, and also read and write access time in 32 nm SOI CMOS technology. It operates at 250MHz with a 0.4 V supply voltage and above 4 GHz with a 0.9 V supply voltage.

Bi-Directional Input/Output Circuits with Integrated Level Shifters for Near-Threshold Computing 1240
Md Shazzad Hossain (Drexel University), Ioannis Savidis (Drexel University)

Interfacing techniques for near-threshold computing are described in this paper. A bi-directional input/output circuit with integrated level shifters is proposed for multiple near-threshold power domains. The circuit provides conversion ranges of 0.38 V to 1.2 V and 0.45 V to 3.3 V depending on the targeted output voltage. Eight different configurations of I/O circuits are evaluated with level shifters implemented with a standard current mirror, cross coupled, and a proposed single ended topology. The use of a single ended level shifter provides the optimum power-delay point.

Margin Aware Timing Test and Tuning Algorithm for Post-Silicon Skew Tuning 1244
Mineo Kaneko (Japan Advanced Institute of Science and Technology)

Post-Silicon clock-Skew Tuning (PSST) is a promising technology for improving performance-yield of VLSIs under process variations. On the other hand, due to run-time timing variations induced by temperature variation, power supply noise, etc, the resultant circuit after clock-skew tuning should be also robust against run-time variations. In this paper, the timing margin in the context of PSST is introduced in terms of control values for programmable delay elements (PDEs), and setup/hold timing test considering timing margin, which is named ``mu-margin timing test'', and an efficient way of its application are discussed. After that, a PDE tuning algorithm which includes mu-margin timing test as a core routine is proposed. Experimental results show us the robustness of a circuit tuned by our algorithm against run-time delay variations as well as the efficiency of our tuning algorithm in tuning cost.

Session C2P-M: Hardware Security

Chair: Massi Corba, *Draper Laboratory*
Time: Wednesday, August 9, 2017, 10:40 - 12:00
Location: Ballou Hall - Coolidge Room

Optical Physical Unclonable Function 1248
Michael Geis (Massachusetts Institute of Technology), Karen Gettings (Massachusetts Institute of Technology), Michael Vai (Massachusetts Institute of Technology)

Many military and commercial systems require a unique digital identification for authentication, key derivation, and other purposes. Our approach uses an optical physical unclonable function (PUF) that can be implemented on printed circuit boards (PCB). Various environmental factors, such as physical stress, temperature, heat dissipation, and aging, affect the effectiveness of such a PUF. This paper will discuss our recent research in addressing these and other concerns by advancing in the areas of waveguide construction, system longevity, and PCB cooling. We will also discuss the enhanced capability of differentiating between intact and disturbed systems.

Using On-Chip Cryptographic Units for Security in Wireless Sensor Networks 1252
Janhavi Kulkarni (Eduvance), Karan Nair (Eduvance), Aditya Pappu (Eduvance), Sarthak Gadre (Eduvance), Ganesh Gore (Eduvance), Jonathan Joshi (Eduvance)

A method is proposed to continue using simple radio transreceiver for communication while ensuring that the information contained therein is sufficiently secure, without increasing processing time significantly. We have used an off-the-shelf SoC (NXP MK64Fx series) with an on-chip memory mapped cryptographic unit as a test platform. Our results demonstrate that without any loss in security parameters like key space and adversary's advantage, we are still able to achieve a low cost and low complexity solution. We have shown that the core protocol stacks of simple radio transceivers can be made secure without significantly increasing processing time in the system. Such an approach provides greater flexibility in controlling the security parameters while allowing for greater optimization of the system.

Template Attacks based on Static Power Analysis of Block Ciphers in 45-nm CMOS Environment 1256
Jiming Xu (Memorial University of Newfoundland), Howard M. Heys (Memorial University of Newfoundland)

Side-channel attacks are proven to be an efficient tool in attacking cryptographic devices. Dynamic power leakage has been used as a source for many well-known side-channel attack algorithms. As process technology size shrinks, the relative amount of static power consumption increases accordingly, and reaches a significant level in sub-100-nm chips, potentially changing the nature of side-channel analysis. In this paper we propose a type of template attack developed for static power analysis of block ciphers. In addition to the original template distinguisher, the attack is shown to work well using new distinguishers which are faster to compute.

DRNG: DRAM-Based Random Number Generation using its Startup Value Behavior 1260
Charles Eckert (Binghamton University), Fatemeh Tehranipoor (University of Connecticut), John A. Chandy (University of Connecticut)

Looking at the potential for DRAM to be used a both a Physically Unclonable Function and to generate random keys. We investigated randomness and stability of the DRAM startup values.

Secure Communication over CANBus 1264
Ali Shuja Siddiqui (University of North Carolina at Charlotte), Yutian Gui (University of North Carolina at Charlotte), Jim Plusquellic (University of New Mexico), Fareena Saqib (University of North Carolina at Charlotte)

In this paper, we propose hardware based secure and trusted communication over CAN bus in the intra vehicle network connecting electronic Control Units (ECUs). CAN bus is an insecure communication channel, connecting resource constraint devices that have limited resources to devote for data security and real-time requirements to meet the safety critical design specifications. In this paper, we propose a secure and trusted framework that implements lightweight hardware based authentication and secure encryption for enhanced security over the insecure communication channel. Physical unclonable functions provides a temper evident mechanism to detect invasive or ECU exchanges by adversary at the untrusted field, and the Elliptic Curve Cryptography based mutual authentication provides a privacy preserving secure mechanism without sharing the secret bitstrings. The paper details the framework along with the resource overhead and performance analysis of the proposed system.

Session C2P-N: Sensor Technology

Chair: Kye-Shin Lee, *University of Akron*
Co-Chair: Gymama Slaughter, *University of Maryland, Baltimore County*
Time: Wednesday, August 9, 2017, 10:40 - 12:00
Location: Ballou Hall - Coolidge Room

Tactile Array Sensor for Manipulator based on the Barometric Chips 1268
Chaoxiang Yang (Tsinghua University), Chun Zhang (Tsinghua University), Wenao Xie (Tsinghua University), Hanjun Jiang (Tsinghua University), Zhihua Wang (Tsinghua University)

This article presents a new method of using barometric chips to make tactile array sensor for manipulator. The barometric chip can detect and convert analog air pressure to digital signal and calculate the value of surface air pressure. First we design appropriate circuits with the PCB technology and mount the chips on the board, then we manufacture a silica gel air cell on each chip. In the way, the load stress applied on the silica gel surface can be converted to air pressure through the air cells. Using a force gauge we succeed determining the specific relationship of the air pressure versus the load stress. The result shows a high linearity with the R2 coefficient is 0.9951. The sensor chip has a small size (2.5 x 2.5 x 1.0 mm), low power consumption (4μA), high sample rates (40Hz) and is inexpensive(US$ 2.06 per chip). Besides, it can detect the temperature directly. The elastic silica gel also acts as a robust and compliant contact surface and protection. This method can enable progress for tactile sensors in applying to the cognitive robotic manipulator and various fields where the tactile information is valuable.

A Current and Vibration based Detection System for Lightning Strikes on Transmission Towers 1272
Taohid Latif (University of Akron), Nathan Ida (University of Akron), Kye-Shin Lee (University of Akron), Joan Carletta (University of Akron)

The current work proposes a method and circuitry for a lightning strike detection system with current and vibration detecting features. A Rogowski coil is used for current detection, which can be placed around a conductor where the lightning current is expected to flow. The method also provides means of ascertaining which tower is closest during the moment of the strike through use of a dual-axis accelerometer by making use of the vibration at the moment of the strike and correlating that with the current detected. A small scale prototype was built that performed adequately and was in line with the theoretical and simulation results.

Low Power Embedded System for Pre-Fall Detection Application 1276
Neeraj Rathi (Indiana University Purdue University Indianapolis), Ashok Kumar Thella (Indiana University Purdue University Indianapolis), Monika Kakani (Indiana University Purdue University Indianapolis), Maher Rizkalla (Indiana University Purdue University Indianapolis)

Developed a smart wearable device which detects human fall before it occurs and therefore prevents the subject from serious injuries.

Smart Cage for 3D Tracking of Position and Orientation of Magnetically Marked Device 1280
Andrew M. Bourhis (Tufts University), Eric L. Miller (Tufts University), Sameer R. Sonkusale (Tufts University)

This paper presents a smart cage platform using magnetic sensors for 3D tracking of the location and orientation of a magnetically marked capsule (MMC) for targeted drug delivery. For this study, a small permanent magnet is placed inside a capsule to be tracked. A smart cage is developed using eight 3-axis magnetometers that tracks the location and orientation of the capsule using a magnetic source imaging (MSI) algorithm. The capsule location was estimated within 2-3 mm in XY and 6 mm in the Z direction. The results presented here demonstrate that this noninvasive tracking system holds great promise for monitoring the transit of any device (such as a smart pill) that is magnetically marked.

First Results from a Time Domain Impedance Probe for Measuring Plasma Properties in the Ionosphere 1284
Edmund Spencer (University of South Alabama), David Clark (University of South Alabama), Samuel Russ (University of South Alabama), Ravi Gollapalli (University of South Alabama), Dimitris Vassiliadis (West Virginia University), Brannon Kerrigan (Virginia Polytechnic Institute and State University), John Mullins (University of South Alabama), Jeffrey Mizell (University of South Alabama)

A new Time Domain Impedance Probe (TDIP) is presented in this paper. The new instrument is able to make measurements of absolute electron density and electron neutral collision frequency in the ionosphere at temporal and spatial resolutions not previously attained. A prototype of this instrument was integrated into the payload of a NASA USIP sounding rocket launched out of Wallops Island on March 1 2016. Here we describe the instrument, and present some time domain data obtained from the sounding rocket experiment.

Session C3L-A: Linear Analog Systems

Chair: Juan Montiel-Nelson, *University of Las Palmas de Gran Canaria*
Co-Chair: Peter Levine, *University of Waterloo*
Time: Wednesday, August 9, 2017, 12:00 - 13:40
Location: Braker Hall 001

Novel Band-Pass ΔΣ Modulators based on a Modified Adder-Less Feed-Forward Structure 1288
Mohammad Honarparvar (Polytechnique Montreal), José M. de la Rosa (CSIC), Frederic Nabki (École de Technologie Supérieure), Mohamad Sawan (Polytechnique Montreal)

Two Band-Pass (BP) Discrete Time (DT) Delta-Sigma (DS) modulators are proposed in this paper. In both cases, the drawback of high-speed power-hungry adder is tackled by proposing a modified unity signal transfer function (STF) adder-less feed- forward structure. The first proposed BP DT DS modulator is a conventional adder-less multi-stage noise shaping (MASH) DS modulator, while the noise leakage problem, caused by the mismatches between analog loop filter and digital cancellation logic (DCL), is mitigated by proposing a second topology in which the DCL is omitted. All of these features make the proposed modulators suitable for low-voltage and low-power applications, while the second proposed topology features a higher robustness against noise leakage and mismatch. Time-domain behavioral simulations show a 0-dBFS overload input level for the proposed architectures while the DC-gain is relaxed for the second proposed architecture such that a 67-dB SNDR can be obtained with only a 30-dB amplifier DC-gain at a -20-dBFS input signal level.

Design of a Wireless and Batteryless Heart Rate Monitor 1292
J. Sosa (Universidad de Las Palmas de Gran Canaria), H. Solar (Centro de Estudios e Investigaciones Técnicas / University of Navarra)

This paper presents the design of a wireless and batteryless heart rate monitor. The measurement is done using a single–lead ECG raw signal. The design is based on a commercial ultra low power microcontroller, an optimized full–custom RF Front–End, a ultra low power Threshold Comparator and a Programmable Gain Amplifier implemented in commercial 90 nm CMOS. The communications are compliant with the ISO 11784/11785 HDX standard. The complete design consumes only 15 μW and the heart rate measurement is done in only 3.2 seconds. A comparison with the best literature approach demonstrate that presented design is a 45% more efficient in terms of energy.

A Time-Mode LDI-Based Resonator for a Band-Pass ΔΣ TDC 1296
Soheyl Ziabakhsh (Université Du Québec), Ghyslain Gagnon (Université Du Québec), Gordon W. Roberts (McGill University)

In this paper, a time-mode resonator is presented that is used to realize a second-order bandpass delta-sigma time-to-digital converter (TDC). The resonator is constructed as a cascade of two lossless discrete-time integrators implemented using time-latches and some digital logic in a negative feedback configuration. This paper presents for the very first time the means in which time-mode circuits are used in a negative feedback loop. This achieves high-speed time-mode signal processing without the limitations imposed by switched-capacitor (SC) circuit techniques such as the matching of capacitors to realize precise signal gains. Instead, circuit precision is realized using an on-chip calibration circuit referenced to the main system clock to adjust for timing variations in the time-mode circuits. The operation of the time-mode resonator is verified by realizing a second-order BP delta-sigma TDC. The bandpass noise-shaping is validated with transistor-level simulations.

Split-Transistor Compensation: Application to a Low-Dropout Voltage Regulator (LDO) 1300
Venkat Harish Nammi (New Mexico State University), Nitya R. Thota (New Mexico State University), Paul M. Furth (New Mexico State University), Wei Tang (New Mexico State University)

A controlled comparison of three compensation techniques – nested Miller compensation (NMC), Split-Length compensation (SLC) and the new Split-Transistor compensation (STC) – is performed in a multi-stage low-dropout voltage regulator (LDO). The LDO with STC used 41% and 84% lower total compensation capacitance compared to the LDOs with SLC and NMC, respectively. To verify the proposed compensation technique, a micro-power LDO using STC has been fabricated in a 0.5-um CMOS process. Experimental results show an undershoot of 126 mV for a 1 uA – 50 mA load step and an overshoot of 556 mV for a 50 mA – 1 uA load step. At a total quiescent current of less than 5 uA, the fabricated micro-power LDO with STC finds application in IoT devices.

Reference Circuits for Emerging Applications – From Extreme Environment Electronics to Internet of Things ... 1304
Laleh Najafizadeh (Rutgers University)

Almost all electronic circuits require a reference, be it voltage, current, or time. A well-designed reference is expected to provide a ``stable'' point that will be independent of the potential variations in its operating conditions. While there has been decades of extensive amount of creative work in the world of reference design, with the emergence of new applications, reference designers are now faced with new problems and design challenges. In this review paper, we focus on two emerging application domains, namely, extreme environment (EE) electronics and the internet of things (IoT). We briefly describe design challenges imposed by these applications on reference circuits implemented in standard technologies, and discuss some solutions.

Session C3L-B: Active Security Measures

Chair: Ganesh Rao, *Draper Laboratory*
Time: Wednesday, August 9, 2017, 12:00 - 13:40
Location: Eaton Hall 201

Overlay-Based Side-Channel Countermeasures: A Case Study on Correlated Noise Generation 1308
Austin Baylis (University of Florida), Greg Stitt (University of Florida), Ann Gordon-Ross (University of Florida)

Side-channel attacks against field-programmable gate arrays (FPGAs) enable attackers to reverse-engineer bitfile encryption keys, resulting in intellectual-property (IP) theft and tampering. To address this problem, we demonstrate that overlays—virtual architectures implemented atop an FPGA—provide a novel countermeasure strategy that can protect application IP even on vulnerable FPGAs. Although we demonstrate such protection via a case study on correlated noise generation, the approach is potentially applicable to any countermeasure and any overlay. By extending existing overlay benefits (e.g., fast compilation, application portability, 1000x smaller bitfiles) with improved hardware security, our approach provides an attractive platform for Internet of Things, defense, and many embedded applications.

Hardware based Protection Against Malwares by PUF based Access Control Mechanism 1312
Ali Shuja Siddiqui (University of North Carolina at Charlotte), Chia-Che Lee (Florida Institute of Technology), Fareena Saqib (University of North Carolina at Charlotte)

Malwares are software based destructive payloads that infect and damage computing systems. Malwares like ransomware have become a popular form that encrypts directories and corrupt systems. A more recent ransomware has appeared with the name, Petya. Petya ransomware encrypts the master boot record of the hard disk on which it is installed and sabotages the boot process. The current software based anti-virus programs rely on signature based malware detection, but due to the automated malware development toolkits and more sophisticated malwares, the need of hardware based security solutions to prevent such attacks is inevitable. Additionally, such systems are only available for computers and not for IoTs or embedded systems. This paper proposes a hardware based architecture for access control and protection of pre-boot process and data against malwares.

Behavior Profiling of Power Distribution Networks for Runtime Hardware Trojan Detection 1316
Faiq Khalid (Vienna University of Technology), Syed Rafay Hasan (Tennessee Technological University), Osman Hasan (Vienna University of Technology), Falah Awwadl (National University of Sciences & Technology)

Runtime hardware Trojan detection techniques are required in third party IP based SoCs as a last line of defense. Traditional techniques rely on golden data model or exotic signal processing techniques such as utilizing Choas theory or machine learning. Due to cumbersome implementation of such techniques, it is highly impractical to embed them on the hardware, which is a requirement in some mission critical applications. In this paper, we propose a methodology that generates a digital power profile during the manufacturing test phase of the circuit under test. A simple processing mechanism, which requires minimal computation of measured power signals, is proposed. For the proof of concept, we have applied the proposed methodology on a classical Advanced Encryption Standard circuit with 21 available Trojans. The experimental results show that the proposed methodology is able to detect 75% of the intrusions with the potential of implementing the detection mechanism on-chip with minimal overhead compared to the state-of-the-art techniques

A Novel Correlation Power Analysis Attack on PIC based AES-128 without Access to Crypto Device 1320
Oluwadara Adegbite (Tennessee Technological University), Syed Rafay Hasan (Tennessee Technological University)

In most power analysis attack, power traces obtained from the cryptographic device are aligned using a crypto device based triggering signal. In reality, the attacker is not afforded the luxury of inserting a trigger in the encryption device source code. This paper aims to execute a CPA attack on an 8 bit PIC- microcontroller (µC) implementation of AES-128 encryption without a crypto µC–based triggering signal. To address the misalignment, a unique methodology that features the introduction of an intermediate µC coupled with a suitable alignment method is applied. The proposed method is able to extract each byte of the key of an AES-128 using 200 power traces with a correlation coefficient of 0.6225.

Session C3L-C: Low Power and Multi-Band RF Transceivers

Chair: Mona Hella, *Rensselaer Polytechnic Institute*
Time: Wednesday, August 9, 2017, 12:00 - 13:40
Location: Eaton Hall 202

Event-Driven Wakeup Receivers: Applications and Design Challenges 1324
Pouyan Bassirian (University of Virginia), Jesse Moody (University of Virginia), Steven M. Bowers (University of Virginia)

This paper presents an overview of the design considerations and challenges of event-driven wakeup receivers as well as an analysis of state-of-the-art (SOA) research. We consider advantages and disadvantages of the commonly utilized architectures in these systems as well as presenting big picture perspectives from an application standpoint. This paper focuses on event-driven scenarios where the activity factor of a node is so low that its standby power consumption, which sets the power floor in its sleep mode, becomes a dominant factor in determining the node lifetime.

A Transmitter Architecture for Wireless Medical Devices in the MICS Band 1328
Mahmoud A.A. Ibrahim (Northeastern University), Marvin Onabajo (Northeastern University)

This paper introduces a 401-457 MHz BFSK transmitter (TX) architecture that utilizes mixing and image rejection techniques to generate the two carrier frequencies for BFSK transmission. The proposed architecture enables low power consumption for a wide range of data rates by avoiding fast settling time requirements for the frequency-locked loop. Simulations indicate that the TX designed in 130nm CMOS technology can achieve data rates up to 10 Mbps with a power consumption of 140 microwatt or lower from a 0.6 V supply. Its estimated energy efficiency is 14 pJ/b while delivering -19.7 dBm of output power.

A Low-Power 2.4GHz ZigBee Transceiver with Inductor-Less RF Front-End for IoT Applications 1332
Bing Xia (Chinese Academy of Sciences / Weizhou Microelectronics Technology Co., Ltd.), Nan Qi (Chinese Academy of Sciences), Liyuan Liu (Chinese Academy of Sciences), Nanjian Wu (Chinese Academy of Sciences)

A fully integrated low-power 2.4GHz ZigBee transceiver with inductor-less RF front-end implemented in 180nm CMOS technology is demonstrated. The proposed double push-pull LNA collaborates with a current-mode down-converter to provide wideband low-noise reception, as well as the out-of-band blocker resilience. A sliding frequency synthesizer with low-frequency running VCO is employed to provide the local oscillation (LO) for both the RX and TX, with reduced power consumption. Measurement results show that, the RX reaches -102dBm sensitivity and dissipates 11mA power. The FS achieves -91dBc/Hz in-band phase noise with only 6.5mA DC power. The TX features +7.6dBm peak output power, 4% EVM at the cost of 19.5mA power.

A Compact Quadband DPA using a New Multiband Input Matching Network 1336
Bassem M. Abdelrahman (Military Technical College), Hesham N. Ahmed (Military Technical College), A.I. Nashed (University of Waterloo)

In this paper, a design architecture of a compact, concurrent quadband Doherty Power Amplifier (DPA) is proposed that relies on a new quadband band-pass filter comprsinging the input matching network. The filter - based on Quarter Wave Open Stubs (QWOS) at the desired operation frequencies - is embedded within the output arms of a wideband power divider to create the targeted four arbitrary frequencies of operation. A wideband output combining structure enables higher load modulation bandwidth; both the carrier and peaking amplifiers are matched to 100-ohms and their outputs are parallel combined directly to a 50-ohm load, thus eliminating need for an Impedance Transformation Network (ITN) commonly used in conventional DPAs. Proposed DPA architecture is validated through a quadband design targeting 850, 1500, 1800, and 2300 MHz bands. Implemented design achieved peak drain efficiencies of 60.5%, 54%, 61.5% and 44.5% when producing output powers of 42.5 dBm, 42.2 dBm, 41.8 dBm, 41.3 dBm at the four operation bands, respectively. At 6-dB output power back-off, the measured drain efficiencies are 47%, 44.6%, 48.6% and 43% and an output power back-off of about 36-dBm is achieved.

Session C3L-D: Image and Multi-Dimensional Signal Processing

Chair: Robert Brennan, *On Semi*
Time: Wednesday, August 9, 2017, 12:00 - 13:40
Location: Eaton Hall 203

An Ensemble Learning based Adaptive Algorithm for Capsule Endoscope Image Deblocking 1340
Yubing Bai (Tsinghua University), Xiang Xie (Tsinghua University), Guolin Li (Tsinghua University), Zhihua Wang (Tsinghua University)

In capsule endoscope system, discrete cosine transform (DCT) compression on medical image brings annoying mosaic effect. Previous methods focus more on perfect visual smoothness without considering detail reservation. To address this issue, we integrate ensemble learning model into projection onto convex set (POCS) method. Both structure features and severity of blocking artifacts are evaluated by learning model, and the learning results are used to adaptively modify parameters of constraint convex sets. Finally, we obtain a visually smooth diagnosis image with good detail reservation and an average peak signal to noise radio (PSNR) of 42.90.

Emotion Recognition based on Vertical Cross Correlation Sequence of Facial Expression Images 1344
M.I. Rashid (Bangladesh University of Engineering and Technology), M. Hasan (Bangladesh University of Engineering and Technology), N. Yeasmin (Bangladesh University of Engineering and Technology), C. Shahnaz (Bangladesh University of Engineering and Technology), S.A. Fattah (Bangladesh University of Engineering and Technology), W.P. Zhu (Concordia University), M.O. Ahmed (Concordia University)

Command extraction from human beings becomes easier for a machine if it can analyze the non verbal ways of communication such as emotions. This paper focuses on improving the efficiency of extracting emotion from human facial expression images. The features that were extracted in this experiment were obtained from JAFFE (Japanese Female Facial Expression) database which includes 213 images of different models who posed for 7 classes of expressions. Their images were refined through some steps and prepared for the classification process to recognize the emotions. We used viola-jones algorithm to find the ROI (regions of interest), where human emotions can be observed and detected noticeably and then the ROI parts have been segmented separately after some preprocessing. With these pre-processed segmented parts, we have performed cross correlation to build our feature vector which gives us the information about variation. The k-NN classifier has been used to detect emotion from test images.

Eye Gaze Detection System for Impaired User GUI Control 1348
Jared Hughes (Gentex Corporation), Samhita Rhodes (Grand Valley State University), Bruce E. Dunne (Grand Valley State University)

Gaze point, or point of regard, refers to the point in space where an individual's visual attention is focused. Estimating gaze point at a given time can provide a host of information pertaining to intention and perception of a scene. This information can be applied toward enhancement of Human-Computer Interaction (HCI), making such interfaces more smooth and efficient. For the population with limited or no mobility, a gaze point estimation system that accurately selects components of a computer application is extremely beneficial. Herein, a custom gaze point detection HW/SW system intended to allow the mobility hindered population the ability to control selection in a computer interface via gaze is presented. The principles of the image difference method for pupil detection, coupled with glint detection and calibration were implemented for an accurate, occlusion-immune estimation of gaze point in real-time. Under the ideal scenario of static head pose and lighting environment, the system was accurate to 1.05 . The gaze estimator tolerated small 1.5 inch head translations and over two orders of magnitude change in ambient illuminance, while sacrificing less than 1 of accuracy.

A Facial Recognition Method based on DMW Transformed Partitioned Images 1352
Ahmed Aldhahab (University of Central Florida / University of Babylon), Wasfy B. Mikhael (University of Central Florida)

A new approach based on applying the Two-Dimensional Discrete Multiwavelet Transform (2D DMWT) to the partitioned faces is proposed for face recognition. First, the input image is divided into six parts to reduce the effect of the unnecessary information on the system performance. Then, the 2D DMWT is applied to each part for feature extraction/dimensionality reduction. These features are classified using a Neural Network (NN) classifier. The system is evaluated using four databases. K-fold Cross Validation is used to analyze the results. The results confirm the system improvement in the recognition rates and the storage requirements.

Skin Lesions Classification based on Color Plane-Histogram-Image Quality Analysis Features Extracted from Digital Images 1356
M.A. Rahman (Bangladesh University of Engineering and Technology), M.T. Haque (Bangladesh University of Engineering and Technology), C. Shahnaz (Bangladesh University of Engineering and Technology), S.A. Fattah (Bangladesh University of Engineering and Technology), W.P. Zhu (Concordia University), M.O. Ahmed (Concordia University)

At first, images of skin lesions are pre-processed by resizing, removing hair, removing noise by filtering and enhancing contrast. The proposed segmentation of the preprocessed images is carried out by Color Thresholding in Lab color plane in order to obtain better contrast between normal and diseased regions. Segmented RGB images obtained after color thresholding in Lab plane are validated by open source software Interactive Segmentation Tool to yield an improved segmented image for feature extraction. Then higher order statistics based analysis, histogram based analysis and Image Quality Analysis(IQA) are performed for feature extraction. The features thus obtained from segmented images are fed to SVM and kNN classifiers to classify four classes of skin lesions such as Melanoma, Basal Cell Carcinoma, Keratoacanthoma and Squamous cell carcinoma. The simulation results of the proposed method is obtained using Dermnet database from where the four types of skin lesions images are obtained. In comparison to the another state of the art method of skin lesions classification, it is found that the proposed method is capable of producing better F1 score and accuracy.

Session C3L-E: Energy Harvesting and Power Management

Chair: Aatmesh Shrivastava, *Northeastern University*
Time: Wednesday, August 9, 2017, 12:00 - 13:40
Location: Eaton Hall 206

A Drift-Diffusion Solver using a Finite-Element Method to Analyze Carrier Dynamics at Ultra-High Solar Concentrations 1360
Emily Carlson (Tufts University), Margaret Stevens (Tufts University), David Emerson (Tufts University), Xiaozhe Hu (Tufts University), James Adler (Tufts University), Thomas E. Vandervelde (Tufts University)

We present a drift-diffusion and Poisson solver using a finite-element method to study carrier dynamics under ultra-high solar concentration. By modeling the carrier densities and the electric potential in quasi steady-state and dynamic conditions, we can use the splitting of the quasi-Fermi levels to model electrical properties such as open-circuit voltage. In this work, we analyze the validity of previously used approximations on open-circuit voltage and the effects of increasing optical carrier densities on small band gap solar cells. Graded mesh refinement is implemented to improve runtime. Ultimately, we show a change in the carrier profiles that may lead to detrimental charge carrier extraction.

Quantifying Power System Resiliency Improvement using Network Reconfiguration 1364
Pooria Dehghanian (Texas State University), Semih Aslan (Texas State University), Payman Dehghanian (Texas A&M University)

Resiliency assessment of the large-scale smart electricity grids has recently attracted many attentions in electric industry for more efficient daily operations in the face of emergencies. This paper aims to quantify the power system resiliency in dealing with grid severe vulnerabilities and extreme emergencies. The suggested approach for resiliency improvement is to harness the existing system infrastructure, with minimum additional cost, through transmission network reconfiguration. The applied concept of reconfiguration is predictively planned and used as a temporary operation mechanism for the main sake of electricity outage recovery. The system resiliency features, e.g., flexibility, capacity recovery, and the imposed cost indices, are quantified for each optimal reconfiguration option, helping the system operators evaluate the recovery options and decide on the final plan for implementation considering its impacts on system resiliency requirements. The suggested approach is tested on the IEEE 118-Bus test system under a critical contingency, and the results reveal its applicability and efficiency.

Stability and Design of Hysteretic Current-Mode Single-Inductor Multiple-Output Power Supplies 1368
Carlos J. Solis (Georgia Institute of Technology), Gabriel A. Rincón-Mora (Georgia Institute of Technology)

When supplied well and with little power losses, multifunctional microsystems can add life- and cost-saving intelligence to hospitals, factories, and cars. Unfortunately, fitting the multiple power supplies that diverse subsystems require into millimeters is challenging. One reason for this is, although efficient and therefore necessary, inductors are bulky. And supplying several outputs with one switched inductor requires several feedback loops that respond quickly. Even though hysteretic loops can react within one switching cycle, the nonlinear dynamics of intertwined hysteretic loops are difficult to manage. This paper explains how to analyze and design these fast single-inductor multiple-output (SIMO) power supplies.

Autonomous Maximum Power Point Tracking Algorithm for Ultra-Low Power Energy Harvesting 1372
Christoph Steffan (Infineon Technologies AG), Philipp Greiner (Technische Universität Graz), Carolin Kollegger (Technische Universität Graz), Inge Siegl (Infineon Technologies AG), Gerald Holweg (Infineon Technologies AG), Bernd Deutschmann (Technische Universität Graz)

An ultra-low power autonomous MPPT algorithm that maximizes the efficiency of a monolithic 0.98mmxmm solar harvester is presented. The MPPT is based on the perturbation and observation technique. It maximizes the efficiency of the ultra-low power harvester chip by maximizing the output current of the integrated charge pump. The analog algorithm is described in detail, introducing a resistorless high side current sensor for 100 nA to 1 mA. The paper concludes with measurement results regarding the tracking efficiency of the algorithm implemented on the single-chip harvester.

A Dual-Mode Passive Rectifier for Wide-Range Input Power Flow 1376
Ulkuhan Guler (Georgia Institute of Technology), Mohammad S.E. Sendi (Georgia Institute of Technology), Maysam Ghovanloo (Georgia Institute of Technology)

To increase power conversion efficiency (PCE), we introduce a new rectifier, which combines advantages of cross-coupled and cross-coupled bridge rectifiers by switching between the two topologies according to the incoming signal power level. In conventional designs, cross-coupled topology attains up to 80% PCE in the low-power range, while cross-coupled bridge topology attains up to 80% in the mid-power range. Hence, the proposed passive rectifier provides a minimum of 57% PCE in the entire low- and mid-power ranges. To switch between the two topologies, a voltage detector is used to sense very low input voltages followed by a control circuit. The TowerJazz 0.18-µm TS18PM CMOS high voltage power management process has been used for this analysis.

Session C3L-F: Power Management III

Chair: Robert Ashton, *Naval Postgraduate School*
Time: Wednesday, August 9, 2017, 12:00 - 13:40
Location: Paige Hall - Crane Room

Multi-Rate LQR Control of a Multi-Machine MVDC Shipboard Electric Distribution System with Constant Power Loads 1380
Adam J. Mills (Naval Postgraduate School), Robert W. Ashton (Naval Postgraduate School)

While many papers have developed single-input control schemes to regulate MVDC bus voltage where CPLs are present, multi-input controller schemes have not been explored. This paper presents two implementations of adaptive, multi-rate LQR controllers to regulate system voltages during step load transients. Through coordinated use of switching converter based low-rate DC voltage sources and high-rate energy storage device currents, multi-rate LQR controllers can provide excellent bus regulation by leveraging of all available control input devices. A periodic discrete-time multi-rate LQR controller (LQR-P) is described and compared to a selected matrix, multi-rate LQR controller (LQR-SM). Both are designed and implemented in MATLAB software using a hypothetical multi-machine, multi-zone shipboard MVDC electric distribution system with CPLs and energy storage devices.

Using Two Port Network Parameters for Equipment Specification to Ensure Stability and Limit Power Ripple in DC Power Systems 1386
Michael Knauff (Naval Surface Warfare Center), Shawn Plesnick (Naval Surface Warfare Center), Jonathan Berardino (Naval Surface Warfare Center), Nathan Spivey (Naval Surface Warfare Center)

Analysis methods for DC power interfaces using techniques built around the Nyquist stability criteria have previously been utilized to create system level specifications to ensure the stability of interconnected systems. This paper extends these concepts to not just ensure stability, but to also ensure a guaranteed maximum level of voltage and current perturbation within the system. The technique relies on representation of the subsystems as two-port networks. This paper discusses how two port networks can be used to form system specification. An example is also presented to illustrate how system specifications may be developed.

Application of a New Coupled-Inductor based DC Circuit Breaker 1390
Atif Maqsood (University of California-Santa Cruz), Keith Corzine (University of California-Santa Cruz)

This paper presents the design for a dc circuit breaker based on the coupled-inductor for use in dc grid protection. The breaker acts autonomously as a result of the fault current path. The exact step change in current required to open the breaker can be adjusted in the design by selecting an appropriate turns ratio for the coupled-inductor. A simulation is run for a zonal dc grid to demonstrate the application of multiple such breakers.

PAOA: A Power and Area Optimization Approach of Reed-Muller Logic Circuits 1394
Xiang Wang (Beihang University), Mingzhe Li (Beihang University), Zhenxue He (Beihang University), Weike Wang (Beihang University), Cheng Zhou (Beihang University), Zongmin Zhao (Beihang University)

To find the best polarity of large-scale Mixed Polarity Reed-Muller (MPRM) logic circuits, we proposes a new Adaptive Simulated Annealing Genetic Algorithm (ASAGA). Genetic Algorithm (GA) has outstanding global searching ability but easily falls into the local optimum , while the Simulated Annealing Algorithm (SAA) is expert in local searching but has the limitation of poor convergence. The new method incorporating SAA into GA can play their strengths to the utmost extent and make up their shortcomings. Additionally, for key parameters, we adopt self-adaptive adjustment, which can effectively improve the convergence and robustness of the algorithm.

Session C3L-G: Sensor Fusion

Chair: Claudio Talarico, *Gonzaga University*
Time: Wednesday, August 9, 2017, 12:00 - 13:40
Location: Paige Hall - Terrace Room

On Recent Advances in Synthetic Biology to Enable Programming Bacteria for Biosensing Applications 1398
Meghdad Hajimorad (California State University-Chico), Jeffrey A. Gralnick (University of Minnesota)

Traditionally, the “engineering” of microbes to arrive at organisms with desired behavior has required months (more often years) of trial-and-error type of experiments, with the undertaking being more akin to art than engineering. Enter synthetic biology, a burgeoning area that aims to put the engineering into genetic engineering. Here, we provide a short commentary on some advancements in this field. By relating these advances to recent progress in our understanding of extracellular electron transfer in bacteria, we also provide a perspective on synthetic biology having the potential to enable the programming of bacteria for electronics engineering-related applications such as biosensors.

Multilayer Graphene Nanoribbon based BioFET Sensor Design 1402
Nahid M. Hossain (University of Missouri-Kansas City), Emeshaw Ashenafi (University of Missouri-Kansas City), Moqbull Hossen (University of Missouri-Kansas City), Azzedin Es-Sakhi (University of Missouri-Kansas City), Masud H. Chowdhury (University of Missouri-Kansas City)

High performance biofunctionalized field effect transistors (BioFETs) use nanoscale electronic materials such as silicon nanowires (SiNWs), carbon nanotubes (CNT) and graphene for the sensing application. Specific focus will be on high-performance, low-cost,scalable, and reliable biofunctionalized field effect transistor (BioFET)based on graphene. We attempted to build the graphene based sensing device on silicon substrate. We are proposing a biosensor where graphene could be used as a channel material and extended gate for ion detection. The idea is to combine existing concepts of biosensors based on ion- sensitive field-effect transistor (ISFET) and chemically modified field-effect transistors (CHEMFET), and implement it on a new Graphene nanoribbons (GNR) based BioFET. Both ISFET and CHEMFET concepts are based on floating-gate transistor operation similar to that of Flash memory design. In this paper, we will explore regular transistor based graphene FET (GFET) intended for biosensing application.

A Dynamic Model-Aided Sensor Fusion Approach to Aircraft Attitude Estimation 1406
Matthew Rhudy (Pennsylvania State University)

Sensor fusion techniques are a popular approach to attitude estimation. However, an additional source of information that has been mostly overlooked is the control inputs. This information is typically known, and when coupled with an aircraft dynamic model, can predict the aircraft states. This information when fused with other sensor measurements through Kalman filtering techniques offers a reasonable method for using all available information to predict aircraft attitude. This work presents the procedure for implementing this sensor fusion idea with some simulation results from a known aircraft dynamic model.

New Approach for Indoor Fall Detection by Infrared Thermal Array Sensor 1410
Akira Hayashida (Fukuoka University), Vasily Moshnyaga (Fukuoka University), Koji Hashimoto (Fukuoka University)

This paper presents new approach for unobtrusive indoor fall detection by an IR thermal array sensor. Unlike existing methods that run fall detection at server and require high communication rates, we perform fall detection within the sensor node by a computationally inexpensive algorithm that only signals the server when a fall occurs. Experiments with prototype design show that such formulation provides robust and real-time fall detection even in a noisy environment.

Automated Phase Offset Correction using Reflectometry in Fault Detection Systems 1414
Esteban Cabanillas (CEA, LIST), Christophe Layer (CEA, LIST)

Well established cable network diagnosis systems rely on reflectometry principles to detect faults using specific signals within a frequency spectrum of a few hundreds MHz only. Huge performance improvements in terms of precision and sensitivity can be achieved higher frequencies and signal modulation, hence revealing phase and amplitude response of the potential impedance discontinuities on the tested channel to better classify the defects. However, frequency translation requires a special care in signal processing and the relative complexity has discouraged its implementation in wire diagnosis systems for now. Crossing domains with an ingenious phase offset correction mechanism, we show that defects can be accurately detected and correctly analyzed. Our method provides several advantages over state-of-the-art techniques and is particularly well suited for implementations in distributed sensor networks. Accordingly, measurements were performed using an FPGA-based embedded platform and discrete high-frequency components.

Session C4P-H: Circuits and Systems

Chair: Sherif Michael, *Naval Postgraduate School*
Time: Wednesday, August 9, 2017, 13:40 - 15:00
Location: Ballou Hall - Coolidge Room

A Novel Optimization Framework for the Design of Gilbert Cell Mixers 1418
G. Piccinni (Politecnico di Bari), G. Avitabile (Politecnico di Bari), G. Coviello (Politecnico di Bari), C. Talarico (Gonzaga University)

This paper presents a new framework for the design optimization of a CMOS down-conversion mixer based on a conventional double balanced Gilbert cell. The framework exploits the gm/ID methodology to find the transistors' dimensions that optimize the tradeoff between conversion gain, noise figure, third-order intercept and power DC consumption of the mixer. The mixer has been designed using a 0.13 µm process from IHP Microelectronics, and it exhibits a conversion gain of 13.1 dB at 0 dBm local oscillator's power. The average noise figure is 11.9 dB, the input third-order intercept is -2.8 dBm and the output third-order intercept is 9.7 dBm. Finally, the chip-core without bonding pads measures only 0.028 mm by 0.034 mm and it dissipates 1.5 mW with a 1.5 V supply.

A Hybrid Memristor-CMOS Multiplier Design based on Memristive Universal Logic Gates 1422
Mehri Teimoory (University of Windsor), Amirali Amirsoleimani (University of Windsor), Arash Ahmadi (University of Windsor), Majid Ahmadi (University of Windsor)

Memristor is considered as one of the promising solutions to the fundamental limitations of the VLSI systems. Logic implementation with memristor device by considering its compatibility with CMOS fabric provides a new vision for digital logic circuits. This work presents a 2 by 2 multiplier cell design using a hybrid CMOS-memristor universal gate. The universal gate based implementation approach is the extension for memristor ratioed logic (MRL) with lower implementation cost. Simulation results confirm functionality of the proposed circuit. This circuit requires 16 memristors, 8 transistors and only one computational time step for multiplication. Compared with previous works, this approach presents considerably lower implementation cost.

Power Management Circuit for Kinetic Energy Harvesting from Freight Railcars 1426
Thomas O'Connor (Virginia Polytechnic Institute and State University), Ji Hoon Hyun (Virginia Polytechnic Institute and State University), Dong Sam Ha (Virginia Polytechnic Institute and State University)

The proposed circuit aims to harvest energy from freight railcars, in which a three-phase electromagnetic generator is used to harvest kinetic energy. The key idea of the proposed circuit is to extract maximum power from the transducer through impedance matching until the charge level of the battery reaches 90 %. Once, the batter reaches the charge level, it switches the operation mode and regulates the output voltage to protect the battery from overcharging. In contract to the conventional two-stage topology, the proposed circuit adopts a single stage topology to reduce power dissipation and hence the conversion efficiency.

Design and Analysis of 2T-2M Ternary Content Addressable Memories 1430
M.A. Bahloul (King Abdullah University of Science and Technology), M.E. Fouda (University of California-Irvine), R. Naous (King Abdullah University of Science and Technology), M.A. Zidan (King Abdullah University of Science and Technology), A.M. Eltawil (University of California-Irvine), F. Kurdahi (University of California-Irvine), K.N. Salama (King Abdullah University of Science and Technology)

Associate and approximate computing using resistive memory based Ternary Content Addressable Memory is becoming widely used. In this paper, a simplified model based analysis of a 2T2M-Ternary Content Addressable Memory using memristors is introduced. A comprehensive study is presented taking into consideration different circuit parameters and parasitic effects. Parameters such as the memristor RH=RL ratio, transistor technology, operating frequency, and memory width are taken into consideration. The proposed model is verified with SPICE showing a high degree of matching between theory and simulation. The utility of the model is established using a design example.

THz Detection in Sub-Threshold Si MOSFETs by Non-Linear Channel Electron Density Modulation 1434
Moeen Hassanalieragh (University of Rochester), J. Daniel Newman (Harris Corporation), Kenneth Fourspring (Harris Corporation), Zeljko Ignjatovic (University of Rochester)

In this paper, we explain the THz detection mechanism in sub-threshold Si MOSFETs by exploiting the exponential dependence of channel electron density to the gate-source voltage. According to our theory, this high frequency non-linear dependence is the underlying mechanism for rectification of THz radiation. The maximum detection frequency is limited by dielectric relaxation time of the electrons inside the channel close to the source region, which lies well into the THz range. Extensive two-dimensional TCAD device simulations in time domain support our proposed theory.

A Full-Rate 40 Gb/s Clock and Data Recovery with Resonator-Based Frequency-Doubling Mechanism in 0.13-µm CMOS 1438
Joseph Chong (Virginia Polytechnic Institute and State University), Dong Sam Ha (Virginia Polytechnic Institute and State University)

A clock and data recovery circuit for full-rate 40 Gb/s optical receiver is presented employing mixer-based phase detection architecture. A frequency-doubling mechanism architecture preceding the mixer is proposed to achieve higher clock frequency. Utilizing LC-resonator based tuned amplifier and frequency-doubler, the approach doubles clock frequency comparing to similar architecture or technology, and realizes a 40 GHz clock recovery with 0.13-um CMOS technology.

FPGA Implementation of Multi-Band Spectral Subtraction Method for Speech Enhancement 1442
Mohammed Bahoura (University of Quebec at Rimouski)

This paper proposes a hardware architecture of the multi-band spectral subtraction method for real-time speech enhancement. The proposed hardware architecture has been implemented on field programmable gate array (FPGA) device using Xilinx system generator (XSG) and Nexys-4 development board. Multi-band approach is based on the fact the whole speech spectrum does not be affected uniformly by the colored noise. Speech enhancement performances obtained by the hardware architecture are compared to those obtained by MATLAB simulation. The resource utilization and the maximum operating frequency are reported for an Artix-7 FPGA chip.

Algorithmic-Pipelined ADC with a Modified Residue Curve for Better Linearity 1446
Mohammad H. Naderi (Texas A&M University), Jose Silva-Martinez (Texas A&M University)

In this paper, the minimum total required transconductance for the different architectures of the pipelined ADC are computed. This helps the pipelined ADC designers to find the most power-efficient architecture between different topologies based on the same input-referred thermal noise. It is shown that the Algorithmic-Pipelined ADC requires a simpler Sub-ADC and shows lower sensitivity to the MDAC errors and smaller area and power dissipation in comparison to the conventional multi-bit per stage pipelined ADC. Also, it is shown that the Algorithmic-Pipelined architecture is more-tolerant to capacitive mismatch for the same input-referred thermal noise than the conventional multi-bit per stage architecture. To take full advantage of these properties, a modified residue curve for the pipelined ADC is proposed. This concept introduces better linearity compared with the conventional residue curve of the pipelined ADC; this approach is particularly attractive for the digitization of signals with large peak to average ratio such as OFDM coded signals.

100mV Precision 40V Tolerant Scalable Cap free Current Limited Voltage Source for Wide Input Current Range 1450
Sri Navaneeth Easwaran (Texas Instruments Inc.),
Robert Weigel (Friedrich-Alexander-Universität Erlangen-Nürnberg)

A 40V tolerant current limited voltage source for a wide input current range is presented. Integrated current limited voltage sources are needed for diagnosis purposes in automotive applications like airbag squib drivers that deploy airbags. The topology proposed here overcomes the conventional on chip Zener based topology that is sensitive to process variations and provides reliable operation in a multiple supply voltage environment. The poles and unity gain bandwidth of the circuit remain constant for all input currents. The circuit can be programmed to any output voltage with 100mV precision. A cap free topology is achieved such that a wide range of load capacitors can be connected without impacting stability. This circuit is needed in automotive applications but not limited to other applications. This circuit is fabricated in a 40V, 0.35µm BiCMOS process.

A Neural Network Architecture using High Resolution Multiplying Digital to Analog Converters 1454
Farrinoush Saffar (University of Windsor), Mitra Mirhassani (University of Windsor),
Majid Ahmadi (University of Windsor)

In this paper, a novel neural network architecture is proposed which results in an area-efficient feed-forward network. These structures require high-resolution multipliers. In order to overcome this problem, a mixed-signal Multiplying Digital to Analog Converter (MDAC) architecture which employs Delta- Sigma Modulation (DSM) to encode the multiplication results into the time domain. The time-domain pulse stream sequence can be converted to into a current-mode signal using a Low-Pass filter. The outcome is an area efficient neural network with a high degree of integration.

A 4.3 to 5.7 GHz Frequency-Agile Receiver for Rapidly-Changing Channels 1458
Dai Li (Rice University), Aydin Babakhani (Rice University)

This work reports a frequency-agile receiver front-end for rapidly changing channels. The receiver includes a programmable low noise amplifier (LNA) that can be tuned from 4.3 to 5.7 GHz using an all-digital phase-locked loop (ADPLL). It also includes a power detector, a 10-bit SAR ADC, and a closed-loop system to dynamically adjust the matching of the LNA to maximize its output power.

A Low-Noise, Low-Power Signal Conditioning Circuit with Narrow Bandwidth 1461
Parisa Vejdani (École de Technologie Supérieure), Frederic Nabki (École de Technologie Supérieure)

A low-noise and low-power signal conditioning circuit with narrow bandwidth is presented. The circuit cascades three stages. A high current and low supply voltage amplifier as the first stage decreases the thermal noise and power consumption. A differentiator and integrator are used as the second and third stages to reach the amplification with anarrow bandwidth suitable for microelectromechanical systems. Moreover, the first and second stages are chopped with two different frequencies to remove their flicker noise. The circuit is designed in a 0.13 µm CMOS technology with a 1.2 V and 0.4 V supplies. The simulated power consumption is 7 µW, the gain is 55 dB, and the bandwidth can be tuned to 3.7 kHz, 1.9 kHz and 0.24 kHz. The input noise floor is 14.4 nV/√Hz.

An 8b 5-GS/s CMOS SAR ADC with Speed Optimized SAR Logic 1465
Aarti Shah (University of Illinois at Urbana-Champaign),
Bibhu Datta Sahoo (University of Illinois at Urbana-Champaign)

An 8b 5-GS/s Successive Approximation Register (SAR) ADC is implemented in 65-nm CMOS using 16-channel time-interleaving, achieving a SNR of 43.5 dB and Figure-of-Merit (FoM) of 245 fJ/conv-step. High speed operation is achieved by optimizing the critical path in the SAR ADC loop. A sampling network with a split-array with unit bridge capacitor topology is used to reduced the area of the sampling network and switch drivers. The ADC consumes 149 mW of power.

Electrochemical Impedance Spectroscopy Circuitry for Biosensor Applications 1469
Purva Bhatnagar (University of Cincinnati), Fred R. Beyette Jr. (University of Cincinnati)

Electrochemical Impedance Spectroscopy (EIS) is widely popular in the medical field where it is often referred to as bioelectrical impedance analysis (BIA) used to analyze biological materials as well as characterization of body fluids. It is a complex technique requiring expensive equipment that is also large making it difficult to integrate into small form-factor systems that are hand-held, wearable and intended for use in point-of-care testing. This paper presents a prototype design of a miniaturized and low cost EIS module aimed to render effective point-of-care testing of biomarkers from body fluids. The proposed system is based on an embedded system design to be factored to achieve small valuation time for results along with being compact and portable enough to be used outside laboratory bench setting.

N-Port LNAs for mmW Array Processors using 2-D Spatio-Temporal Δ-Σ Noise-Shaping 1473
Yingying Wang (Case Western Reserve University), Suranga Handagala (University of Akron), Arjuna Madanayake (University of Akron), Leonid Belostotski (University of Calgary), Soumyajit Mandal (Case Western Reserve University)

A novel delta-sigma (Δ-Σ) modulation method is proposed for extending noise-shaping to two dimensions: space and time. The goal is to improve the noise figure (NF) and linearity of low noise amplifiers (LNAs) for use in microwave and mm-wave antenna arrays. We show that a spatially-oversampled antenna array coupled to an N-port noise-shaped LNA can diminish in-band additive noise and distortion by shaping the multi-dimensional spectrum of these unwanted components towards higher spatial frequencies that are outside the space-time region of support (ROS) of all possible propagating electromagnetic waves. The shaped noise is then removed by spatial filtering with a linear beamformer. This paper analyzes the concept and presents simulation results for a 33, 65, and 129-port noise-shaped LNAs in 65nm CMOS operating at 4GHz.

Continuous Recognition with Incremental Learning on Grassmann Manifolds 1477
Sherif Azary (Rochester Institute of Technology), Andreas Savakis (Rochester Institute of Technology)

We present incremental learning on Grassmann manifolds. In Grassmann kernel learning frameworks, data are embedded on subspaces and kernels are constructed to map data subspaces to a projection space for classification. As new data become available, retraining degrades computational performance as Grassmann kernels need to be recomputed on larger matrices. We propose a computationally efficient technique for incremental Grassmann kernel learning that achieve linear time complexity utilizing the GROUSE framework to embed new data onto a pre-existing Grassmann manifold and mapping the embeddings from a Grassmann space onto a projection space by exploiting the positive definite structure of Grassmann kernels.

A 200MS/s 7bit Time Domain Ring Quantizer 1481
Arun Javvaji (University of Florida), Pavan Terdal (University of Florida), Changsok Han (University of Florida), Taewook Kim (University of Florida), Nima Maghari (University of Florida)

This paper presents a new switched capacitor based ring quantizer circuit. The circuit is inspired from a ring amplifier with some important modifications to enable time based quantization instead of amplification. The proposed quantizer which is a natural extension of the ring amplifier can be employed as a multi bit quantizer in pipelined analogue-to-digital converter and delta-sigma-modulators thereby replacing conventional comparator based quantizers, hence drastically reducing the overall complexity. The proposed structure was designed and simulated in a 130 nm CMOS process. The quantizer was sampled at a clock frequency of 200 MHz (fs) and consumes 600μW at 1.2V power supply.

Tunneling Transistor based 6T SRAM Bitcell Circuit Design in Sub-10nm Domain 1485
Nahid Hossain (University of Missouri-Kansas City), Arif Iqbal (University of Missouri-Kansas City), Hemanshu Shishupal (University of Missouri-Kansas City), Masud H. Chowdhury (University of Missouri-Kansas City)

We investigate the effect sub-10-nm n-type GaSb–InAs heterojunction tunnel field-effect transistor (Het-j TFET) on 6T based SRAM cell. Because of the high performance at ultra-low voltage operation TFET would be an attractive choice for designing memory device. We also study the reliability issue of for both TFET based SRAM & 10nm FinFET based SRAM. It shows that TFET based SRAM has greater reliability than the FinFET based SRAM. A look up table based Verilog A behavioral model was designed to simulate the circuit in the HSPICE.

Offset Compensation in a Track and Hold Circuit 1489
Shirin Pourashraf (New Mexico State University), Jaime Ramirez-Angulo (New Mexico State University), Alfonso R. Cabrera-Galicia (INAOE), Antonio J. Lopez-Martin (Universidad de Navarra), Ramon González-Carvajal (Universidad de Sevilla)

Using a new DC offset compensation method, a fully differential track and hold circuit is presented. It stores an amplified version of the offset during the hold phase, which is used in attenuated fashion during the track phase to compensate offset. This scheme is less sensitive to charge injection and other errors than conventional offset compensation schemes. Experimental results of a test chip in 180 nm CMOS technology verify the proposed scheme.

On-Die Power Grid Broadband Model Determination using a Priori Narrowband Measurements 1493
Leonard Maceachern (Carleton University), Xin Jie Wang (Carleton University), Tad Kwasniewski (Carleton University)

Frequency domain methods of extracting equivalent series resistance (ESR) and equivalent series capacitance (ESC) for on-die decoupling capacitors using spice-like simulators are briefly reviewed. A concise method is then proposed for converting the frequency domain equivalent ESR and ESC to an approximate broadband equivalent circuit which can be readily used in time domain simulations. The method is validated using empirical measurements of relevant integrated circuits.

Enhanced Vehicle Classification via 3D Geometries 1497
William McDowell (Lockheed Martin), Wasfy B. Mikhael (University of Central Florida)

We present a mobile vehicle classification technique achieved by tracking two vehicle based Points of Interest (PoI) in multiple filter configurations to compose a vehicle specific 3D geometry. Using high fidelity physics based simulation we demonstrate the capability to classify the 3D geometries in the presence of noise by extracting vector lengths and angles as features. Additionally, we investigate the classification advantages presented by representing the features in multiple linear transform domains and fusing the information from those different domains into a single ensemble classifier.

Carbon Nanomaterial based Sensors for Astrobiology Exploration 1501
S.K. Islam (University of Tennessee), I. Mahbub (University of Tennessee), S. Shamsir (University of Tennessee)

Carbon nanomaterials are emerging as popular platforms for the development of advanced sensor technologies. This paper reports fabrication, characterization, and testing of carbon nanomaterial based sensors for astrobiology exploration. Development of nanostructured sensor instruments and associated sensor electronics are designed to implement a prototype sensor instrument in "lab-in-a-teacup" platform. The prototype nanostructured sensors consisting of vertically aligned carbon nanofibers (VACNF) are capable of providing a basis for small volume electroanalyses in probing regions elevated above the planar substrate. In addition, the sensor probes demonstrate excellent sensitivity and fast response time which can potentially extend the application of these probes in various electrochemical sensor systems. The prototype sensors instrument incorporates massively parallel electrochemical sensing devices capable of investigating life in either terrestrial or extraterrestrial environment.

Session C4P-J: Late Breaking News

Time: Wednesday, August 9, 2017, 13:40 - 15:00
Location: Ballou Hall - Coolidge Room

Charge Recovery Implementation of an Analog Comparator: Initial Results 1505
Leo Filippini (Drexel University), Lunal Khuon (Drexel University), Baris Taskin (Drexel University)

This work introduces a charge recovery comparator circuit for low-power low-frequency applications. For the first time, the principles of charge recovery logic, or adiabatic logic, are applied to an analog circuit. The comparator was designed and simulated in a 180nm technology and compared to state of the art solutions. Post-extraction simulations show that the proposed comparator consumes only 46 fJ per conversion in the nominal PVT corner, while having a total area of 45μm2. The proposed comparator consumes up to 70% less power than a state of the art dynamic latch comparator.

A Low-IF Bandpass ΔΣ ADC for Fully-Integrated CMOS Magnetic Resonance Imaging Receivers 1509
S. Paton (Carlos III University of Madrid), E. Prefasi (Carlos III University of Madrid), M. Dominguez-Suarez (Carlos III University of Madrid), M. Portela-Garcia (Carlos III University of Madrid)

This work presents a 180-nm CMOS bandpass SD Analog-to-Digital Converter (ADC) developed to fulfill the specifications of a fully-integrated receiver for Magnetic Resonance Imaging (MRI). CMOS integration of a multichannel digital receiver would increase the quality of the image without the need of using many coaxial cables to connect the RF coils (located close to the patient) with the digitizing and processing hardware. A very simple Low-IF receiver is proposed with digital IQ demodulation, where a continuous time Low-IF bandpass ADC is the most efficient architecture. The continuous time circuitry can be used to remove the classical filter, as in this application no interferers are expected, and an anti-alias filter is enough. The bandpass loop filter attenuates the quantization noise in the narrow input bandwidth, while stability is easily achieved, as in many low-pass loop filters, due to the selected Low-IF. Measurements show 82dB DR over 1MHz bandwidth, centered at 5MHz. The measured IMD3 product is 74dB, which is good enough for the application.

All-Digital ΔΣ TDC with Differential Bi-Directional Gated-Delay-Line Time Integrator 1513
Young Jun Park (Ryerson University), Fei Yuan (Ryerson University)

This paper presents a fully differential bi-directional gated delay line (BD-GDL) time integrator and its application in an all-digital first-order $\Delta\Sigma$ time-to-digital converter (TDC). The BD-GDL time integrator performs simultaneous time integration and multi-bit quantization, allowing rapid time integration and quantization with minimum power consumption. The nonlinearity of the BD-GDL time integrator is examined in detail. An all-digital first-order $\Delta\Sigma$ TDC utilizing the proposed DB-GDL time integrator was designed in an IBM 130 nm 1.2 V CMOS technology. A sinusoidal time input of 430 ps amplitude and 231 kHz frequency is digitized by the TDC with 25 MHz sampling frequency. The figure-of-merit (FOM) of the TDC is 8.03 fJ, outperforming known all-digital $\Delta\Sigma$ TDCs.

Pseudo-Pseudo-Differential Circuits 1517
Tao He (Oregon State University), Manjunath Kareppagoudr (Oregon State University), Un-Ku Moon (Oregon State University), Gabor C. Temes (Oregon State University), Yi Zhang (Analog Devices Inc.)

Pseudo-differential circuits approximate the performance of fully-differential structures, while allowing single-ended operation of the two half stages in the circuit. This requires duplication of the circuitry, with accurate symmetry needed between the two halves to cancel common-mode noise. This paper proposes a single-ended scheme which uses double sampling and time interleaving to achieve a performance comparable to that of differential circuits. It requires only half the complexity and reduced power dissipation compared to fully- or pseudo-differential circuits.

Bayesian Inference using Spintronic Technology: A Proposal for an MRAM-Based Stochastic Logic Gate 1521
David H.K. Hoe (Loyola University Maryland)

The design of a stochastic Muller C-element that uses spin-based magnetic tunnel junction devices is described. These nanodevices allow the compact implementation of the memory buffers, which are required to reshuffle the output bitstream in order to minimize the problem of autocorrelation inherent to the Muller C gate. A simple rotating buffer is shown to be effective in mitigating the impact of the autocorrelation effect when used with a multi-input C element. Improved area efficiency is expected compared to previous designs as the control signals for the memory buffer can be shared across several C-elements.

A New Approach of Stochastic Computing for Arithmetic Functions in Wideband RF Transceivers 1525
Van-Tinh Nguyen (Le Quy Don Technical University), Van-Phuc Hoang (Le Quy Don Technical University), Van-Thuan Sai (Le Quy Don Technical University), Tieu-Khanh Luong (Le Quy Don Technical University), Minh-Tu Nguyen (Le Quy Don Technical University), Han Le Duc (Le Quy Don Technical University)

This paper presents a new approach to approximate various complex arithmetic functions for applications in wideband RF transceivers by using stochastic computing based on the piecewise linear (PWL) approximation. The optimized design parameters for PWL approximation are chosen by an optimization algorithm targeting the best tradeoff between hardware complexity and approximation accuracy. Then, this approximation is implemented by stochastic logic circuits. The proposed approach outperforms previous works based on Maclaurin expansions, Bernstein polynomial and finite-state-machine implementations while achieve similar computation accuracy.

Spin Transfer Torque Driven Coupled Oscillators for Self-Oscillating RF Mixers 1529
Supriyo Maji (Purdue University)

Spin transfer torque oscillators (STOs) based on magnetic tunnel junction (MTJ) devices are emerging as a possible replacement for complementary metal-oxide semiconductors for radio-frequency (RF) signal generation. Advantages include low power consumption, small device area, and large frequency tunability. But such a single device cannot achieve the necessary noise performance for RF applications. It has been reported lately that a network of globally coupled STOs achieves significant improvement in phase noise. The study here is to propose use of such coupled STOs as self-oscillating RF mixers. Critical mixer performance parameters, including conversion gain, output power, and linearity, are discussed.

Novel Technique to Improve Strength of Weak Arbiter PUF 1532
Nitin Pundir (University of Toledo), Fathi Amsaad (University of Toledo), Muhtadi Choudhury (University of Toledo), Mohammed Niamat (University of Toledo)

In this paper, we aim at increasing the strength of weak arbiter physical unclonable function (APUF) which are vulnerable to modeling attacks because of low uniqueness and randomness. We propose a unique technique which takes n x 1 challenge-response pairs (CRPs) from APUF and combines them with ring oscillators (ROs) implemented on the same FPGA to get n x n CRPs. We claim the proposed technique to be immune to modeling attacks to a great extent. The experimental results show that the uniqueness and randomness of the APUF increase by at least 19% and 16%, respectively after the implementation of proposed technique.

Characterization and Model Validation of Triboelectric Nanogenerators using Verilog-A 1536
Ahmed Zaky (University of Science and Technology at Zewail City), Mohamed Shehata (Cairo University), Yehea Ismail (American University in Cairo), Hassan Mostafa (Cairo University)

Triboelectric nanogenerators (TENGs) are considered a very promising technique for harvesting mechanical energy due to its ease of fabrication, relatively cheap materials, large output power and high conversion efficiency compared to other techniques such as those relying on piezoelectric and electromagnetic effects. However, no study has yet been reported to present circuit simulation models for this type of devices. In this paper, a Verlilog-A model is established for TENGs as a circuit element to describe the TENGs behavior and explore its ability to be integrated into different applications. These models are validated by comparing its results to those obtained in the literature both analytically and numerically. Simulation results show an excellent agreement with prior work, which was a motivation for further investigation for the performance of those various modes. A unified parameter set is used to the four TENG fundamental modes such that a fair comparison is guaranteed between them in terms of both intrinsic characteristics and under different loading conditions.

A Reconfigurable Hardware Platform Implementation for Software Defined Radio using Dynamic Partial Reconfiguration on Xilinx Zynq FPGA 1540
Ahmed Kamaleldin (Cairo University), Sherif Hosny (Mentor Graphics), Khaled Mohamed (German University in Cairo), Mostafa Gamal (Cairo University), Abdelrhman Hussien (Cairo University), Eslam Elnader (Cairo University), Ahmed Shalash (Cairo University), Abdelfattah M. Obeid (King Abdulaziz City for Science and Technology), Yehea Ismail (American University in Cairo), Hassan Mostafa (Cairo University)

Dynamic Partial Reconfiguration (DPR) can be used efficiently to implement a reconfigurable hardware platform for SDR system that supports 3G, WIFI, and LTE standards. This method optimizes several design metrics such as: hardware resources, power, and reconfiguration time. Nevertheless, partitioning is a challengeable issue in the DPR flow. In this work, we implement two design approaches: one with single-partition approach and another with multi-partitions using a partitioning algorithm, introduced in the literature. A complete DPR design flow is discussed. Also, a comparison between the two approaches is evaluated on a Xilinx Zynq FPGA. It is observed that the multi-partition-based approach gives 16% less reconfiguration time, while reducing the reconfiguration area and power consumption by 4.5% and 9.8% respectively.

Area-Efficient Read/Write Circuit for Spintronic Memristor based Memories 1544
Sherif F. Nafea (Suez Canal University), Ahmed A.S. Dessouki (Port Said University), S. El-Rabaie (Menoufia University), Basem E. Elnaghi (Suez Canal University), Yehea Ismail (American University in Cairo), Hassan Mostafa (Cairo University)

Memory circuits occupy substantial area percentage of recent integrated circuits' chips. In addition, the continuous scaling of CMOS technology faces increasing technological difficulties. Thus, there is a need for alternative technologies that can offer larger memory densities and better performance. Spintronic memristor offers a good alternative for memory design due to its inherent non-volatility, good scalability, and radiation hardness. In this paper, a read/write circuit for spintronic memristor based memories is proposed. The proposed read/write circuit achieves a significant reduction in the occupied area. The read disturbance of the circuit is investigated to calculate the maximum allowed number of reading cycles before a refreshment operation is needed.

Multi-Context Scrubbing Method 1548
Takumi Fujimori (Shizuoka University), Minoru Watanabe (Shizuoka University)

Two salient concerns of current field programmable gate arrays (FPGAs) used for space applications are how to block soft errors that arise on their configuration memories and how to treat permanent failures attributable to total dose effects. To date, those two main concerns have been treated separately, but we present a proposal for multi-context scrubbing to "kill two birds with one stone" and resolve both issues simultaneously.

Simulation, Design and Integration of 60 GHz Gallium Nitride Transceiver into Nano-Ferrite Circulator On-Silicon CMOS Substrate 1552
Jun Jadormio (Tufts University), Mohammed Nurul Afsar (Tufts University), Valencia Joyner Koomson (Tufts University)

In this work the design and integration of 60 GHz monolithic microwave integrated circuit (MMIC) transceiver using 0.15 um Gallium Nitride (GaN) Qorvo process that will support the Wireless Gigabit Alliance (WiGig)/802.11ad radio specifications will be presented. The wideband GaN Power Amplifier (PA) can operate at 60-65 GHz with output power of 27 dBm and large signal gain of 23.5 dB. The wideband Low Noise Amplifier (LNA) has a small signal gain of 16 dB with a noise figure (NF) of 1 dB. The GaN PA and LNA are integrated to a nano-ferrite on-silicon CMOS circulator to construct a single front-end transceiver module.

Explicit Layout Pattern Density Controlling based on Transistor-Array-Style 1557
Chao Geng (The University of Kitakyushu), Bo Liu (The University of Kitakyushu), Shigetoshi Nakatake (The University of Kitakyushu)

An aggressive controlling for layout pattern density is becoming essential for the manufacturability of advanced processes. Focusing on analog layout under severe density constraints, this paper provides a novel idea that layout generation and verification are coworking on a density-aware format. Our idea follows a transistor-array(TA)-style of analog layout where unit-transistors of the same channel-size are used to form an array. In this style, we can explicitly control the layout pattern density by changing array pitch, stretching poly gates or widening diffusion of unit-transistors. We present a framework to enumerate feasible design parameters satisfying density and DRC constraints. In a design case of an OPAMP layout in a 65nm process, we demonstrate that our framework can converge the design in much fewer iterations compared with a traditional style layout by manual drawing.

Technique for Generating Timing Skew Resistant Time-Interleaved Signals 1561
Qianqian Wang (Iowa State University), Degang Chen (Iowa State University), Randall L. Geiger (Iowa State University)

A technique generating timing skew resistant time-interleaved signals is proposed. With a simple logic function, all the timing alignment critical signals' falling edges or rising edges can be trimmed by the master clock. Thus the generated time-interleaved signals are resistant to timing skew. Applied these time-interleaved signals to a time-interleaved ADC, the extra complex technique for timing skew calibration can be saved.

A 1.2-V 730-nW 10-Hz–3.5-kHz Programmable Biopotential Front-End 1565
R. Pulido (University of Las Palmas of Gran Canaria), J. Santana-Abril (University of Las Palmas of Gran Canaria), J. Sosa (University of Las Palmas of Gran Canaria), Juan A. Montiel-Nelson (University of Las Palmas of Gran Canaria)

This paper introduces a power and gain optimized programmable gain-bandwidth amplifier as sensor interface of physiological signals for batteryless applications. The proposed interface is divided in two independent stages that use capacitive networks to efficiently calibrate its gain and bandwidth. The sensor interface adjusts the lower (analog control)and the upper (digital control) cutoff frequencies of the filter. The gain is digitally controlled by a capacitive network in the feedback path of the PGA. The circuit has been integrated in a chip using a 90nm CMOS commercial technology process. The power consumption of the whole sensor interface is 730 nW for a voltage power supply of 1.2 V.

Tunable kΩ to GΩ Pseudo-Resistor with Bootstrapping Technique 1569
Diogo M. Caetano (Universidade de Lisboa), David Oliveira (Universidade de Lisboa), João Silva (Universidade de Lisboa), Taimur Rabuske (Universidade de Lisboa), Jorge Fernandes (Universidade de Lisboa)

This paper presents a novel architecture for a kilo-ohm to giga-ohm pseudo-resistor (PR), based on transistors operating in subthreshold with a fixed-V_GS configuration. This PR when used in an RC filter has a very low and constant settling time regardless of the programmed pole frequency. The proposed PR takes advantage of bootstrapping to improve its tuning range. By defining a constant V_GS for the transistors using a pre-charged capacitor, voltages from GND to VDD can be used and the transistor can be tuned to work from the cut-off region (for high resistances in the order of giga-ohms) to the deep triode region (for low resistances in the order of kilo-ohms). The disclosed PR can be used in the DC feedback loop of a capacitively coupled amplifier, enabling a bandwidth tuning range of 9 decades (mHz to MHz). Moreover, by using the pre-charge period to connect the gate of the PR transistor to ground, the amplifier settles in less than 1 μs, conforming with applications where electrodes/sensors with different nominal impedances are multiplexed to the amplifier input. The amplifier and the PR were validated in a 0.35 μm CMOS process, with post-layout simulations.

Principal Component Analysis-Based Occupancy Detection with Ultra Wideband Radar 1573
Zach Baird (Carleton University), Isuru Gunasekara (University of Ottawa), Miodrag Bolic (University of Ottawa), Sreeraman Rajan (Carleton University)

In this work we propose a threshold based algorithm which uses Principal Component Analysis (PCA) to determine room occupancy of up to two persons from Ultra WideBand radar returns. The average accuracy of the algorithm is 88% and is capable of correctly determining occupancy of two people when two subjects are standing only 0.8m apart.

Channel Equalization Techniques for Capacitive Proximity Communication 1577
Saber Amini (University of Toronto)

Capacitive couplers used in proximity communication suffer from large insertion loss due to the parasitic capacitances in the channel path. This paper proposes two active equalization techniques that reduce channel losses by 10 and 15 dB respectively using a 3 by 1.5 mm coupler allowing for smaller coupler size or lower BER.

A Late Adaptive Graph-Based Edge-Aware Filtering with Iterative Weight Updating Process 1581
Hamidreza Sadreazami (Concordia University), Amir Asif (Concordia University), Arash Mohammadi (Concordia University)

In this work, we propose a parallelized graph based framework for lowpass and highpass edge-aware filtering for detail manipulation (smoothening/boosting). Our proposed filter abstracts images through simplifying their visual content while preserving edges and emphasizing most of the perceptually important information. The proposed filtering framework is realized by using the graph similarity and Laplacian matrices to obtain smoothened image at each layer. The resulted smoothened images are iteratively treated as inputs to the next layer of the filtering framework and the weights are updated accordingly. The effectiveness of the proposed graph-based image abstraction method is verified through simulations. It is shown that the proposed method can yield better visual quality for abstracted images as compared to other existing works.

A Novel Approach Towards Less Area Overhead Self-Healing Hardware Systems 1585
Kasem Khalil (University of Louisiana at Lafayette), Omar K. Eldash (University of Louisiana at Lafayette), Magdy Bayoumi (University of Louisiana at Lafayette)

Self-healing digital systems has been a key approach towards reliable systems. It has been challenging for researchers to find an optimal scalable solution for it. Self-healing is based on redundancy by adding spare cells to replace faulty cells when needed for recovery which makes an area overhead. One of main problem in current self-healing approaches is area overhead because they are based on redundancy (spare blocks). This paper presents an idea for self-healing without using redundancy through embryonic hardware where each cell is a universal cell. Therefore, the area overhead will be lower compared to previous works. The idea is based on using every active block as a spare cell for its neighbor through time multiplexing. In case of faulty cell, the neighbor cell will run its task as well as the task of the faulty cell successively in one clock cycle. The area overhead of the proposed technique is shown to be much lower than compared other approaches relying on spare cells. The proposed solution provides 50\% chance of repairing.

Real-Time and Event-Triggered Object Detection, Recognition, and Tracking 1589
Désirée Blizzard (Concordia University), Somayeh Davar (Concordia University), Arash Mohammadi (Concordia University)

This paper presents the current state of a novel event-based surveillance framework for real-time detection and tracking of the person-of-interest with IP PTZ network camera. Formulating the problem in a (non-linear) Bayesian filtering framework in combination with Convolutional Neural Networks (CNN), we develop dynamical and adaptive approaches for identifying the Person-of-Interest(PoI) from its given signature. We identify the target as human or non-human then recognize the facial Histogram of Oriented Gradients (HOG) feature of the PoI to finally start tracking the PoI across the surveillance area covered by the IP PTZ network camera. In particular, this research work intends to incorporate and combine recently developed event-based tracking algorithms with deep learning algorithms and implement in a practical setting for real-time detection and tracking via a IP PTZ network camera.

Simplified Minimal Gated Unit Variations for Recurrent Neural Networks 1593
Joel C. Heck, Jr. (Michigan State University), Fathi M. Salem (Michigan State University)

Recurrent neural networks with various types of hidden units have been used to solve a diverse range of problems involving sequence data. Two of the most recent proposals, gated recurrent units (GRU) and minimal gated units (MGU), have shown comparable promising results on example public datasets. In this paper, we introduce three model variants of the minimal gated unit which further simplify that design by reducing the number of parameters in the forget-gate dynamic equation. These three model variants, referred to simply as MGU1, MGU2, and MGU3, were tested on sequences generated from the MNIST dataset and the real sequences from the Reuters Newswire Topics (RNT) dataset. Here, we report on the RNT results. The new models have shown similar accuracy to the MGU model while using fewer parameters and thus lower training expense. One model variant, namely MGU2, performed better than MGU on the datasets considered, and thus may be used as an alternate to MGU or GRU in recurrent neural networks.

Gate-Variants of Gated Recurrent Unit (GRU) Neural Networks 1597
Rahul Dey (Michigan State University), Fathi M. Salem (Michigan State University)

The paper evaluates three variants of the Gated Recurrent Unit (GRU) in recurrent neural networks (RNNs) by retaining the structure and systematically reducing parameters in the update and reset gates. We evaluate the three variant GRU models on MNIST and IMDB datasets and show that these GRU-RNN variant models perform as well as the original GRU RNN model while reducing the computational expense. In this comparative study, we simply refer to the three variants as, respectively, GRU1, GRU2, and GRU3 RNNs.

Simplified Gating in Long Short-Term Memory (LSTM) Recurrent Neural Networks 1601
Yuzhen Lu (Michigan State University), Fathi M. Salem (Michigan State University)

The standard LSTM recurrent neural networks while very powerful in long-range dependency sequence applications have highly complex structure and relatively large (adaptive) parameters. In this work, we present empirical comparison between the standard LSTM recurrent neural network architecture and three new parameter-reduced variants obtained by eliminating combinations of the input signal, bias, and hidden unit signals from individual gating signals. The experiments on two sequence datasets show that the three new variants, called simply as LSTM1, LSTM2, and LSTM3, can achieve comparable performance to the standard LSTM model with less (adaptive) parameters.

A 1 GS/s 6-Bit Time-Based Analog-to-Digital Converter (T-ADC) for Front-End Receivers 1605
Ali H. Hassan (Cairo University), Ahmed Ali (Cairo University), M. Wagih Ismail (University of Toronto), Mohamed Refky (Cairo University), Yehea Ismail (American University in Cairo), Hassan Mostafa (American University in Cairo)

Recently, researchers are targeting low-power consumption, and integrating more blocks on-chip. This paper proposes a 1GS/s 6-bit Time based Analog to Digital Converter (TADC) for front-end receivers. This T-ADC eliminates the preprocessing analog blocks, and reduces power consumption by removing the power-hungry sample and hold circuit. A prototype of the proposed T-ADC is implemented in 65nm CMOS technology, where it consumes 1 mW and achieves a maximum SNDR of 35.5 dB with sampling rate 1 GHZ that corresponds to a Figure of Merit (FoM) of 20.62 fJ/step.

Adaptive Data-Transition Decision Feedback Equalizer for Serial Links 1609
Yue Li (Ryerson University), Fei Yuan (Ryerson University)

Data-state decision feedback equalizers (DFEs) suffer from the fundamental drawback of deteriorating vertical eye-opening when consecutive 1s or 0s are present in data. To combat this, a new data-transition adaptive DFE is proposed. The proposed DFE is analyzed in both time and frequency domains. We show that the DFE does not reduce vertical eye-opening whereas data-state DFE shrinks vertical eye-opening when consecutive 1s or 0s are present. We further show that the proposed DFE not only offers a unity signal transfer function at low frequencies where most of the energy of data is located but also provides first-order shaping on the difference between the desired and equalized data. Both result in large vertical eye-opening. The details of the implementation of the proposed DFE are presented. The theoretical findings were validated using the simulation results of two serial links, one with data-state DFE with loop-unrolling and the other with the data-transition DFE designed in a TSMC 65 nm CMOS technology.

Progressive Fusion of Multi-Rate Motor Imagery Classification for Brain Computer Interfaces 1613
Tim Maloney (Concordia University), Golnar Kalantar (Concordia University), Arash Mohammadi (Concordia University)

Motivated by limited availability of training data for practical implementation of a synchronous Brain computer interface (BCI), the paper proposes a novel EEG-based framework consisting of two separate (partially coupled) filters running in parallel: (i) The Progressive Filter: An efficient but computationally extensive combination of feature extraction and classification that uses new arriving epochs to train in an offline fashion, and; (ii) The Active Filter: A simplified feature extraction approach running online based on pre-trained classifiers. The $\AF$ produces MI classification results at the end of each epoch while the Progressive Filter takes several epochs to perform processing, adaptation, and re-training tasks. Once the computation of the Progressive Filter is complete, the two filters are coupled to improve the real-time performance of the overall system.

Calculation of Voltage Gain Transfer Functions using Trajectance Analysis 1617
Sotoudeh Hamedi-Hagh (San Jose State University)

Numerator of the voltage gain transfer functions are directly derived with Trajectance analysis in this paper. Denominator of the voltage gain transfer functions are directly calculated by Suspendance analysis that was explained in prior publications. The voltage gain numerator is obtained by i) identifying all paths that connect the input node to output node of the circuit through sequential passive components and dependent active sources, ii) calculating the Suspendance of each path when the path segments are shorted to ground and iii) adding the products of path Trajectance and Suspendance together. The voltage gains of a four-node active MOSFET inductor are extracted and compared with numerical plots from Spice simulator to demonstrate the effectiveness of the Trajectance analysis.

Bio-Impedance Analysis for High-Speed and Wide-Band Application by using Pulse Stimulation 1621
Taehyoung Kim (Yonsei University), Gunhee Han (Yonsei University), Myungjin Han (Yonsei University)

Conventional bio-impedance analysis to estimate the body composition has been used for many bio applications. It has been commonly applied by a sinusoidal wave or wide-band frequency signal in current domain on the target tissue, and its measured response is processed for providing the impedances. These techniques, however, have common trade-off between detectable frequency range and data rate. For some applications both wide-band frequency detection and high-speed update rate are required. This paper presents a pulse stimulation technique for the bio-impedance analysis, which is proper to the high-speed and wide-band applications. The proposed method is proved by theoretical analysis. It is also verified with the simulation and measurement results.