Seoul, South Korea 15 – 20 October 2017



IEEE Catalog Number: ISBN:

CFP17CCS-POD 978-1-5090-6540-0

Copyright © 2017, Association for Computing Machinery (ACM) All Rights Reserved

*** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.

 IEEE Catalog Number:
 CFP17CCS-POD

 ISBN (Print-On-Demand):
 978-1-5090-6540-0

 ISBN (Online):
 978-1-4503-5184-3

ISSN: 2381-1560

Additional Copies of This Publication Are Available From:

Curran Associates, Inc 57 Morehouse Lane Red Hook, NY 12571 USA

Phone: (845) 758-0400 Fax: (845) 758-2633

Fax: (845) 758-2633 E-mail: curran@proceedings.com Web: www.proceedings.com



TABLE OF CONTENTS

CA1A.1 - Modular Compilation of Hybrid Systems for Emulation and Large Scale Simulation.....N/A *Avinash Malik, Partha Roop, Sidharta Andalam, Mark Trew, Michael Mendler* https://doi.org/10.1145/3126536

CA1A.2 - Complete and Practical Universal Instruction Selection.....N/A *Gabriel Hjort Blindell, Mats Carlsson, Roberto Castañeda Lozano, Christian Schulte* https://doi.org/10.1145/3126528

CA1A.3 - An Efficient WCET-Aware Instruction Scheduling and Register Allocation Approach for Clustered VLIW Processors.....N/A *Xuesong Su, Hui Wu, Jingling Xue* https://doi.org/10.1145/3126524

CA2A.1 - A Study of Dynamic Phase Adaptation Using a Dynamic Multicore Processor......N/A *Paul-Jules Micolet, Aaron Smith, Christophe Dubach* https://doi.org/10.1145/3126523

CA2A.2 - Implementation of Partitioned Mixed-Criticality Scheduling on a Multi-Core Platform.....N/A *Roman Trüb, Georgia Giannopoulou, Andreas Tretter, Lothar Thiele* https://doi.org/10.1145/3126533

CA2A.3 - DyPO: Dynamic Pareto Optimal Configuration Selection for Heterogeneous MpSoCs.....N/A *Ujjwal Gupta, Chetan Arvind Patil, Ganapati Bhat, Prabhat Mishra, Umit Ogras* https://doi.org/10.1145/3126530

CA3A.1 - A Quantifiable Approach to Approximate Computing (Special Session).....1

Chaofan Li, Deepashree Sengupta, Farhana Sharmin Snigdha, Wenbin Xu, Jiang Hu, Sachin S. Sapatnekar https://doi.org/10.1145/3125501.3125511

CA3A.2 - Quality-Configurable Memory Hierarchy through Approximation (Special Session).....3 *Majid Shoushtari, Amir M. Rahmani, Nikil Dutt* https://doi.org/10.1145/3125501.3125525

CA3A.3 - Hardware Approximate Computing: Why, How, When and Where (Special Session).....5 *Hassaan Saadat, Sri Parameswaran* https://doi.org/10.1145/3125501.3125518

TABLE OF CONTENTS

CA3A.4 - Probabilistic Reasoning for Analysis of Approximate Computations (Special Session).....N/A Sasa Misailovic

https://doi.org/10.1145/3125501.3125524

CA4A.1 - The CURE: Cluster Communication Using Registers.....N/A *Vignyan Reddy Kothinti Naresh, Dibakar Gope, Mikko Lipasti* https://doi.org/10.1145/3126527

CA4A.2 - An Out-of-Order Load-Store Queue for Spatial Computing.....N/A *Lana Josipovic, Philip Brisk, Paolo Ienne* https://doi.org/10.1145/3126525

CA4A.3 - Efficient Pulsed-Latch Implementation for Multiport Register Files (Work In Progress).....7 Wael M. Elsharkasy, Hasan Erdem Yantir, Amin Khajeh, Ahmed M. Eltawil, Fadi J. Kurdahi https://doi.org/10.1145/3125501.3125515

CA4A.4 - A "High Resilience" Mode to Minimize Soft Error Vulnerabilities in ARM Cortex-R CPU Pipelines (Work In Progress).....9 *Xabier Iturbe, Balaji Venu, John Penton, Emre Ozer*https://doi.org/10.1145/3125501.3125509

CA4A.5 - Balanced Cache Bypassing for Critical Warp Reduction (Work In Progress).....11 *Sungin Hong, Hyunjun Kim, Hwansoo Han* https://doi.org/10.1145/3125501.3125513

CA4A.6 - SSS: Self-aware System-on-chip using Static-dynamic Hybrid Method (Work In Progress).....13 *Gaoming Du, Shibi Ma, Zhenmin Li, Zhonghai Lu, Duoli Zhang, Yiming Ouyang, Minglun Gao* https://doi.org/10.1145/3125501.3125527

CA5A.1 - Diagonal Component Expansion for Flow-layer Placement of Flow-based Microfluidic Biochips.....N/A *Brian Crites, Karen Kong, Philip Brisk* https://doi.org/10.1145/3126529

CA5A.2 - Synthesis of Error-Recovery Protocols for Micro-Electrode-Dot-Array Digital Microfluidic Biochips.....N/A *Mahmoud Elfar, Zhanwei Zhong, Zipeng Li, Krishnendu Chakrabarty, Miroslav Pajic* https://doi.org/10.1145/3126538

TABLE OF CONTENTS

CA5A.3 - Incremental Training of CNNs for User Customization (Work In Progress).....15 *Mansureh S. Moghaddam, Barend Harris, Duseok Kang, Inpyo Bae, Euiseok Kim, Hyemi Min, Hansu Cho, Sukjin Kim, Bernhard Egger, Soonhoi Ha, Kiyoung Choi* https://doi.org/10.1145/3125501.3125519

CA5A.4 - Prediction based Convolution Neural Network Acceleration (Work In Progress).....17 *Yuan Yao, Zhonghai Lu* https://doi.org/10.1145/3125501.3125523

CA5A.5 - Optimizing DCNN FPGA Accelerator Design for Handwritten Hangul Character Recognition (Work In Progress).....19

Hanwool Park, Changdae Lee, Hakkyung Lee, Yechan Yoo, Yoonjin Park, Injung Kim, Kang Yi https://doi.org/10.1145/3125501.3125522

CA5A.6 - A High-performance FPGA Accelerator for Sparse Neural Networks (Work In Progress).....21 *Yuntao Lu, Lei Gong, Chongchong Xu, Fan Sun, Yiwei Zhang, Chao Wang, Xuehai Zhou* https://doi.org/10.1145/3125501.3125510

IoT5D.1 - Low-Cost Memory Fault Tolerance for IoT Devices.....N/A *Mark Gottscho, Irina Alam, Clayton Schoeny, Lara Dolecek, Puneet Gupta* https://doi.org/10.1145/3126534

IoT5D.3 - Towards Industry Strength Mapping of AUTOSAR\\Automotive Functionality on Multicore Architectures (Work In Progress).....23 *Cosmin Avasalcai, Dhanesh Budhrani, Paul Pop*https://doi.org/10.1145/3125501.3125623

CA6A.1 - Approximate Memristive In-memory Computing.....N/A *Hasan Erdem Yantır, Ahmed M. Eltawil, Fadi Kurdahi* https://doi.org/10.1145/3126526

CA6A.2 - QLUT: Input-Aware Quantized Table Lookup for Energy-Efficient Approximate Accelerators.....N/A *Arnab Raha, Vijay Raghunathan* https://doi.org/10.1145/3126531

CA6A.3 - Code-Size-Aware Mapping for Synchronous Dataflow Graphs on Multicore Systems (Work In Progress).....25 *Mingze Ma, Rizos Sakellariou*https://doi.org/10.1145/3125501.3125514

TABLE OF CONTENTS

CA6A.4 - Multi-Grained Performance Estimation for MPSoC Compilers (Work In Progress).....27 *Miguel Angel Aguilar, Abishek Aggarwal, Awaid Shaheen, Rainer Leupers, Gerd Ascheid, Jeronimo Castrillon, Liam Fitzpatrick* https://doi.org/10.1145/3125501.3125521

CA6A.5 - REDEFINE - A Case for WCET-friendly Hardware Accelerators for Real time Applications (Work In Progress).....29

Kavitha Madhu, Tarun Singla, S K Nandy, Ranjani Narayan, Francois Neumann, Philippe Baufreton https://doi.org/10.1145/3125501.3125526

CA6A.6 - Advanced Ahead-of-Time Compilation for JavaScript Engine (Work In Progress).....31 *HyukWoo Park, SungKook Kim, Soo-Mook Moon* https://doi.org/10.1145/3125501.3125512

CA7A.1 - Emerging (Un-)Reliability Based Security Threats and Mitigations for Embedded Systems (Special Session).....33

Hussam Amrouch, Prashanth Krishnamurthy, Naman Patel, Jörg Henkel, Ramesh Karri, Farshad Khorrami

https://doi.org/10.1145/3125501.3125529

CA8A.1 - User-aware Frame Rate Management in Android Smartphones.....N/A

Begum Birsen Egilmez, Matthew Schuchhardt, Gokhan Memik, Raid Ayoub, Niranjan Soundararajan,

Michael Kishinevsky

https://doi.org/10.1145/3126539

CA8A.2 - FlowPaP and FlowReR: Improving Energy Efficiency and Performance for STT-MRAM-Based Handheld Devices Under Read Disturbance.....N/A *Hao Yan, Lei Jiang, Lide Duan, Wei-Ming Lin, Eugene John* https://doi.org/10.1145/3126532

CA8A.3 - Towards Efficient Quantized Neural Network Inference on Mobile Devices (Work In Progress).....43 *Yaman Umuroglu, Magnus Jahre* https://doi.org/10.1145/3125501.3125528

CA8A.4 - Improving NVMe SSD I/O Determinism with PCIe Virtual Channel (Work In Progress).....45 *Seonbong Kim, Joon-Sung Yang* https://doi.org/10.1145/3125501.3125520

TABLE OF CONTENTS

CA8A.5 - Enabling NVM-Based Deep Learning Acceleration Using Nonuniform Data -Quantization (Work In Progress).....47

Hao Yan, Ethan C. Ahn, Lide Duan

https://doi.org/10.1145/3125501.3125516

CA8A.6 - Enabling Reliable Main Memory Using STT-MRAM via Restore-Aware Memory Management (Work In Progress).....49 *Armin Haj Aboutalebi, Lide Duan*https://doi.org/10.1145/3125501.3125517

CA9A.1 - Using Criticality of GPU Accesses in Memory Management for CPU-GPU Heterogeneous Multicore Processors.....N/A

Siddharth Rai, Mainak Chaudhuri

https://doi.org/10.1145/3126540

CA9A.2 - Reinforcement Learning-Assisted Garbage Collection to Mitigate Long Tail Latency Problem in SSD.....N/A *Wonkyung Kang, Dongkun Shin, Sungjoo Yoo*https://doi.org/10.1145/3126537

CA9A.3 - Minimising Access Conflicts on Shared Multi-Bank Memory.....N/A *Andreas Tretter, Georgia Giannopoulou, Matthias Baer, Lothar Thiele* https://doi.org/10.1145/3126535