2017 Fifth Berkeley Symposium on Energy Efficient Electronic Systems & Steep Transistors Workshop (E3S 2017)

Berkeley, California, USA
19-20 October 2017

IEEE Catalog Number: CFP17E3S-POD
ISBN: 978-1-5386-3291-8

IEEE Catalog Number:	CFP17E3S-POD
ISBN (Print-On-Demand):	978-1-5386-3291-8
ISBN (Online):	978-1-5386-3290-1

Additional Copies of This Publication Are Available From:

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Red Hook, NY 12571 USA
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Paolo Gargini (IRDS, USA) invited

104 *Sub-unity Body Factor: The Next CMOS and Beyond CMOS Technology Booster for Enhanced Energy Efficiency?*
A. Ionescu (Ecole Polytechnique Fédérale Lausanne, Switzerland) invited

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S. Mitra (Stanford University, USA) *invited*

90 *Standby-Power-Free Integrated Circuits Using MTJ-Based VLSI Computing for IoT Applications*
T. Hanyu (Tohoku University, Japan) *invited*

N/A *Keynote Presentation: "Building a Platform for AI"*
A. Khosrowshahi (Intel Corporation, USA) *invited keynote*

107 *Memristive Boltzmann Machine: A Hardware Accelerator for Combinatorial Optimization and Deep Learning*
E. Ipek (University of Rochester, USA) and M. N. Bojnordi (University of Utah, USA) *invited*

N/A *Advance of Steep Transistors*
A. Seabaugh (University of Notre Dame, USA) *invited*

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99 *Steep Switch with Hybrid Operation Mechanism for Performance Improvement*
R. Huang, Q.Huang, Y.Zhao, C. Chen, R. Jia, L. Guo and Y. Wang (Peking University, China) *invited*

N/A *Modeling the Influence of Dielectric Interface Traps on I-V Characteristics of TFETs*
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