2017 IEEE 24th International Conference on High Performance Computing (HiPC 2017)

Jaipur, India 18 – 21 December 2017



IEEE Catalog Number: ISBN:

CFP17176-POD 978-1-5386-2294-0

Copyright © 2017 by the Institute of Electrical and Electronics Engineers, Inc. All Rights Reserved

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved.

*** This is a print representation of what appears in the IEEE Digital Library. Some format issues inherent in the e-media version may also appear in this print version.

IEEE Catalog Number:	CF
ISBN (Print-On-Demand):	978
ISBN (Online):	978
ISSN:	109

CFP17176-POD 978-1-5386-2294-0 978-1-5386-2293-3 1094-7256

Additional Copies of This Publication Are Available From:

Curran Associates, Inc 57 Morehouse Lane Red Hook, NY 12571 USA Phone: (845) 758-0400 Fax: (845) 758-2633 E-mail: curran@proceedings.com Web: www.proceedings.com



2017 IEEE 24th International Conference on High Performance Computing HiPC 2017

Table of Contents

Message from the General and Vice-General Chairs	xi
Message from the Program Chair	xiii
Message from the Steering Chair	xv
HiPC 2017 Committees	
HiPC 2017 Technical Program	xxi

Keynote 1

End of Moore's Law: Or, a Computer Architect's Mid-life Crisis	?
Parthasarathy Ranganathan (Google)	

Technical Session 1: Graph Algorithms

Exact and Parallel Triangle Counting in Dynamic Graphs
Shared-Memory Graph Truss Decomposition
Humayun Kabir (The Pennsylvania State University) and Kamesh Madduri (The Pennsylvania State University)
Approximate Computing Techniques for Iterative Graph Algorithms
Ajay Panyala (Pacific Northwest National Laboratory), Omer Subasi
(Pacific Northwest National Laboratory), Mahantesh Halappanavar
(Pacific Northwest National Laboratory), Ananth Kalyanaraman (Washington State University), Daniel Chavarría-Miranda (Trovares
Inc.), and Sriram Krishnamoorthy (Pacific Northwest National
Laboratory)
Scalable Exact Parent Sets Identification in Bayesian Networks Learning with Apache Spark
Parallel Exact Dynamic Bayesian Network Structure Learning with Application to Gene Networks

Technical Session 2: Architecture and Communication

 Designing Registration Caching Free High-Performance MPI Library with Implicit On-Demand Paging (ODP) of InfiniBand
Last Level Collective Hardware Prefetching For Data-Parallel Applications
 Kernel-Assisted Communication Engine for MPI on Emerging Manycore Processors
 Support for Power Efficient Proactive Cooling Mechanisms
Redundant Arithmetic Based High Speed Carry Free Hybrid Adders with Built-In Scan Chain on FPGAs 104 Ayan Palchaudhuri (Indian Institute of Technology Kharagpur) and Anindya Sundar Dhar (Indian Institute of Technology Kharagpur)
ConvLight: A Convolutional Accelerator with Memristor Integrated Photonic Computing

Technical Session 3: Algorithms

Provably Efficient Scheduling of Dynamically Allocating Programs on Parallel Cache Hierarchies	24
Further Explorations in State-Space Search for Optimal Task Scheduling 1	34
Michael Orr (University of Auckland) and Oliver Sinnen (University of	
Auckland)	
A Novel Approach for Job Scheduling Optimizations Under Power Cap for ARM and Intel HPC Systems 1	42
Dineshkumar Rajagopal (Bull Atos Technologies), Daniele Tafani	
(Leibniz Supercomputing Centre), Yiannis Georgiou (Bull Atos	
Technologies), David Glesser (Bull Atos Technologies), and Michael Ott	
(Leibniz Supercomputing Centre)	

A Memory Congestion-Aware MPI Process Placement for Modern NUMA Systems	152
Mulya Agung (Tohoku University), Muhammad Alfian Amrizal (Tohoku	
University), Kazuhiko Komatsu (Tohoku University), Ryusuke Egawa	
(Tohoku University), and Hiroyuki Takizawa (Tohoku University)	
Expander: Lock-Free Cache for a Concurrent Data Structure Pooja Aggarwal (IBM Research Labs Bangalore) and Smruti R. Sarangi (IIT Delhi India)	162
Adaptive Code Refinement: A Compiler Technique and Extensions to Generate Self-Tuning Applications Maxime Schmitt (University of Strasbourg, INRIA), Philippe Helluy (University of Strasbourg, INRIA), and Cédric Bastoul (University of Strasbourg)	172

Keynote 2

Machine Learning @ Amazon	
Rajeev Rastogi (Amazon)	

Technical Session 4: Big Data, Machine Learning and Optimization

Parallel Deep Convolutional Neural Network Training by Exploiting the Overlapping of Computation and Communication	. 183
Parallel Dynamic Data Driven Approaches for Synthetic Aperture Radar	. 193
ARM Wrestling with Big Data: A Study of Commodity ARM64 Server for Big Data Workloads Jayanth Kalyanasundaram (Indian Institute of Science) and Yogesh Simmhan (Indian Institute of Science)	203
MPI-LiFE: Designing High-Performance Linear Fascicle Evaluation of Brain Connectome with MPI Shashank Gugnani (The Ohio State University), Xiaoyi Lu (The Ohio State University), Franco Pestilli (Indiana University), Cesar Caiafa (Indiana University), and Dhabaleswar K. (DK) Panda (The Ohio State University)	213
Reducing Network Congestion and Synchronization Overhead During Aggregation of Hierarchical Data Sidharth Kumar (SCI, University of Utah), Duong Hoang (SCI, University of Utah), Steve Petruzza (SCI, University of Utah), John Edwards (Idaho State University), and Valerio Pascucci (SCI, University of Utah)	. 223
Fast Parallel Randomized QR with Column Pivoting Algorithms for Reliable Low-Rank Matrix Approximations Jianwei Xiao (UC Berkeley), Ming Gu (UC Berkeley), and Julien Langou (University of Colorado Denver)	.233

Technical Session 5: Graph Algorithms and GPU

An X10-Based Distributed Streaming Graph Database Engine Miyuru Dayarathna (WSO2 Inc. / JST CREST), Sathya Bandara (University of Moratuwa), Nandula Jayamaha (University of Moratuwa), Mahen Herath (University of Moratuwa), Achala Madhushan (University of Moratuwa), Sanath Jayasena (University of Moratuwa), and Toyotaro Suzumura (IBM T.J. Watson Research Center)	243
GPU-Centric Communication on NVIDIA GPU Clusters with InfiniBand: A Case Study with OpenSHMEM Sreeram Potluri (NVIDIA Corporation), Anshuman Goswami (NVIDIA Corporation), Davide Rossetti (NVIDIA Corporation), C.J. Newburn (NVIDIA Corporation), Manjunath Gorentla Venkata (Oak Ridge National Laboratory), and Neena Imam (Oak Ridge National Laboratory)	253
Distributed Algorithm for High-Utility Subgraph Pattern Mining Over Big Data Platforms Alind Khare (IIIT-D), Vikram Goyal (IIIT-Delhi), Srikanth Baride (IIIT-Delhi), Sushil K. Prasad (Georgia State University), Michael McDermott (Georgia State University), and Dhara Shah (Georgia State University)	263
ReCALL: Reordered Cache Aware Locality Based Graph Processing Kartik Lakhotia (University of Southern California), Shreyas Singapura, Rajgopal Kannan (US Army Research Lab), and Viktor Prasanna (University of Southern California)	273
 Characterization of Data Movement Requirements for Sparse Matrix Computations on GPUs Süreyya Emre Kurt (The Ohio State University), Vineeth Thumma (The Ohio State University), Changwan Hong (The Ohio State University), Aravind Sukumaran-Rajam (The Ohio State University), and P. Sadayappan (The Ohio State University) 	283
Applying Graph Analytics to Understand Compute Core Usage and Publication Trends in a Petascale Supercomputing Facility Sangkeun Lee (Oak Ridge National Laboratory), Sudharshan S. Vazhkudai (Oak Ridge National Laboratory), and Raghul Gunasekaran (Oak Ridge National Laboratory)	294

Keynote 3

Computing Just What You Need: Online Data Analysis and Reduction at Extreme Scales	306
Ian Foster (Argonne National Lab and University of Chicago)	

Technical Session 6: System Software

 Enabling Dependability-Driven Resource Use and Message Log-Analysis for Cluster System Diagnosis
Context-Aware Memory Profiling for Speculative Parallelism
Lifting Barriers Using Parallel Polyhedral Regions
Exploiting Common Neighborhoods to Optimize MPI Neighborhood Collectives
 Efficient Fork-Join on GPUs Through Warp Specialization

Technical Session 7: GPU Frameworks and Applications

Thrust++: Extending Thrust Framework for Better Abstraction and Performance Ajai V. George (BITS Pilani KK Birla Goa Campus), Sankar Manoj (BITS Pilani KK Birla Goa Campus), Sanket R. Gupte (BITS Pilani KK Birla Goa Campus), Sayantan Mitra (Siemens Technology & Services Pvt Ltd., Bangalore, India), and Santonu Sarkar (BITS Pilani KK Birla Goa Campus)	368
A Novel Implementation of 2D3V Particle-in-Cell (PIC) Algorithm for Kepler GPU Architecture Harshil Shah (DA-IICT, Gandhinagar), Siddharth Kamaria (DA-IICT, Gandhinagar), Riddhesh Markandeya (DA-IICT, Gandhinagar), Miral Shah (DA-IICT, Gandhinagar), and Bhaskar Chaudhury (DA-IICT, Gandhinagar)	378
 Parallelizing Hines Matrix Solver in Neuron Simulations on GPU Dharma Teja Vooturi (International Institute of Information Technology - Hyderabad), Kishore Kothapalli (International Institute of Information Technology - Hyderabad), and Upinder Singh Bhalla (National Center for Biological Sciences - Tata Institute of Fundamental Research.) 	388

Building Halo Merger Trees from the Q Continuum Simulation	. 398
Esteban Rangel (Northwestern University), Nicholas Frontiere	
(University of Chicago), Salman Habib (Argonne National Laboratory),	
Katrin Heitmann (Argonne National Laboratory), Wei-keng Liao	
(Northwestern University), Ankit Agrawal (Northwestern University),	
and Alok Choudhary (Northwestern University)	
A Memory-Efficient GPU Method for Hamming and Levenshtein Distance Similarity	. 408
Andrew Todd (University of Missouri), Marziyeh Nourian (North Carolina	
State University), and Michela Becchi (North Carolina State	
University)	

Author Index	 	 419
Author Index	 	 41