

---

# Silicon Compatible Materials, Processes, and Technologies for Advanced Integrated Circuits and Emerging Applications 3

---

## Editors:

### **F. Roozeboom**

Eindhoven University of Technology,  
and TNO Technical Sciences  
Eindhoven, The Netherlands

### **K. Kakushima**

Tokyo Institute of Technology  
Yokohama, Kanagawa, Japan

### **D.-L. Kwong**

Institute of Microelectronics  
Singapore

### **E. P. Gusev**

Qualcomm Technologies, Inc.  
Santa Clara, California, USA

### **V. Narayanan**

IBM T. J. Watson Research Center  
Yorktown Heights, New York, USA

### **H. Iwai**

Tokyo Institute of Technology  
Yokohama, Kanagawa, Japan

### **P. J. Timans**

Mattson Technology, Inc.  
Fremont, California, USA

## Sponsoring Divisions:



**Electronics and Photonics**



**Dielectric Science & Technology**



Published by

**The Electrochemical Society**

65 South Main Street, Building D  
Pennington, NJ 08534-2839, USA

tel 609 737 1902

fax 609 737 2743

[www.electrochem.org](http://www.electrochem.org)

**ecstransactions**™

**Vol. 53, No. 3**

---

Copyright 2013 by The Electrochemical Society.  
All rights reserved.

This book has been registered with Copyright Clearance Center.  
For further information, please contact the Copyright Clearance Center,  
Salem, Massachusetts.

Published by:

The Electrochemical Society  
65 South Main Street  
Pennington, New Jersey 08534-2839, USA

Telephone 609.737.1902  
Fax 609.737.2743  
e-mail: [ecs@electrochem.org](mailto:ecs@electrochem.org)  
Web: [www.electrochem.org](http://www.electrochem.org)

ISSN 1938-6737 (online)  
ISSN 1938-5862 (print)  
ISSN 2151-2051 (cd-rom)

ISBN 978-1-62332-025-6 (Softcover)  
ISBN 978-1-60768-376-6 (PDF)

Printed in the United States of America.

---

***ECS Transactions, Volume 53, Issue 3***

Silicon Compatible Materials, Processes, and Technologies for Advanced Integrated Circuits and Emerging Applications 3

**Table of Contents**

*Preface* *iii*

**Chapter 1  
Welcome and Plenary Session**

(Keynote) III-V Compound Semiconductor Field Effect Transistors for Low Power Digital Logic 3  
*S. Datta, A. V. Thathachary, L. Liu, E. Hwang, A. Agrawal, N. Agrawal*

**Chapter 2  
Planar Si and SiGe: Stressors/Gate Stack**

(Invited) The Past, Present and Future of High-k/Metal Gates 17  
*K. Choi, T. Ando, E. A. Cartier, A. Kerber, V. Paruchuri, J. Iacoponi, V. Narayanan*

Investigation of Embedded SiGe Source/Drain for 28nm HKMG PFET Performance Enhancement 27  
*E. M. Bazizi, A. Zaka, G. Dillaway, B. Bai, M. Wiatr, F. Benistant, M. Horstmann*

Si-Passivation of Epitaxial SiGe: Kinetics and Impact on Morphology 33  
*B. Seiss, D. Dutartre*

Very Low Electron Density in Undoped Enhancement-Mode Si/SiGe Two-Dimensional Electron Gases with Thin SiGe Cap Layers 45  
*C. T. Huang, J. Y. Li, J. C. Sturm*

Evaluation of Stress Induced by Plasma Assisted ALD SiN Film 51  
*K. Nagata, M. Nagasaka, T. Yamaguchi, A. Ogura, H. Oji, J. Y. Son, I. Hirose, Y. Watanabe, Y. Hirota*

### Chapter 3 High Mobility Channels

(Invited) The Materials Integration of Ge and $\text{In}_x\text{Ga}_{1-x}\text{As}$ on Si Template for Next Generation CMOS Applications <i>E. Y. Chang, S. H. Tang, Y. C. Lin</i>	59
(Electronics & Photonics Division Award Presentation) Si-SiO <sub>2</sub> Interface to High-K-Ge/III-V Interface: Passivation and Reliability <i>D. Misra</i>	69
(Invited) III-V/Ge CMOS Device Technologies for High Performance Logic Applications <i>S. Takagi, M. Yokoyama, S. H. Kim, R. Zhang, R. Suzuki, N. Taoka, M. Takenaka</i>	85
(Invited) A Brief Review of Doping Issues in III-V Semiconductors <i>K. S. Jones, A. G. Lind, C. Hatem, S. Moffatt, M. C. Ridgeway</i>	97
Limiting Factors of Channel Mobility in III-V/Ge MOSFETs <i>S. Takagi, S. H. Kim, R. Zhang, N. Taoka, M. Yokoyama, M. Takenaka</i>	107

### Chapter 4 Non-Planar Devices: FINFETS/Nanowires

(Invited) Strain-Enhanced Performance of Si-Nanowire FETs <i>M. Cassé, S. Barraud, R. Coquand, M. Koyama, D. Cooper, C. Vizios, C. Comboroure, P. Perreau, V. Maffini-Alvaro, C. Tabone, L. Tosti, S. Barnola, V. Delaye, F. Aussenac, G. Ghibaudo, H. Iwai, G. Reimbold</i>	125
Deposited ALD SiO <sub>2</sub> High-k/Metal Gate Interface for High Voltage Analog and I/O Devices on Next Generation Alternative Channels and FINFET Device Structures <i>S. Siddiqui, M. M. Chowdhury, M. Brodsky, N. Rahim, M. Dai, S. Krishnan, S. Fugardi, E. Wu, A. Chou, S. Narasimha, J. Li, K. Mestay, B. Linder, E. Maciejewski, R. Rettmann, S. Mittl, U. Kwon, V. Narayanan, W. Henson, D. Schepis, M. Chudzik</i>	137
Defect Characterization of ALD Grown SiO <sub>2</sub> Films: A Systematic Approach <i>F. L. Pasquale, S. Swaminathan, H. Kang, A. Lavoie</i>	147

## Chapter 5 Patterning and Lithography Challenges

A Study of Polysilicon Gate Etch Uniformity in 300 mm Silicon Wafers <i>W. S. Lau, P. Yang, S. Y. Siah</i>	161
Visualization of Plasma Etching Damage of Si Using Room Temperature Spectroscopic Photoluminescence <i>S. K. Jang Jian, C. C. Jeng, T. C. Wang, C. M. Huang, Y. L. Wang, W. S. Yoo</i>	167
On the Optimization of Ebeam Lithography Using Hydrogen Silsesquioxane (HSQ) for Innovative Self-Aligned CMOS Process <i>R. Coquand, S. Monfray, J. Pradelles, L. Martin, M. P. Samson, J. Bustos, S. Barraud, F. Boeuf, T. Skotnicki, G. Ghibaudo, T. Poiroux, O. Faynot</i>	177

## Chapter 6 Si Channel: Gate Stack Reliability

(Invited) Metal Gate/High- $\kappa$ Dielectric Gate Stack Reliability; or How I Learned to Live with Trappy Oxides <i>B. P. Linder, E. A. Cartier, S. Krishnan</i>	187
Impact of Lanthanum on Positive-Bias Temperature Instability – Insight from First-Principles Simulation <i>C. Gu, D. S. Ang</i>	193
On the Evolution of Switching Oxide Traps in the HfO <sub>2</sub> /TiN Gate Stack Subjected to Positive- and Negative-Bias Temperature Stressing <i>Y. Gao, D. S. Ang, C. J. Gu</i>	205

## Chapter 7 3D Integration/ReRAM/MEMS

Adjustable Switching Voltage Via Sol-Gel Derived and Ag In Situ Doped SiO <sub>2</sub> Thin Films for ReRAM <i>Y. P. Hsiao, W. L. Yang, Y. H. Lin, Y. C. Yang, C. C. Hsu, C. L. Peng, C. H. Liao, F. T. Chin, S. H. Liu, Y. M. Chang, L. M. Lin</i>	223
--	-----

On the Resistive Switching and Current Conduction Mechanisms of Amorphous LaGdO <sub>3</sub> Films Grown by Pulsed Laser Deposition <i>P. Misra, S. P. Pavunny, R. S. Katiyar</i>	229
(Invited) Challenges in 3D Integration <i>M. Koyanagi, K. W. Lee, T. Fukushima, T. Tanaka</i>	237
InP-Si BiCMOS Heterointegration Using a Substrate Transfer Process <i>M. Lisker, A. Trusch, A. Krüger, M. Fräschke, P. Kulse, Y. Borokhovich, B. Tillack, I. Ostermay, T. Krämer, A. Thies, O. Krüger, F. J. Schmückle, V. Krozer, W. Heinrich</i>	245
(Invited) Commercial CMOS-Integrated RF-MEMS <i>A. Morris, S. Cunningham</i>	255
Author Index	265