

---

# Silicon-on-Insulator Technology and Devices 14

---

## Editors:

### Y. Omura

Kansai University  
Osaka, Japan

### S. Cristoloveanu

IMEP-INPG-Grenoble  
Grenoble, France

### F. Gámiz

University of Granada  
Granada, Spain

### B-Y. Nguyen

SOITEC USA  
Bernin, France

## Sponsoring Division:



**Electronics and Photonics**



Published by

**The Electrochemical Society**

65 South Main Street, Building D  
Pennington, NJ 08534-2839, USA

tel 609 737 1902

fax 609 737 2743

[www.electrochem.org](http://www.electrochem.org)

**ecstransactions**™

**Vol. 19 No. 4**

---

Copyright 2009 by The Electrochemical Society.  
All rights reserved.

This book has been registered with Copyright Clearance Center.  
For further information, please contact the Copyright Clearance Center,  
Salem, Massachusetts.

Published by:

The Electrochemical Society  
65 South Main Street  
Pennington, New Jersey 08534-2839, USA

Telephone 609.737.1902  
Fax 609.737.2743  
e-mail: [ecs@electrochem.org](mailto:ecs@electrochem.org)  
Web: [www.electrochem.org](http://www.electrochem.org)

ISSN 1938-6737 (online)  
ISSN 1938-5862 (print)

Printed in the United States of America.

---

## Table of Contents

*Preface* *iii*

### **Chapter 1** **Plenary Talks**

SOI Technology Driving the 21st Century Ubiquitous Electronics 3  
*G. K. Celler*

Impact of Confinement of Semiconductor and Band Engineering on Future 15  
Device Performance  
*V. Sverdlov, O. Baumgartner, T. Windbacher, F. Schanovsky and S. Selberherr*

### **Chapter 2** **Materials and Characterization I**

Copper Decoration Combined with Preferential Etching for Delineation of Crystal 29  
Defects in SOI and sSOI Materials  
*H. Idrisi, M. Pejic, F. Uzelli and B. Kolbesen*

Simulation and Characterization of the Strain Induced by an Original "Embedded 37  
Buried Nitride" Technique  
*S. Baudot, F. Andrieu, M. Kostrzewa, J. Widiez, J. Barbe, O. Faynot,  
Y. Lamrani, C. Vizios, L. Brevard, H. Denis, V. Delaye, F. Rieutord and  
J. Eymery*

### **Chapter 3** **Device Technology I**

Advanced FinFET Devices for Sub-32nm Technology Nodes: Characteristics and 45  
Integration Challenges \*  
*A. Veloso, N. Collaert, A. De Keersgieter, L. Witters, R. Rooyackers,  
M. J. van Dal, R. Duffy, B. J. Pawlak, R. J. Lander, T. Hoffmann,  
S. Biesemans and M. Jurczak*

Ultra Compact FDSOI Transistors including Strain and Orientation: Processing and Performance *	55
<i>C. Fenouillet-Beranger, L. Pham Nguyen, P. Perreau, S. Denorme, F. Andrieu, O. Faynot, L. Tosti, L. Brevard, C. Buj, O. Weber, C. Gallon, V. Fiori, F. Boeuf, S. Cristoloveanu and T. Skotnicki</i>	
Impact of New Approach to Improve MOSFETs Performance with Ultrathin Gate Insulator	65
<i>W. Cheng, A. Teramoto and T. Ohmi</i>	
Process and Characterization of Hybrid-Oriented Complementary Single-Crystal Si Thin-Film Transistors on A Plastic Substrate	71
<i>H. Pang, G. K. Celler and Z. Ma</i>	

#### **Chapter 4 Materials and Characterization II**

SOI and Other Semiconductor-On-Insulator Substrates Characterization *	79
<i>A. Abbadie, Y. -M. Le Vaillant, C. Figuet and E. Guiot</i>	
Morphological and Electrical Comparison of GeOI Enriched Structures Obtained from SOI and sSOI Substrates	93
<i>J. Damlencourt, B. Vincent, L. Clavelier, C. Le Royer, Y. Campidelli, S. Bernasconi, Y. Morand, T. Nguyen and S. Cristoloveanu</i>	

#### **Chapter 5 Device Physics and Modeling I**

Comparison of SOI FinFETs and Bulk FinFETs *	101
<i>J. Lee, J. Lee, H. Jung and B. Choi</i>	
Mechanisms that Explain Short-Channel Effects of Sub-50-nm-Channel Ultra-Thin Symmetric Double-Gate SOI MOSFET	113
<i>Y. Omura and Y. Tahara</i>	

## **Chapter 6** **Device Physics and Modeling II**

Advanced Design Methodology of High-Performance Sub-100-nm-Channel GAA MOSFET <i>S. Nakano, O. Hayashi, Y. Omura, S. Yamakawa and H. Wakabayashi</i>	121
Comparison of the Electrostatics of Bulk and SOI Trigate MOSFETs <i>F. G. Ruiz, A. Godoy, I. Tienda-Luna and F. Gamiz</i>	127
Gate Stack Influence on GIFBE in nFinFETs <i>J. A. Martino, M. Rodrigues, A. Mercha, E. Simoen, A. Veloso, N. Collaert, M. Jurczak and C. Claeys</i>	133
Analytical Modeling of Double Gate Graded-Channel SOI Transistors for Analog Applications <i>F. A. Ferreira, A. Cerdeira, D. Flandre and M. Pavanello</i>	139
Low-Temperature Measurements on Germanium-on-Insulator pMOSFETs: Evaluation of the Background Doping Level and Modeling of the Threshold Voltage Temperature Dependence <i>W. Van Den Daele, E. Augendre, K. Romanjek, C. Le Royer, L. Clavelier, J. Damlencourt, E. Guiot, B. Ghyselen and S. Cristoloveanu</i>	145
The Wave SOI MOSFET: A New Accuracy Transistor Layout to Improve Drain Current and Reduce Die Area for Current Drivers Applications <i>S. P. Gimenez</i>	153

## **Chapter 7** **Device Technology II**

SOI as Platform for Transition from Micro to Nano * <i>F. Balestra</i>	161
Optimization of Blue/UV Sensors Using PIN Photodiodes in Thin-Film SOI Technology <i>O. Bulteel and D. Flandre</i>	175
A Wide Range Temperature Sensor Using SOI Technology <i>R. Patterson, M. E. Elbuluk and A. Hammoud</i>	181

## **Chapter 8** **Device Process Technology**

Diamond-on-SOI Field Emission Device Patterning <i>X. C. LeQuan, B. Choi, W. Kang and J. Davidson</i>	189
H-shaped Vertical Polycrystalline Silicon Thin Film Transistor on Insulator <i>H. Toure, T. Gaillard, N. Coulon and O. A. Bonnaud</i>	195
Issues Associated to Rare Earth Silicide Integration in Ultra Thin FD SOI Schottky Barrier nMOSFETs <i>G. Larrieu, D. A. Yarekha, E. Dubois, D. Deresmes, N. Breil, N. Reckinger, X. Tang and A. Halimaoui</i>	201

## **Chapter 9** **Simulations for Nano-scale SOI Devices I**

Device Physics and Simulation Techniques for Nanoscale SOI-MOSFETs * <i>H. Tsuchiya, Y. Yamada, S. Souma and M. Ogawa</i>	211
Analytical Model for Conduction Band Nonparabolicity to Transport Analysis of Nano-Scale SOI MOSFET <i>Y. Omura</i>	221

## **Chapter 10** **Simulations for Nano-scale SOI Devices II**

Three-Dimensional NEGF Simulations of Constriction Tunnel Barrier Silicon Nanowire MUGFETs <i>A. Afzaljan, C. Lee, R. Yan, N. Dehdashti Akhavan, C. Colinge and J. Colinge</i>	229
Simulation of Hole Mobility in DGSOI Transistors <i>L. Donetti, F. Gamiz, F. Garcia Ruiz, N. Rodriguez and A. Godoy</i>	235

## **Chapter 11** **Circuit Technology I**

Floating-Body SOI Memory: Concepts, Physics and Challenges * <i>M. Bawedin, S. Cristoloveanu, D. Flandre and F. Udrea</i>	243
--	-----

65nm Low Power (LP) SOI Technology on High Resistivity (HR) Substrate for WLAN and Mmwave SOCs 257  
*C. Raynaud, S. Haendler, G. Guegan, F. Giancesello, B. Martineau, P. Touret and N. Planeau*

Performance of Common-Source, Cascode and Wilson Current Mirrors Implemented with Graded-Channel SOI nMOSFETs in a Wide Temperature Range 265  
*M. de Souza, D. Flandre and M. Pavanello*

## **Chapter 12 Circuit Technology II**

Highly Reliable SRAM Circuit Technology Using FinFETs \* 273  
*S. Ouchi, K. Endo, T. Matsukawa, Y. Liu, Y. Ishikawa, J. Tsukada, H. Yamauchi, K. Sakamoto and M. Masahara*

Optimizing Spacer-to-Straggle Ratio in Underlap Double Gate MOSFETs for Low Voltage Analog and Digital Circuits 283  
*A. Kranti, R. Rashmi and G. Armstrong*

Harmonic Distortion Analysis of SOI Triple Gate FinFETs Applied to 2-MOS Balanced Structures 289  
*R. T. Doria, J. A. Martino, A. Cerdeira and M. Pavanello*

## **Chapter 13 Device Technology III**

Comparison of Short-Channel Effects in SOI and sSOI Triple-Gate MOSFETs 297  
*K. Na, S. Cristoloveanu, Y. Bae, W. Xiong, C. Cleavelin, P. Patruno and J. Lee*

## **Chapter 14 Poster Session**

Thermal Resistance Model for Multi-finger Trench-Isolated Bipolar Transistors on SOI Substrate 305  
*R. Rashmi, A. Kranti, G. Armstrong and S. Nirgin*

Fabrication of Thick-film Silicon-on-Insulator by Separation by Implanted Oxygen Layer Transfer <i>X. Wei, A. Wu, B. Zhang, M. Zhang, X. Wang and C. Lin</i>	311
The "U" Shape Behavior of GIFBE in Function of Back Gate Bias in FinFETs <i>P. G. Agopian, J. A. Martino, E. Simoen and C. Claeys</i>	317
Quantization Effect in Capacitance Behavior of Nanoscale Silicon Multigate Mosfets <i>A. Afzalian, C. Lee, R. Yan, N. Dehdashti Akhavan, C. Colinge and J. Colinge</i>	321
Pseudo-Mosfet Analysis of Proton Irradiated and Annealed SOI Wafer <i>S. Jung, J. Kim, L. Jung, Y. Lee, S. Cristoloveanu and Y. Bae</i>	329
High-K Ta2O5 Polyoxide Deposited on Polycrystalline with NH3 Plasma Treatment <i>C. H. Kao, K. S. Chen, J. S. Chiu, C. S. Chen, T. C. Chen, W. S. Luo and Y. T. Chung</i>	335
Author Index	341

*\* invited paper*