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### Session A1L-A: Communication Circuits and Systems

**Chair:** Mohammad Haider, *University of Alabama at Birmingham*
**Co-Chair:** Mitra Mirhasani, *University of Windsor*
**Time:** Monday, August 6, 2018, 8:30 - 10:00
**Location:** Mercuri

A low power CMOS voltage mode line driver for Fast Ethernet has been designed in a 180nm low cost technology from GlobalFoundries. Very low power consumption is achieved by using a voltage mode approach with a low power rail-to-rail operational amplifier (opamp). Using a Class-AB output stage further reduces the power consumption. While transmitting pseudo random data the power consumption is measured to be only 24mW which is to the best of the authors knowledge the lowest power consumption reported to date for such a line driver.

## Session A1L-B: VLSI Low Power Digital Circuits

**Chair:** Arezoo Emadi, *University of Windsor*
**Time:** Monday, August 6, 2018, 8:30 - 10:00
**Location:** Martis



Robust GNRFET/MOSFET Conjunction is employed to build various power gating structures using 16nm technology. The evolved Power Gating (PG) structure is composed of GNRFET as a footer sleep transistor and Silicon CMOS logic power gated module. The proposed structure resolves the main drawbacks of the traditional PG design from the point of view increasing the propagation delay and wake-up time in low–voltage regions. Leakage power, rush current, wake-up time and power delay product are used as the performance circuit parameters for the evaluation. The performance results of the proposed power gating structure with single footer reveals a reduction in leakage power, delay time, and wake-up time, on average up to 88%, 44%, and 24%, respectively, for different logic circuit modules compared to the MOSPG structure.



This paper compares designs of an asynchronous dual-rail domino logic (DRDL) and the conventional CMOS logic under near-threshold operation. The delay time and energy consumption of an 8-bit full adder are simulated by HSPICE with a 180nm CMOS technology. The results show, considering the process variations, DRDL is faster than CMOS below 1.1V. The delay performance of DRDL at 0.25V is equivalent to that of CMOS at 0.4V, when the energy-delay product of DRDL is 40% smaller than that of CMOS.



Sensing temperature for localizing hot spots provides additional observability in modern integrated circuits. A digital temperature sensor with modified inverter interlaced cascaded delay cells (IICDCs) is presented in this paper. Temperature is sensed using a temperature-to-pulse generator that produces pulse with an XOR gate and a temperature dependent delay line with the modified IICDCs. A D flip-flop based T flip-flop is used to produce a pulse used as the input signal of the delay line, and the inverted input signal is used to reduce the offset of temperature sensor. The output of the temperature-to-pulse generator is applied to a time-to-digital converter (TDC) to achieve digital codes of the sensed temperature. By using the modified IICDCs, it is possible to consume lower power than the conventional approach using the inverter-based delay lines. The temperature sensor is designed with 180 nm CMOS technology and 1.8 V supply voltage. This temperature sensor circuit consumes 324 μW and monitors -20 ℃ to 110 ℃ with a good linearity.



The globalization of the integrated circuit (IC) design flow has led to increased security vulnerabilities. Modern IC supply chain consists of multiple untrusted entities which makes it vulnerable to potential compromise by attackers, who can insert counterfeit ICs at any stage in the supply chain. The deployment of counterfeit ICs threatens the security and reliability of electronic components and systems. For this reason, it is imperative to mitigate these risks by developing robust counterfeit IC detection techniques. In this paper, we investigated the viability of a completely digital design technique for identifying counterfeit ICs by exploiting changes in the threshold voltage. We introduce a solution that is based on the premise that a recycled/remarked or reused IC exhibits a degraded threshold voltage (Vt) that leads to changes in the timing characteristics of CMOS designs. In contrast to currently available counterfeit IC detection techniques, the proposed method measures IC degradation after it has been used and does not require a reference IC to provide a baseline signature. We propose a robust aging sensor for detecting changes in Vt with a sensitivity of about 5%.

Pseudo-transient analysis (PTA) method has been researched for many years from the practical viewpoint since it is considered as the most promising method to find DC operating point for transistor-level circuits, which is the most fundamental and difficult task in circuit simulation. However, in many cases, especially for some large-scale circuits or combination circuits which contain different kinds of sub-circuits, different nodes may require different pseudo-capacitor values to converge. Same-rate of step size and capacitor values for all nodes may lead to nonconvergence. In this research, an adaptive dynamic-element algorithm is proposed for PTA method, which inserts dynamic pseudo-element to each transistor respectively, and the values vary according to the simulation states independently and automatically. Numerical examples are shown to illustrate the effectiveness and efficiency of proposed algorithm.

## Session A1L-C: Bioengineering Systems and Biochip

**Chair:** Mohamad Sawan, *Polytechnic Montreal*
**Co-Chair:** Ming-Dou Ker, *National Chiao Tung University, Taiwan*
**Time:** Monday, August 6, 2018, 8:30 - 10:00
**Location:** Luna



This paper presents the design of a MEMS based Outer Hair Cell (OHC) for use as a prosthetic implant on the top of the basilar membrane in the Cochlea to improve the hearing conditions for persons with damaged OHC. The MEMS hair cell (OHC) is designed to have a set of 6 variable length microfabricated cantilever beams that can be excited to deform like normal healthy OHC using electrostatic actuation. A 3D Finite Element Analysis (FEA) of the developed OHC has been carried out using IntelliSuite. The FEA results are in 17% agreement with an analytical model published elsewhere. The design eliminates the use of electrode as used in conventional cochlear implants (CIs) and has the potential to improve the hearing condition for patients suffering from sensory neural hearing loss due to cochlear outer hair cell damage.



This work presents the design and construction of a H-field probe with active balun for MRI (magnetic resonance imaging) conditional testing of medical devices. The H-field probe was designed using a small loop antenna with 2 mm radius to have high spatial resolution and sensitivity. It was tuned and matched at a center frequency of 128 MHz, which corresponds to 3 T MRI systems or equivalent RF exposure systems. An active balun with a gain 18.28 dB and noise figure of 0.5 dB was employed to boost the detected H-field signal level. The designed Hfield probe and active balun have been fabricated on a double sided printed circuit board (PCB), FR4 thickness of 1.57 mm and a copper thickness of 35 μm, with overall footprint of 22 mm × 11 mm.



Neuro-stimulators have been widely used in neural disorder control. This work presents a four-channel stimulator with adjustable positive and negative stimulus voltage from +/- 0.5V to +/- 8V. In the proposed stimulator, circuit operation with negative voltage has been successfully realized in a 0.25-μm 2.5V/5V/12V CMOS process with the grounded p-type substrate, and without suffering the p-n junction breakdown or electrical overstress issues. The proposed stimulator has been also practically verified with in-vivo animal test. By integrating the stimulator circuit with other circuit blocks together, the close-loop neuromodulation treatment can be implemented by an implantable system-on-chip (SoC) with low-power consumption.



In this work, we explore the fractional viscoelastic properties of the arterial blood vessel, and present a fractional-order lumped parameter model. We refer to this model as arterial fractional order visco-elastic (AFV) model. A novel feature of this characterization is that the ideal analog parameter displaying the arterial compliance in the well known windkessel model, has been replaced by a fractional order element (Fractional Capacitor). It displays the complex and frequency dependent total arterial compliance by combining both resistive and capacitive properties that exhibit the fractional viscoelastic behavior of the vessel wall. The contribution of both characteristics is controlled by a fractional differentiation order parameter (\alpha) enabling an accurate and real physiological description. The proposed model offers a pioneer way for the better interpretation of the viscoelastic effect on the arterial hemodynamic. In addition, it can be investigated as a reliable computer-based simulation platform for cardiac pathophysiology diagnosis and treatment.

## Session A1L-D: Hardware Implementation of Neural Network and Neuromorhic Computing

**Chair:** Vishal Saxena, *University of Idaho*
**Co-Chair:** Ayman Fayed, *The Ohio State University*
**Time:** Monday, August 6, 2018, 8:30 - 10:00
**Location:** Saturni

An important question when replicating biologically inspired networks is to model the synaptic interconnections between neurons. Biological representations often use unidirectional couplings between neurons. This waives problems on electrical models since electrical circuits are in general not free from feedback. We propose a solution based on a four-port circulator to overcome this issue. The method involves attaching appropriate resistances to this circulator, depending on the desired coupling. The wave digital representation of this approach reveals that our modeling enables true unidirectional interconnections between neurons. We use this method to investigate multiple gait pattern generators of a four-legged animal.

## Session A2P-E: Analog Design Applications

**Chair:** Mitra Mirhasani, *University of Windsor*
**Co-Chair:** Igor Filanovsky, *University of Alberta*
**Time:** Monday, August 6, 2018, 8:30 - 10:00
**Location:** Poster Area



This paper presents a 77 GHz CMOS Monotonically Linear Digitally Controlled Oscillator (ML-DCO) that is derived from a Colpitts topology. A new tuning mechanism is developed that alleviates the need for an ideal switch and assures linearity. Large nonlinear varactors are avoided, and the ML-DCO achieves 5 GHz linear tuning range that fulfills the requirements for short range and long range automotive radar sensors. The ML-DCO consumes a maximum of 9:12 mW and achieves a phase-noise of -98.53 dBc/Hz at a 1MHz offset frequency. The ML-DCO demonstrates



The paper considers a new method of modifying the transfer function denominator polynomial of a wideband amplifier to obtain a desirable overshoot. The method assumes that this initial polynomial is stable, and, using even and odd parts of this polynomial, one finds the ladder impedance or admittance which is called "phantom immittance". The modification of this immittance by introducing the resistances in series with the coils or in parallel with the capacitors changes the oscillating properties (damping and transient duration) of the immittance. The modified immitance numerator may be used as the transfer function denominator of the modified amplifier. The examples which illustrate the approach are taken from adapting for amplifier design the Butterworth or Bessel polynomials. In addition, a new property of immittance two-ports involving the Bessel polynomials is formulated.



This paper deals with linear time-invariant (LTI) systems and examines the link between the 3dB cutoff and time-constants. It shows that the cutoff frequency of a low-pass damped network can be estimated from the reciprocal of a p-norm calculated from the system's time-constants. Furthermore, to achieve good accuracy the p factor must have a fractional value, for example, p = 1.7. Two formulas are derived, and their performance evaluated using Monte Carlo simulations which reveal a sub-3% error for most cases.



In this paper we examine the influence of CMOS CCII non-idealities in an IC realization of a two-integrator Biquad. We compare two CMOS-CCII realizations of the Biquad; the same basic topology of the translinear CCIIs, but the W/L ratios of their transistors are optimized differently. One CCII possesses fewer non-idealities, while the other operates at higher frequencies. It is shown how the CCII nonidealities, causing lossy integrators, are applied in the Biquad design. Realizability constraints are given. With the example of a fourth-order 1MHz/100kHz BP filter, post-layout simulations with AMS 0.35-micron technology using Cadence, show close agreement with our analysis.

## Session A3L-A: Special Session on Computer Arithmetic in Honor of Drs. Graham Jullien and William Miller – Part I

**Chair:** Kenneth Jenkins, *Pennsylvania State University*
**Time:** Monday, August 6, 2018, 13:30 - 15:00
**Location:** Mercuri

## Session A3L-B: CMOS Implementation of Analog Circuits

**Chair:** Vishal Saxena, *University of Idaho*
**Co-Chair:** Rashmi Jha, *University of Cincinnati*
**Time:** Monday, August 6, 2018, 13:30 - 15:00
**Location:** Martis

## Session A3L-C: Wireless Communications

**Chair:** Hassan Mostafa, *Cairo University*
**Co-Chair:** Ibrahim M. Elfadel, *Khalifa University, Abu Dhabi*
**Time:** Monday, August 6, 2018, 13:30 - 15:00
**Location:** Luna



Optimization of the LTE network is crucial to obtain the best performance. The handover margin (HOM) and time to trigger (TTT) should be chosen so that the system will have minimum number of handovers per user per second, minimum system delay, and maximum throughput. In this paper a new handover optimization algorithm for long term evolution (LTE) network based on Q-learning optimization is presented. The proposed algorithm operates by testing different values of HOM and TTT then observes the output performance corresponding to the values of these parameters, and it eventually selects the values that produce the best performance. The proposed handover optimization technique is evaluated and compared to previous work. Q-learning achieves minimum average number of handover per user and also has maximum throughput than the fuzzy logic optimization technique.



We propose a multiplatform spectrum sensing prototype, which is capable to sense the UHF TV frequency bands from 500 MHz to 698 MHz (Channels 19 to 51) and identify the characteristic features of the primary users. Combining a high accurate spectrum sensing device, an open source RF Explorer and an RTL SDR receptor we collected critical information of the TV spectrum and know its usability. Results obtained shows the availability of white and gray spaces in the Centre for Engineering Innovation of the University of Windsor.



Ultrawide band (UWB) signals are extremely power limited due to the severe power spectral density (PSD) constraints obligated by the Federal Communications Committee (FCC). Therefore, the design of radiation efficient antennas for UWB signalling is a challenging step in the design and development of UWB communication systems, especially when these signals co-exist with previously standardized narrowband (NB) wireless services. This work presents a compact microstrip-based UWB antenna design that is capable of suppressing narrowband interference (NBI) signals. The immunity of the proposed design to NBI is tested both experimentally and through simulations. Moreover, the experimentally measured spectral characteristics are employed in simulating the impact of the proposed UWB antenna on a typical UWB signalling waveform. Both experimental and simulation results confirm the capability of the proposed design to suppress NBI signals at six different frequencies, corresponding to the most frequently used wireless services at these frequencies, while introducing an almost negligible distortion to the UWB signalling waveforms.



The paper presents area efficient 4Gbps clock and data recovery (CDR) by using improved phase interpolator (PI) with error monitor. The proposed CDR architecture has only two sets of phase interpolator while the conventional CDR has eight sets of phase interpolators. Each set of the PI is comprised of eight inverters to get 11.25˚ phase interpolation from 0˚ to 348.75˚ by using the proposed phase error monitor. The outputs of the phase error monitor are composed of 9 bits sampled from early pulse. The monitor chooses four clock phases among 0˚, 45˚, 90˚, 135˚, 180˚, 225˚, 270˚, and 315˚ from an analog voltage controlled oscillator (VCO) by sending 3 bits to the mutiplexer. Then, the other 6 bits determine the interpolation phase of each block by using the inverter switches. Vcont (Charge Pump Output Voltage) is pre-charged to 345mV for fast locking time. The time for frequency locking and phase selection are 23.35ns with pre-charge time (1.1ns). The design is simulated with a 180nm CMOS technology node at 1.8V power supply. The total power consumption of the proposed CDR is 4.35mW.

## Session A3L-D: Image Processing I

**Chair:** Wasfy Mikhael, *University of Central Florida*
**Co-Chair:** Vasily Moshnyaga, *Fukuoka University, Japan*
**Time:** Monday, August 6, 2018, 13:30 - 15:00
**Location:** Saturni

## Session A4P-E: Analog Circuit Designs

**Chair:** Yehia Massoud, *Stevens Institute of Technology*
**Co-Chair:** Mona Zaghloul, *National Science Foundation*
**Time:** Monday, August 6, 2018, 13:30 - 15:00
**Location:** Poster Area

## Session A5L-A: Special Session on Computer Arithmetic in Honor of Drs. Graham Jullien and William Miller – Part II

**Chair:** Earl Swartzlander, *University of Texas at Austin*
**Time:** Monday, August 6, 2018, 15:30 - 17:00
**Location:** Mercuri

## Session A5L-B: Oscillators and Modulators

**Chair:** Igor Filanovsky, *University of Alberta*
**Co-Chair:** Ebrahim Ghafar-Zadeh, *York University*
**Time:** Monday, August 6, 2018, 15:30 - 17:00
**Location:** Martis

This paper presents a technique to reduce the required number of cycles to reach a given quantization resolution of conversion performed by incremental Delta Sigma ADCs. Thanks to a specifically designed dynamic weighting of the modulator's coefficients combined with a dedicated digital filter, the OverSampling Ratio (i.e. OSR) can be reduced compared to conventional structures thanks to a more efficient quantization noise shaping. This dynamic weighted integration (DWI) technique is first motivated in the context of a first order modulator supported with a mathematical proof. In the second part, the proposed technique is extended to the specific case of a complex fourth order modulator with four different examples of topology regarding the position of the dynamic weighting.



In this article, a Ring-Assisted-Mach-Zehnder Interferometer (RAMZI) based RF-to-Optical Modulator with excellent spurious-free-dynamic- range (SFDR) performance has been presented. The performance of this silicon-based RAMZI device has been analyzed and verified with a commercial Photonic Circuit simulation tool. A compact Verilog-A model of RAMZI is also developed for hybrid CMOS circuit in Cadence environment. An SFDR of 129.97 dB/Hz^(2/3) has been obtained for this type of modulator.

## Session A5L-C: Image Processing II

**Chair:** M. Omair Ahmad, *Concordia University, Montreal, Canada*
**Time:** Monday, August 6, 2018, 15:30 - 17:00
**Location:** Luna



Unlike the regular cryptographic usage, hashing methods can be used to extract signatures in relation to the similar images detection. However, finding a hashing function for detecting image similarity seems to be a challenging task, as the hash code needs to represent the content rather than encrypt it. In this paper, a novel content-based image retrieval method using image hashing is proposed that generated a signature per image based on image rotation and DCT. The acquired hash code is used to train a memory model to find similar images. We evaluate our method by comparing it with some state-of-the-art methods.



This paper provides a computer vision based technique for automatically detecting and classifying fire by processing the video data generated by an ordinary camera. While there are a copious amount of publications in fire detection with images, distinguishing hazardous fire from non-hazardous is a problem that is still unsolved. The proposed technique uses the color and fluctuation characteristics of fire to detect it. Initially, the algorithm locates regions of the video where there is motion; from these regions fire colored pixels are extracted and then wavelet transform is applied to confirm that the moving object is fire. The proposed technique tracks the rate of increment of fire region to distinguish between hazardous and controlled fire. Experimental results demonstrate that the proposed technique is effective in detecting the fire and classifying it as hazardous or controlled flame. The performance of the technique was observed in terms of true positive rate which was observed to be 85.57% while the average delay in detection of hazardous fire was 66.2 frames at a frame rate of 10 frames per second or 6.62 seconds.



Curb detection is an important research topic in environment perception, which is an essential part of Autonomous Land Vehicles (ALV) and Unmanned Ground Vehicle (UGV) operations. Also, curb detection is specifically a component in Advanced Driver Assistance Systems (ADAS) that are assisting drivers in parking their cars without hitting the concrete curbs/parking blocks. In this paper, a novel curb detection algorithm is developed by using Canny edge detection along with Hough transform.

## Session A5L-D: Control I

**Chair:** Roozbeh Razavi-Far, *University of Windsor*
**Co-Chair:** Maher Azzouz Abdekkhalek, *University of Windsor*
**Time:** Monday, August 6, 2018, 15:30 - 17:00
**Location:** Saturni

# Tuesday, August 7, 2018

## Session B1L-A: Analog to Digital Converters

**Chair:** Igor Filanovsky, *University of Alberta*
**Co-Chair:** Mitra Mirhasani, *University of Windsor*
**Time:** Tuesday, August 7, 2018, 8:30 - 10:00
**Location:** Mercuri

This work describes an area efficient time-mode SAR ADC with capacitor flipping bit-cycling operation. The proposed SAR ADC can be realized with a single-capacitor and a single- current source where the capacitor flipping scheme eliminates multiple current sources used for the capacitor charging and discharging operation. Furthermore, the charge sharing error caused by parasitic capacitance is reduced by pre-charging the parasitic capacitor before the capacitor flipping operation. As a result, the SAR ADC can be implemented with extremely small area and low power consumption due to the reduced number of circuit components. An 8-bit 364.9kS/s time-mode SAR ADC is designed with CMOS 0.18um technology where the ADC operation and performance are verified through circuit level simulations.



A stochastic ADC is naturally a non-uniform nonlinear quantizer, in which post-correction is typically needed. In addition, even though it can achieve high precision, the range of a stochastic ADC is limited. Therefore, it is beneficial to use the stochastic array as a fine-stage in a sub-ranging architecture. In this work, look-up-table linearization with full mapping and sigma-based mapping for a stochastic ADC and sub-ranging stochastic ADC are examined and compared experimentally by Monte Carlo simulation and measurement. A test chip is fabricated for 4-bit coarse flash stage and 127 comparator arrays on 0.18μm CMOS. Measurements confirmed simulation results, and it is shown that full mapping can improve equivalent number of bit by 2 bits compared to sigma-based mapping. Furthermore, the results suggest that the coarse stage comparator with 5 times better input offset variation than fine stage comparator is suitable for sub-ranging implementation.

## Session B1L-B: VLSI Digital Integrated Circuits I

**Chair:** Masud Chowdhury, *University of Missouri at Kansas City*
**Co-Chair:** Hassan Mostafa, *Cairo University*
**Time:** Tuesday, August 7, 2018, 8:30 - 10:00
**Location:** Martis



This paper presents new 8T SRAM design that avoids the stability and reliability issues of the conventional 6T and other existing SRAM cells. The proposed 8T SRAM is as good as the 10T design without the overheads of the 10T cell. In the proposed design, virtual ground technique weakens the positive feedback and improves the write ability of the cell. Precharging circuit is not required for read operation, which reduce the area overheads of the SRAM memory system. The design isolates the storage node from the read path, which improves the read stability. For reliability study, we have investigated the static noise margin (SNM) of the proposed 8T SRAM and compared with the conventional designs at different process corners. The delay of the proposed bitcell is reduced to 69.67% during write and 52.87% during read compared to conventional 6T bitcell. In addition to this, leakage currents of the proposed 8T bitcell reduced to 4.24%, 9.5% and 18.65% in hold, read and write operations in contrast to conventional 6T bitcell. We have also analyzed the impact of the process and parametric variations in the proposed 8T SRAM using Monte Carlo simulations.



In this paper, two reverse converters for the four- moduli set {2^n,(2^n)-1,(2^n)+1,(2^(n-1))-1} are described. One of these is based on Mixed Radix Conversion (MRC). Another converter is based on two-stage MRC in which two pairs of moduli are considered and intermediate results are obtained using MRC. A second stage uses MRC to obtain the final decoded number from these intermediate results. Both the converters are compared with previously reported converter for this moduli set regarding hardware resources and conversion time. Synthesis results on FPGA and ASIC are also presented.



The Gate-All-Around (GAA) FET device structure is expected to become the next widely used evolution of FET architecture in the near future. In this paper, full-adder datapath circuits using Lateral GAA FETs (LGAA FETs) based on BSIMCMG model are analyzed. Full adder designs include minimum count (10 transistor) adders such as 13A adder, the SERF adder, the CLRCL adder as well as the standard mirror adder and Ultra-Low-Power Full Adder (ULPFA). To better characterize the operation of LGAA FETs, their performance is compared against multi-gate FinFETs, such as double-gate FinFETs, triplegate FinFETs and quadruple-gate FinFETs.

As Chip Multiprocessors (CMPs) scale to tens or hundreds of nodes, the interconnect becomes a significant factor in cost, energy consumption and performance. Energy efficiency of the underlying communication framework plays a major role in the performance of multi-core systems. Recent work proposes buffer-less deflection routing as a cost effective alternative. A modified version of CONfigurable NETwork Creation Tool (CONNECT) is proposed as a buffer-less router to be lightweight and efficient. Modified CONNECT is based on parallel port allocation mechanism within the routers, that allows maximum number of flits to be deflected in a productive direction. Modified CONNECT is evaluated using uniform, transpose and inverse traffic workloads against CONNECT, BLESS and CheapInterconnect Partially Permuting Router (CHIPPER) on a 4x4 mesh network. Modified CONNECT saves 30% area compared to CONNECT while employing lower performance. Modified CONNECT also saves 24% in area against BLESS keeping the same performance.



We present a flexible, low-complexity additive white Gaussian noise (AWGN) channel emulator. The proposed generator employs multiple improved Tausworthe generators to generate uniform random numbers, which are then summed up and manipulated based on the central limit theorem to generate Gaussian random numbers. We simulated the hardware design with 12 and 48 Tausworthe random number generators (RNGs) with different seed sets. The proposed design provides one sample per clock useful towards high speed channel emulation.

## Session B1L-C: Energy Harvesting

**Chair:** Mohamad Sawan, *Polytechnic Montreal*
**Co-Chair:** Po-Hung Chen, *National Chiao Tung University, Taiwan*
**Time:** Tuesday, August 7, 2018, 8:30 - 10:00
**Location:** Luna



This paper presents an automatic-frequency-tuning RF energy harvester. The proposed self-startup system tracks the frequency of maximum input power automatically within its wide frequency range of operation from 1.65 GHz to 2.5 GHz. The system is mainly composed of two rectifying paths and a frequency tuning control loop. Implemented in a 130-nm CMOS technology, simulation results show power conversion efficiency (PCE) of the main path rectifier of 62% at 10-kΩ load resistance. The input power sensitivity of the main path is -18 dBm for output voltage of 0.5 V and a load resistance of 100 kΩ.



This paper presents a 5.2 GHz band, 67 % efficiency at the input power of +20 dBm RF Energy Harvester (EH) for IoT/wearable devices. In order to keep the high efficiency over the wide RF input range, the reconfigurable 6-parallel rectenna is proposed. The configuration of rectenna is automatically changed depending on the RF input power level. Also, adaptive matching is proposed to adjust the matching network automatically depending on the number of stages of rectenna, RF input frequency, and load current. Each RF-DC converter in rectenna is implemented by two Schottky diodes in a package and with a harmonic control scheme to produce a reasonable output DC voltage. Buck-boost converter is integrated to provide a constant voltage to the IoT/wearable devices. By using reconfigurable structure, different values of efficiency and the output DC voltage can be achieved. The measured efficiency of RF EH is 67 % with an output DC voltage of 6.1 V when the RF input power level is +20 dBm at the frequency of 5.2 GHz single-tone signal. It can charge the wearable devices such as G Watch, Mi band, and SmartThinQ.

## Session B1L-D: Control II

**Chair:** Maher Azzouz Abdekkhalek, *University of Windsor*
**Co-Chair:** Mohan Krishnan, *The University of Detroit Mercy*
**Time:** Tuesday, August 7, 2018, 8:30 - 10:00
**Location:** Saturni

In this paper, we show that multiple, maliciously controlled vehicles can destabilize a vehicular platoon, to catastrophic effect, through local modifications to the longitudinal control law. We propose a systematic method that illustrates how multiple attackers can change their control configuration in tandem with each other in order to create a successful attack. We determine the range of gains based on the changes the other attacker initiated that allow an attacker to violate the stability criteria at different positions in the platoon. Finally, we demonstrate the impact of the designed collaborative attack on the vehicular platoon through an example.

## Session B2P-E: Circuits and Systems I

**Chair:** Hassan Mostafa, *Cairo University*
**Co-Chair:** Sherif Michael, *Naval Postgraduate School*
**Time:** Tuesday, August 7, 2018, 8:30 - 10:00
**Location:** Poster Area



Fruit quality control is receiving increasing attention as an important application of bio-impedance measurements, which is a non-invasive technique. However, to effectively monitor fruit samples in the market, cheap and portable bio-impedance analyzers are needed while maintaining the accuracy of measurements over a wide frequency range. In this work, we report on the results obtained from a portable bio-impedance measuring device that relies on a modified Kramers-Kronig transform for calculating the phase from the measured impedance magnitude. This means that no actual hardware phase measurement takes place. The aging effect of strawberries is shown to be detected clearly via the change in impedance.



Due to the complexity of stochastic random errors of inertial measurements units (IMU) and Global Navigation Satellite Systems (GNSS), the design of IMU/GNSS fusion filters is challenging. Conventional approaches collect IMU/GNSS data and tune filter parameters against a ground-truth trajectory. However, this process does not verify the ability of the integration filter to correctly estimate hidden errors of sensors. Another challenge is the design of different dynamic models and error models for different moving platforms. To test a dynamic model, linearization and approximation of the dynamic model are commonly performed manually. This conventional design method is not flexible and prone to errors. To address these design challenges, this paper introduces a flexible simulation and design environment for IMU/GNSS integration. A MATLAB implementation of the environment is given. While the current implementation of the environment is handling IMU/GNSS integration for vehicular dynamic models, other dynamic models and additional sensors can be easily integrated in the environment.



Implementation of a Pressure Ulcer Prevention System would prevent pressure ulcers, ease workload on caregivers, enabling patient treatment and monitoring outside a hospital setting, and reduce health care costs. Accurate measurement of pressure is an important criteria in order to achieve the above said goals. A challenge associated with using Force-Sensing Resistors (FSRs) as a pressure sensor is the part-to-part variability of up to +/-25%. This paper presents a novel modeling technique for correcting force sensor nonidealities, without requirement of prior knowledge of material parameters, and enabling measurement accuracies of +/-2% over a pressure range of 1N to 5N.

**Automatic Crop Furrow Detection for Precision Agriculture** .....
*Manpreet Kaur (University of St. Thomas), Cheol-Hong Min (University of St. Thomas)*

The development in the robotics equipped with machine vision sensors applied to Precision agriculture is a demanding solution for various applications in the agriculture. This paper proposes an automatic furrow detection system based on identifying crop furrows from different growth stages of maize plants in the presence of weeds. The proposed image processing method consists of four different processes. First, image segmentation based on HSV (Hue, Saturation, Value) decision tree which discriminate crops, weeds, sky, and soil. Then, the noises in the images are eliminated by selecting pixel values. Further, mathematical morphological processes, that is, erosion to remove smaller objects followed by dilation to enlarge the boundaries of regions of foreground pixels are applied. To detect the position of furrows, ROI was defined by creating a binary mask. The Hough Transform and blob analysis were applied to detect crop furrows. The experimental results show that the method is effective.

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*Alex Roman (Case Western Reserve University), Parisa Dehghanzadeh (Case Western Reserve University), Vida Pashaei (Case Western Reserve University), Abhishek Basak (Case Western Reserve University), Swarup Bhunia (Case Western Reserve University), Soumyajit Mandal (Case Western Reserve University)*

Due to the need for development of customized transmission, reception, and processing algorithms, low-cost programmable ultrasound imaging devices are desirable for a variety of research applications. This paper describes a programmable 64-channel system-on-chip (SoC)-based test bench for research on autonomous wearable and implantable medical ultrasound imaging. The setup consists of a custom transmitter, a custom high-voltage (HV) multiplexer, an off-the-shelf receiver, and embedded software on the SoC. This results in a modular design that can be easily updated with improved hardware and software for different applications. This paper describes the system design and initial imaging results on tissue phantoms.

**Utilizing Inherent Randomness in Stochastic Computing** ..... 528
*Xiaojia Wang (Clemson University), Yingjie Lao (Clemson University)*

Nowadays, low-cost and efficient integrated circuit (IC) design is of great interest due to the proliferation of computing devices, the resource-constrained nature of these systems, the desire to improve computing capability, and the need to reduce the cost. Stochastic computing has emerged as a promising alternative computing paradigm to binary deterministic computing, which enables very low-cost implementations of arithmetic operations using standard logic elements while achieving a higher degree of fault-resistance. However, it exhibits inherent randomness owing to its stochastic representation of data, which degrades the accuracy of the computation. Instead of trying to eliminate the inherent randomness to improve accuracy, this paper introduces the idea of utilizing the inherent randomness to enhance the performance of stochastic computing applications. We show that the inherent noise in stochastic computing can be utilized to perturb neural networks to escape local optima or saddle points, reduce over-fitting, and augment data. For example, the proposed methodology could improve the test accuracy of a multi-layer convolutional neural network on the CIFAR-10 dataset by 5%.

**An Error Analysis Model for Floating-Point DFT Algorithms** ..... 532
*Violeta Reyes-Rodríguez (University of Puerto Rico at Mayagüez), Manuel Jiménez (University of Puerto Rico at Mayagüez), Domingo Rodríguez (University of Puerto Rico at Mayagüez)*

This paper presents a study of accuracy and hardware performance of floating-point (FP) implementations of the Discrete Fourier transform (DFT) and its fast algorithms. The studied formulations include Cooley-Tukey's and Pease's. Approximation and statistical methods were used to assess the accuracy of the FP treatments, while quantifying their normwise relative error. A hardware performance analysis was carried via FPGA synthesis, allowing for quantifying resource consumption and latency of each treatment. The results of the study showed significant differences in accuracy in the different treatments and to interesting accuracy-space-speed tradeoffs when transform sizes were scaled.

## Session B2P-F: Live Demos and M.Sc./PhD Forum

**Time:** Tuesday, August 7, 2018, 8:30 - 10:00
**Location:** Poster Area

**Antenna Design for Magnetic Energy Transmission to Low Frequency RFID Tags in Small Aquaculture Tanks** ..... 536
*Judith Santana Abril (University of Las Palmas de Gran Canaria), Graciela Santana Sosa (University of Las Palmas de Gran Canaria), Juan A. Montiel-Nelson (University of Las Palmas de Gran Canaria)*

This work is focused in the antenna design of a RFID reader operating at low frequency. The RFID system is for transmitting magnetic energy between a tag located on a free-swimming fish in an aquaculture tank and a base station located outside the tank. It operates at the frequency of 134.2 kHz. In particular, the ad-hoc antenna design and the transmission stage of the proposed system is optimized for maximum distance and energy transmission efficiency.

## Session B3L-A: Low Power Design and Modelling

**Chair:** Mitra Mirhasani, *University of Windsor*
**Co-Chair:** Sebastian Magierowski, *York University*
**Time:** Tuesday, August 7, 2018, 13:30 - 15:00
**Location:** Mercuri



This paper introduces a review of Event-Driven Wake-Up Sensors interfaces and investigates Time-Domain Injection-Locked Oscillator design solutions to reduce power consumption. Threshold-based sensing, digital classifying and analog feature extraction method are presented. To overcome the power consumption limits provided by State of the Art threshold detection methods, a novel threshold detection method based on Injection-Locked-Oscillator time-domain comparator is proposed. The proposed comparator architecture consumes 790 pW for an input full scale signal of 320 mV with a frequency of 1 KHz.



A high-accuracy switched-capacitor (SC) capaci-tance-to-time (C/T) converter for differential capacitive sensors is presented. In the proposed circuit the propagation delays and the offset voltage of the comparator, the finite gain of the op-amp, and the channel charge injection and clock feedthrough due to analog switches have negligible effect on the accuracy of the circuit. Therefore, the design constraints of op-amp and comparator can be relaxed even for high conversion accuracy. Performances of the proposed circuit are simulated by HSPICE using 0.18 micrometers CMOS process parameters. Simulated results have demonstrated that the gain error is 0.0035 % and the maximum nonlinear error is about 0.015 % of the full scale and indicate that 0.1% resolution is achievable even when low-gain amplifier is used. The power consumption of the proposed circuits was 41.3 microwatts for ±0.9 V supply voltages.



Analyzing trace components in complex samples is important in many research fields. However, factors such as power consumption, input dynamic range, and non-portability limit the efficacy of the devices used for electrochemical analysis. This paper proposes an integrated low-power multi-modal wide-dynamic-range potentiostat to overcome these limitations. A continuous mode and a discontinuous mode are integrated in the circuit to increase its dynamic range. The operation mode and the programmable gain can also be set automatically by a microcontroller. The circuit is realized in the UMC 180 nm process and consumes 60 \muA from a 1.8 V supply with an active area of 350 \mum \times 150 \mum. Both simulations and experimental results prove the functionality of the proposed potentiostat.



Automatic analog integrated circuit design is still an open topic. Simulation-based optimization is accurate but relies on the efficacy of heuristics to find a solution. Equation-based optimization is faster but the accuracy depends on the set of equations. We propose an equation-based surrogate model that combines physics-based transistor model, curve fitting approximations for device parameters, and circuit analysis describing the metrics of the circuit to optimize. Two design examples are provided as proof of concept of the proposed optimization framework. The results prove this technique to be effective finding solutions for different processes technologies and flexible to the specifications.



This paper describes an experimental study and modeling of the current-transconductance dependence of the ALD1106 and ALD1107 arrays. The study tests the hypothesis that the I-gm dependence of these 7.8µm MOSFETs conforms to the Advanced Compact Model (ACM). Results from performed measurements, however, do not support this expectation. Despite the relatively large length, both ALD1106 and ALD1107 show sufficiently pronounced `short-channel' effects to render the ACM inadequate. As a byproduct of this effort, we confirmed the modified ACM equation. With an m factor of approximately 0.6, it captures the I-gm dependence quite well. The paper also introduces several formulas and procedures for I-gm model extraction and tuning. These are not specific to the ALD transistor family and can be applied to MOSFETs with different physical size and electrical performance.

## Session B3L-B: VLSI Digital Arithmetic Circuits

**Chair:** Arezoo Emadi, *University of Windsor*
**Time:** Tuesday, August 7, 2018, 13:30 - 15:00
**Location:** Martis

## Session B3L-C: Power Converters

**Chair:** Po-Hung Chen, *National Chiao Tung University, Taiwan*
**Co-Chair:** Ayman Fayed, *The Ohio State University*
**Time:** Tuesday, August 7, 2018, 13:30 - 15:00
**Location:** Luna

## Session B3L-D: Design, Modelling and Fabrication of Semiconductor Technologies

**Chair:** Vishal Saxena, *University of Idaho*
**Co-Chair:** Sudarshan Srinivasan, *North Dakota State University*
**Time:** Tuesday, August 7, 2018, 13:30 - 15:00
**Location:** Saturni

## Session B4P-E: Signal Processing Systems

**Chair:** Wasfy Mikhael, *University of Central Florida*
**Co-Chair:** Kenneth Jenkins, *Pennsylvania State University*
**Time:** Tuesday, August 7, 2018, 13:30 - 15:00
**Location:** Poster Area



This paper presents novel two-stage comb decimation filter for the multiple of three odd decimation factors. The novelty of this filter is the alias improvement in all folding bands at low cost. More specifically, like in comb-zero rotation method, the alias rejection improvement is obtained by placing additional zeros into comb folding bands. However, this is achieved by using simple multiplierless filters, placed in both stages of the comb structure. The second stage is decimated by three, while the first stage is decimated by one third of the overall decimation factor. The choice of multiplierless filters is discussed and the corresponding structures are presented. Finally, the comparisons with some methods, proposed in literature, are provided.



This paper presents method to reduce Mean Squared Error (MSE) produced by additive Gaussian noise and impulse noise, using Oversampled Filter Banks (OFB) and Low-Density Parity-Check (LDPC) coding. Two methods are used for the OFB design: Discrete Cosine Transform (DCT) modulation and the Discrete Fourier Transform (DFT) modulation. The same lowpass prototype Finite Impulse Response (FIR) filter is used in both approaches. The polyphase decomposition of the analysis and synthesis filters bank is performed to obtain more efficient structure. The input signal, in the transmitter, is splitted into subbands using the analysis filter bank and coded with LDPC coding.On the receiver side, the inverse process is performed. The proposed method is compared with the similar approaches from literature, using Matlab simulations.



Pulse compression is a powerful tool to estimate the impulse response of a system in noisy measurement environment conditions. A direct application of this technique, however, implies the introduction of side-lobes that come together with the desired response. A reduction of these side-lobes can be obtained through appropriate windowing techniques: one of these techniques, based on the Reactance Transformation, has recently been proposed by the authors and applied to the Nyquist's Raised Cosine Window. In this paper, the Reactance Transformation technique is applied to a number of windowing techniques, among the most frequently used in NDT. The experimental results show that, when applied to bandpass signals, it always has a positive effect in reducing the side-lobes closer to the main peak, and therefore in improving the range resolution of Pulse Compression-based systems.



The fractional spurs of All Digital Phase-lock Loops (ADPLL) is limited by the resolution and linearity of the time-to-digital converter (TDC). Although a high resolution narrow range TDC can be achieved in digital-to-time converters (DTC) assisted ADPLL, it actually shifts the nonlinearity issue to the DTC block, which may also bring unwanted spurs. In this paper a multi-phase detecting method is proposed for the cancellation of the spur caused by the nonlinearity both from DTC and TDC. The proposed multi-phase detecting architecture contains an inherent finite impulse response (FIR) filter to suppress the fractional spur. What's more, the FIR filter can adapt to the frequency variation of fractional spurs. The simulation results show that this method significantly eliminates fractional spur without adding other noise.

## Session B5P-E: System Architecture, Hardware, Software Co-Design

**Chair:** Sazzadur Chowdhury, *University of Windsor*
**Co-Chair:** Fathi Hassan Amsaad, *The University of Toledo*
**Time:** Tuesday, August 7, 2018, 15:30 - 17:00
**Location:** Poster Area

## Session B6L-A: Low Power and Low Density Communication Systems

**Chair:** Arjuna Madanyake, *University of Akron*
**Co-Chair:** Magdy Bayoumi, *University of Louisiana*
**Time:** Tuesday, August 7, 2018, 15:30 - 17:00
**Location:** Mercuri

## Session B6L-B: VLSI Digital Integrated Circuits II

**Chair:** Nader Rafla, *Boise State University*
**Co-Chair:** Sudarshan Srinivasan, *North Dakota State University*
**Time:** Tuesday, August 7, 2018, 15:30 - 17:00
**Location:** Martis



Pre-Charge Half Buffer (PCHB) is a Quasi-Delay Insensitive (QDI) asynchronous design paradigm that has found commercial applications in the semiconductor industry. PCHB circuits use dual-rail signals instead of Boolean logic and are unique in that PCHB gates incorporate both registration and a handshaking scheme for synchronization. We have developed a methodology for formal equivalence verification of combinational PCHB circuits against their corresponding Boolean specification circuits. The methodology transforms the PCHB circuit into a Boolean circuit, which can then be checked against a Boolean specification circuit using an existing combinational equivalence checker. The methodology also checks for liveness and handshaking correctness of the original PCHB circuit. The proposed methodology has been demonstrated using several multipliers and ISCAS circuit benchmarks.



Standard library cells (STD cells) being basic building blocks for ASIC/CPU design, play a key role in PPA enhancement and hence in design perfection. This paper presents first of its kind research to bridge the gap between conventional STD cell monotonic characterization and resulted STD cell liberty format file (.lib file) attributes usage with respect to ASIC tool cost function in an ASIC/CPU design and proposes a novel 3 dimensional (3D) monotonic characterization method for PPA boosting. An Algorithm for characterizing 3D monotonic cells is defined. About 10% to 60% of library cells are observed to be non-3D-monotonic in various libraries, architecture of libraries, and technology of libraries. Primetime results proving that selecting 3D-monotonic cells in an existing library using the algorithm give excellent PPA gain. By repairing non-3d-monotonic cells to cells fitting 3D-monotonic characterization, summary of post-route, post-extracted, primetime results from study of several projects showed further PPA improvement. PPA gain and advantages varies with ASIC flow settings, ASIC tool vendors, size of CPU, performance target, etc... with no disadvantages.



Network-on-Chip (NoC) has become a target to security attacks. By experiencing outsourcing design, NoC can be infected with a malicious Hardware Trojans (HTs) which potentially degrade the system performance or leave a backdoor for secret key leaking. In this paper, we propose a HT model that applies a denial of service attack by misrouting the packets, which causes deadlock and consequently degrading the NoC-based system. We provide a runtime HT detection and avoiding modules through a proposed secure routing algorithm. Results show that our proposed model has negligible overhead in area and power, 0.4% and 0.6%, respectively.



This paper proposes a digital design method enabling a constant path delay across temperature and process corners in 40nm CMOS. Thus, timing analysis and logic synthesis is simplified significantly. The temperature dependency is eliminated by operating at the zero temperature coefficient supply voltage. Additionally, process corner adaptive body biasing compensates process corner dependent path delays. Extensive transistor level simulations for various standard cells show constant path delays across temperature and 6 sigma process corners. All applied body bias voltages lie within the transistor reliability. This method enables rapid digital synthesis without time consuming process and temperature analyses and optimization.

## Session B6L-C: Digital Signal Processing for Medical Applications

**Chair:** M.N.S. Swamy, *Concordia University, Montreal, Canada*
**Co-Chair:** M. Omair Ahmad, *Concordia University, Montreal, Canada*
**Time:** Tuesday, August 7, 2018, 15:30 - 17:00
**Location:** Luna



In field of angular position sensing MR sensors play a dominant role, because of their high accuracy and robustness. However, upcoming vehicle concepts lead to increasing requirements, which cannot be fulfilled by available sensors. Thus, in this paper promising signal processing methods for MR sensor array are investigated. Three well known image processing methods are adapted to magnetic field sensors arrays for angular detection. The presented methods are compared and judged regarding their applicability.



This study develops a wearable medical system for real-time arrhythmia detection, which acquires electrocardiogram (ECG) data through a three-lead ECG sensor. It performs ECG signal processing and immediately alerts the patient's health care provider of an arrhythmia via wireless messaging. In particular, a common form of arrhythmia known as premature ventricular contractions (PVCs) are identified using the Pan-Tompkins and the wavelet-based template-matching algorithms. When three or more consecutive PVCs are detected, the device sends urgent report email to a patient's health care provider. In the experimental study, the design has been successfully validated using benchmark records from the MIT-BIH arrhythmia database. A low-cost Texas Instruments TMS320C5515 and Raspberry Pi 3 Model B are chosen to be the hardware platform. This study suggests a viable, low-complexity solution for real-time heart monitoring and arrhythmia detection.



In recent years, the accurate early diagnosis of Alzheimer's disease (AD) using different biomarkers through machine learning techniques has been the hottest research in preventing, treating, and slowing down the progression of the disease. However, a common bottleneck of the diagnostic performance is overfitting due to having lot of irrelevant features in the training data. In view of this fact, we propose a novel classification framework which uses unsupervised autoencoder to select the subset from given structural and clinical features followed by a supervised layer to automatically identify the patients having AD, mild cognitive impairment, and cognitively normal.



In this paper, both linear and nonlinear features have been reviewed with linear support vector machine (SVM) classifier for neural seizure detection. The work introduced in the paper includes performance measurement through different metrics: accuracy, sensitivity, and specificity of multiple linear and nonlinear features with linear support vector machine (SVM). A comparison is performed between the performance of different combinations between 11 linear features and 9 nonlinear features to conclude the best set of features. It is found that some features enhance the detection performance greatly. Using a combination of 3 features of them, a linear SVM classifier detects seizures with sensitivity of 96.78%, specificity of 97.9%, and accuracy of 97.9%.

## Session B6L-D: Diagnostics and Fault Tolerant Control System I

**Chair:** Roozbeh Razavi-Far, *University of Windsor*
**Time:** Tuesday, August 7, 2018, 15:30 - 17:00
**Location:** Saturni

# Wednesday, August 8, 2018

## Session C1L-A: Digital Signal Processing

**Chair:** Esam Abdel-Raheem, *University of Windsor*
**Time:** Wednesday, August 8, 2018, 8:30 - 10:00
**Location:** Mercuri



This paper proposes an efficient algorithm for impulsive active noise control (IANC) systems. The impulsive sources cannot be modeled by Gaussian distribution, and hence the standard adaptive algorithm based on second order statistics would give poor performance or even fail to converge. One solution is to derive adaptive algorithm by minimizing a fractional low order moment, resulting in the famous filtered-x least mean p-power (FxLMP) algorithm. The proposed algorithm discussed in this paper is based on a previously proposed generalized FxLMP algorithm. The key idea here is to introduce a variable step-size using a convex-combination approach. A large value is used at the start-up of IANC system to achieve a fast convergence speed. As the AINC system converges, the step-size automatically reduces to a small value to improve the steady-state noise reduction performance. Simulations demonstrate the effectiveness of the proposed algorithm.



One of the more severe attacks for self-recovery schemes is the discordant size content replacement attack. This attack substitutes a set of samples from an audio signal with another set of samples of different sizes. In this paper, a watermarking scheme for digital audio self-recovery that is robust to the discordant size content replacement attack is proposed. Our goal is to recover a tampered audio signal after such an attack. In particular, our scheme models the problem using source-channel coding. This method generates a watermarking where a lossy compressor is applied and the source coding output is protected with a channel coder. The coded data is then distributed into the original audio signal. In the recovery stage, a synchronization strategy is used to synchronize the watermark and this makes audio signal self-recovery possible. Our results shows that the propose scheme is robust to the discordant size content replacement attack for attacks of about 20% of the whole audio.



This research involves the development of an active muffler, an Electromechanical Active Helmholtz Resonator (EMAHR), that suppresses the fundamental frequency being exhausted through an engine's tailpipe. The EMAHR is a tracking side-branch resonator terminated with a composite piezoelectric transducer. The EMAHR creates a notch that can be moved between 200-1000 Hz which can be moved with an impedance consisting of negative capacitance, an inductance varying from positive to negative, and positive or negative resistance. Described in this paper is the required electrical load, and the development and selection of a digital filter that is implemented in an impedance generation circuit.



In this paper, we propose blind source separation (BSS) as pre-processing to unsupervised keyword spotting. We adopted our recently proposed keyword spotting and employed BSS framework to improve the detection rate in keyword spotting when speech signals are affected by mixing. BSS can improve the performance of keyword spotting, when intelligibility of speech signals is affected by mixing of noise or other speech signals. The TIMIT speech corpus is employed to examine the effectiveness and viability of proposed BSS framework as pre-processing to keyword spotting. It is observed that detection rate of keyword spotting framework is improved by applying BSS as pre-processing as compared to the framework without being pre-processed through BSS.



The filter tap-length is a significant structural parameter of adaptive filters that can influence both the complexity and steady-state performance characteristics of the filter. In direct form structure filtering, commonly known as a finite impulse response (FIR) adaptive filter, several schemes were used to estimate the optimum tap-length. Among existing algorithms, pseudo Fractional Tap-length (FT) algorithm is of particular interest because of its fast convergence rate and small steadystate error. Lattice structured adaptive filters, on the other hand, have attracted attention recently due to a number of desirable properties. In this paper a Fractional Order Lattice Predictor (FO-LP) algorithm is formulated using forward residual errors to update the lattice order at each iteration and hence obtain the structural optimum filter order adaptively.

## Session C1L-B: Hardware and Cyber Security I

**Chair:** Yingjie Lao, *Clemson University*
**Co-Chair:** Rashmi Jha, *University of Cincinnati*
**Time:** Wednesday, August 8, 2018, 8:30 - 10:00
**Location:** Martis



Arbiter PUF (APUF) is a popular style of physical unclonable function (PUF) that has been used in many security applications. The amount of process variation of an APUF is an important parameter strongly influencing its resolution. Although various attempts have been made to increase APUFs' random variation from the circuit design prospective, little work has been done to enhance manufacturing mismatch through transistor-level layout. In this work, we propose a novel layout strategy for enlarging inner-die delay variation of an APUF circuit in an area neutral manner. The mechanism separates a pair of racing delay units by an appropriate distance. Corresponding variation enhancement is quantified according to Pelgrom's mismatch model. Cadence Monte Carlo sampling shows the proposed scheme improves delay variation of 0.13 um technology 128-stage APUFs with minimum transistor size by as much as 8% without significantly affecting the inter-die hamming distance.



This paper proposes a novel architecture of a simple, low energy silicon physically unclonable function arrays based on large random variation of threshold voltage of MOSFET, operating in the subthreshold region. The proposed structure is a strong silicon PUF with 2^60 challenge response pairs consuming an energy of 0.48pJ/bit. The PUF simulations are carried out in 65nm CMOS technology. It is found to have inter-HD value of 0.4982 and intra-HD value of 0.0225. It is suitable for building secure IoT devices.



Reliability is an important performance metric of physical unclonable function (PUF) based authentication. This paper proposes a novel methodology that incorporates error rates into PUF response error correction to improve the overall performance. The proposed method first obtains the PUF circuit parameters by using machine learning techniques, which are then used to estimate the corresponding error rates. Then, we assign PUF response bits with different degrees of error-tolerance, according to their estimated error rates. Response weighting algorithm is proposed to determine the optimal weight assignment for each PUF response bit, which is formulated as an integer optimization problem. Experimental results show that the proposed response weighting algorithm can reduce not only the false negative from 20.6% to 8.3% under a noisy environment, but also the false positive rate by 58% for a PUF-based authentication with 127-bit response and 13-bit error correction.



Interest in hardware Trojan detection has grown tremendously over the last decade. Several methods for detecting hardware Trojan have been proposed. Due to enormity of possible Trojans, researchers believe that runtime detection is required as a last line of defense. However, to cater different types of hardware Trojans, several detection techniques should be concurrently applied. In this paper we propose a framework for optimizing runtime hardware Trojan detection monitors. We propose a formal verification approach to identify the vulnerable behavior of the hardware using the counterexamples generated by model checker. We devised a heuristic to understand the relationship between the counterexamples and required detection unit. To optimize the number of detection techniques, we leveraged Game Theoretic models to obtain a set of optimized design choices.



This paper describes the development of a model for the simulation of electrothermal coupling to detect malicious circuits with on-chip temperature sensors. The strategy is presented using the layout of a digital control logic block from an 8-bit conventional successive approximation register (SAR) analog-to-digital converter (ADC). A differential temperature sensor with a high sensitivity of 2.1V/degree Celsius was designed with 130nm CMOS technology. Joint simulation results of the circuit under test and temperature sensor indicate the potential for temperature-based hardware Trojan (HT) detection with on-chip resources.

## Session C1L-C: Power

**Chair:** Narayan Kar, *University of Windsor*
**Co-Chair:** Maher Azzouz Abdekkhalek, *University of Windsor*
**Time:** Wednesday, August 8, 2018, 8:30 - 10:00
**Location:** Luna



## Session C2P-E: Circuits and Systems II

**Chair:** Mohsin M. Jamali, *The University of Texas of the Permian Basin*
**Co-Chair:** Ahmed Abdelgawad, *Central Michigan University*
**Time:** Wednesday, August 8, 2018, 8:30 - 10:00
**Location:** Poster Area

The soft-decision Low-Density Parity-Check (LDPC) decoders have been applied in several storage systems thanks to their powerful error correction capability. However, these systems may suffer a long read latency since the softdecision decoders require an intensive computations as well as a long sensing time for the soft-information to decode. In this paper, we modify the recent-introduced Probabilistic Parallel Bit-Flipping (PPBF) LDPC decoder, to use on the storage systems in replacing the soft decision decoders, to improve the memory reading speed. The modified decoder is named Non-Syndrome Probabilistic Parallel Bit-Flipping (NS-PPBF). A special flipping mechanism is introduced such that the decoder can stop flipping without requiring the syndrome check results, which helps significantly improve the decoding frequency. We provide also the hardware architecture to implement NS-PPBF on the LDPC code used on the memory systems, which are usually very long block length with very high rate. The advantages of using PPBF decoder in terms of error correction and decoding throughput are confirmed by the simulating decoding performance and the hardware synthesis.

## Session C3L-A: Digital Filter Design

**Chair:** Hon Keung Kwan, *University of Windsor*
**Co-Chair:** Arash Ahmadi, *University of Windsor*
**Time:** Wednesday, August 8, 2018, 13:30 - 15:00
**Location:** Mercuri



In this paper, sparse FIR digital filter design using iterative multiobjective cuckoo search algorithm (MOCSA) is presented. The least-squares frequency response error and the l_1-norm of selected non-zero filter coefficients of a sparse digital filter are jointly minimized by iterative multiobjective cuckoo search algorithm until convergence. After convergence, a final round of single-objective cuckoo search is performed to minimize the least-square frequency response error of the sparse digital filter to arrive at an optimal solution. The sparse digital filter design results obtained by the iterative MOCSA compares favorably with the obtained results of another optimization method.



In this paper, sparse linear-phase FIR digital filters are designed using artificial bee colony (ABC) algorithm. Sparse digital filters can be used in applications where computational cost and complexities are of concern as zero-valued coefficients eliminate multiplications required for implementation. In this method, sparse digital filters are designed using minimax optimization by ABC algorithm and successive elimination. In contrast to methods which minimize insignificant coefficient values, this method eliminates insignificant coefficients by setting them to zero. The sparse linear-phase FIR filters designed using ABC algorithm are compared to the partial l1-norm optimization design, the minimum increase design, and the smallest coefficient design to illustrate the effectiveness of each design method.



In this paper, we propose a method for designing a low-delay low-pass/band-pass maximally flat integer-order differentiators in passband based on flatness characteristics and in stopband based on equiripple characteristics. The proposed function consists of two functions. One of functions has low-delay and flat characteristics in the passband. The other gives the whole function equiripple characteristics in the stopband. The low-delay low-pass/band-pass integer-order differentiators designed by the proposed method realizes highly accurate differential estimation near the desired frequency and sharp cutoff characteristics.



This paper presents an analytic design technique for 2D IIR filters with elliptical symmetry, which have useful applications in image processing. The design is based on efficient elliptic digital filters, regarded as 1D prototypes, to which specific complex frequency transformations are applied; this allows to obtain directly a factored form of the transfer function for the 2D elliptically-shaped filter. The design procedure uses some accurate approximations, but no global optimization algorithm. Finally the 2D filter matrices are obtained. The filter is adjustable in the sense that its coefficients depend explicitly on specified orientation and bandwidth. Another advantage is versatility, since the design need not be resumed each time from the start for various specifications. The designed 2D filters have an accurate elliptical shape with low distortions even close to the margins of frequency plane and are efficient, of high selectivity and relatively low order.

## Session C3L-B: Hardware and Cyber Security II

**Chair:** Shantanu Chakarbartty, *Washington University in St. Louis*
**Co-Chair:** Yingjie Lao, *Clemson University*
**Time:** Wednesday, August 8, 2018, 13:30 - 15:00
**Location:** Martis



While many techniques exist for detecting mechanical tampering in an integrated circuit supply-chain, estimating the time-of-occurrence of the tampering event has proven to be challenging. This work builds upon our previously demonstrated self-powered mechanical event detector and self-powered timing device to report a chip-scale system that can accurately timestamp the occurrence of the tampering event. The proposed system uses a combination of Fowler-Nordheim tunneling for continuous time-keeping and a linear hot-electron injector for sensing and recording of mechanical events. Using devices fabricated in a 0.5 um standard CMOS process, we demonstrate event time-stamping with an accuracy of 95% over a duration of 3 days. This accuracy can be further improved by incorporating a parametric model during the system calibration phase.



Advanced Metering Infrastructure (AMI) is the main player in today's Smart Grid, and Home Area Network (HAN) is an important subsystem in AMI. HAN connects the smart home appliances (SHA) inside the home to the smart meter (SM), which is connected to the power utility company. From the last decade, hardware Trojans (HT), have been extensively studied in both academia and industry. Consequently, the vulnerability of integrated circuits (ICs) against HTs leads to the potential security threat to any system that contains ICs, and HAN is no exception. However, to the best of authors knowledge, the potential effect of HTs on HAN has not been studied in the literature so far. In this paper, we are investigating HT in HAN network. In the process, we developed a testbed which can be scalable up to 127 nodes using I2C interface to control and implement any kind of required network behavior. We introduced three possible scenarios of HTs in this HAN network testbed. These scenarios illustrate the manifestation of HTs in the HAN that leads to network performance degradation.



Chaotic systems such as Lorenz functions have been proposed as cryptographic primitives for its divergence attribution. They are mostly used to generate random numbers, assist key agreements, and especially facilitate encryption processes. However in those applications, there are two important gaps in the use of chaotic functions: 1) their convergence attribution is seldom used; 2) their core secret - the system parameters, are statically fixed, which leads to potential vulnerabilities. Through filling the gaps, we have found certain interesting properties of the Lorenz chaotic systems. In this paper we propose an adaptive and dynamic authentication protocol based on discrete Lorenz chaotic systems. This protocol leverages both Lorenz function's divergence and convergence attributions in authentication, which makes it hard to track by attackers, but easy to verify by authenticators. This protocol also proposes in a novel way a dynamic configuration of the Lorenz functions' system parameters, so that the security of the protocol is further enhanced.



Generating pseudo-random sequence is an essential component of security and encryption tasks. Full-length sequences with large period, high output complexity is one of the most important requirements for the security and encryption applications. Different structures and various components are used in random number generators, include most notably, linear feedback shift register, non-linear feedback shift register, and pseudo-random chaos generators. In this paper by review and compare the features of each structure, a new design consists of non-linear feedback shift register and pseudo-random chaos generator is presented generating random numbers with high output quality. Output signal is noise-like and shows a good autocorrelation function and looks like a δ-function. Presented design has an appropriate random characteristic and with improvements compared with previous works.

Hash message authentication is a fundamental building block of many networking security protocols such as SSL, TLS, FTP, and even HTTPS. The sponge-based SHA-3 hashing algorithm is the most recently developed hashing function as a result of a NIST competition to find a new hashing standard after SHA-1 and SHA-2 were found to have collisions, and thus were considered broken. We used Xilinx High-Level Synthesis to develop an optimized and pipelined version of the post-quantum-secure SHA-3 hash message authentication code (HMAC) which is capable of computing a HMAC every 280 clock-cycles with an overall throughput of 604 Mbps. We cover the general security of sponge functions in both a classical and quantum computing standpoint for hash functions, and offer a general architecture for HMAC computation when sponge functions are used.

## Session C3L-C: Advancing Internet of Vehicles and Internet of Things

**Chair:** Ahmed Abdelgawad, *Central Michigan University*
**Co-Chair:** Shantanu Chakarbartty, *Washington University in St. Louis*
**Time:** Wednesday, August 8, 2018, 13:30 - 15:00
**Location:** Luna



Routing is very important for the overall performance of Internet of Things (IoT), which is known as the global network of smart objects. A smart object has a power source, a processing unit, sensors, and a radio module encompassed within. Since the vision of IoT is that everything (smart object) would be connected to the internet, the system would have to deal with low power and lossy networks (LLNs). To address the unpredictability of LLNs, Internet Engineering Task Force (IETF) standardized routing protocol for LLNs (RPL). Due to the overlap between the applications of LLNs and IoT, RPL is becoming the routing protocol for IoT, gradually. However, RPL struggles to provide desirable performance regarding energy-efficiency and reliability simultaneously. This paper focused towards obtaining decent links for information routing, and providing optimal transmission power while ensuring energy-efficiency. First, minimum rank with hysteresis objective function (MRHOF) was used and improved by proposing better parent switching hysteresis value to obtain a better link regarding received signal strength indicator (RSSI).



Embedded systems, such as IoT devices, benefit from low power sensors. We propose a fully-integrated proportional to frequency temperature sensing system. The temperature sensor replaces power hungry ADCs and on-chip time references with a frequency dependent digital output. The system consumes 195 nW, with 0.5 V power supply. The maximum temperature accuracy of 0.2 C is achieved across 0C to 50C in a total area of 0.008 mm2 in 130 nm technology. Experimental measurements of the temperature to voltage circuit is demonstrated, and post layout and Monte Carlo simulations verify the total system design meets performance requirements and is suitable for arrayed applications.



In our previous work, we had demonstrated a CMOS timer-injector integrated circuit for self-powered sensing of time-of-occurrence of mechanical events. While the sensor could achieve an improved time-stamping accuracy by averaging the output across over multiple channels, the mismatch between the channels made the calibration process cumbersome and time-consuming. In this paper, we propose the use of non-parametric machine learning techniques to achieve more robust and accurate event reconstruction. This is demonstrated using training and testing data that were obtained from fabricated prototypes on a 0.5-μm CMOS process; the model trained using Gaussian process regression can achieve an average recovery accuracy of 3.3% on testing data, which is comparable to the performance of using an averaging technique on calibrated injection results. The experimental results also validate that scalable performance can be achieved by employing more injection channels.

## Session C4P-E: Power Management and Hardware Security

**Chair:** Eugene John, *The University of Texas at San Antonio*
**Co-Chair:** Yingjie Lao, *Clemson University*
**Time:** Wednesday, August 8, 2018, 13:30 - 15:00
**Location:** Poster Area

Random Number Generators (RNGs) are crucial for many security applications for generating unpredictable bit streams. Fully digital Random Number Generators which are implemented in FPGA platforms are usually preferred for their high speed convenience and easy integration to digital platforms. On the other hand, attention should be paid while placing and routing ring oscillators as much as possible. This paper presents implementation of a Random Number Generator based on ring oscillators on FPGA and cryptanalysis of it via correlation analysis. The main aim of this paper is to analyze the correlation between RNG and the attack circuit when coupled to the main circuit. In the main RNG circuit all ring oscillators are placed separately to obtain independent random bit streams at the output. Experimental results show that effective correlation between RNG and attack circuit can be obtained due to coupling.

## Session C5L-A: Communication Systems

**Chair:** Yvon Savaria, *Polytechnic Montreal*
**Time:** Wednesday, August 8, 2018, 15:30 - 17:00
**Location:** Mercuri



Increasing throughput requirements for Internet routers and growing routing table sizes have emphasized the need for fast and scalable packet forwarding systems. This paper presents a hardware cache-based IPv6 lookup system. Our goal is to study how much performance can be achieved with a lookup system that is implemented by modifying a processor cache. We show by prototyping our system on an FPGA board that our solution provides efficient IPv6 packet forwarding. In particular, hardware complexity grows only linearly with table size. Also, our basic FPGA implementation can support a 1Gb link for minimum sized packets, while an improved implementation could improve this throughput by an order of magnitude. Finally, an ASIC implementation would support 100Gb of bandwidth if there were no other bottleneck in the system.



This paper presents a temperature analysis for NFC-powered Lab-on-Chip (LoC) solutions. It is based on a monolithically implemented LoC and uses a 130 nm standard CMOS process. An application-independent temperature gathering mesh is implemented on the chip substrate. It allows a real time NFC-caused temperature analysis. Measurement data regarding heat spreading, the influence of the glob top, and the effect of the PCB layout is presented. A warming reduction from 23.05°C to 3.8°C using the same power source is achieved. Detailed data on the temperature gradient over time for warming and cooling is also provided.



One of the important upcoming and futuristic re- quirement noticed from radio interface specifications is the need of performing datapath processing on the mapped samples. The integration of datapath processing needs special circuitry to take care of the delays in the mapping. This paper presents a scalable architecture to efficiently integrate the datapath processing with mapping logic of data link layer in a radio interface.



In This Paper,Realization of Inverter Latch Is Proposed Through an All-Optical Cascadable Tri-State Buffer As a Sequential Circuit Which Is Designed with Mach-Zehnder Interferometer(MZI).This Sequential Circuit Is Assembled Based on Electro-Optic Effect and Is Verified by Simulation. The Applications of Tri-State Buffer for Optical Data Transfer and the Advantage of Using This Circuit As an Octal Tri State Buffer Over the Currently Existing ICs Has Been Explained.

## Session C5L-B: Reconfigurable Architecture

**Chair:** Mohammed Khalid, *University of Windsor*
**Time:** Wednesday, August 8, 2018, 15:30 - 17:00
**Location:** Martis



In recent years, a new CAD tool called Intel FPGA SDK for OpenCL allowed fast and efficient design of FPGA-based hardware accelerators from high level specification such as OpenCL. In this paper, IFSO is used to explore acceleration of k-Nearest-Neighbor (kNN) algorithm using FPGAs. The optimized algorithm was implemented on two different FPGAs (Intel Stratix A7 and Intel Arria 10 GX). Experimental results show that the FPGA-based accelerators provided up to 80X speedup and 83% reduction in power consumption than a traditional workstation based on two Intel Xeon processors E5-2620 Series (each with 6 cores and running at 2.4 GHz).



This work presents a reconfigurable embedded implementation of a fly-inspired edge detection algorithm that allows for run-time alteration of the numerical format in response to constraints on accuracy or resources. The low-resource, high-performance system can effectively detect edge orientation and location. This work illustrates the advantages of run-time reconfiguration technology for the implementation of fly-inspired vision algorithms whose capabilities can surpass or supplement traditional image processing systems.



In this paper, a vision-based target detection system using an Unmanned Aerial Vehicle (UAV) is developed to execute a mission plan. The mission plan is to autonomously take off to a specified altitude, fly to a waypoint with a predefined GPS coordinate, locate the target displayed by an AprilTag, hover above the target, then descend and land near the target. Our result shows that AprilTag is highly viable in UAV vision-based target detection.



The state-of-the-art FPGAs require massive configuration files seeking on-chip large memory storage. Partial reconfigurable applications demand even more data storage for the additional several partial bitstreams. To alleviate the memory storage requirements, bitstream compression techniques are needed. Efficient compression algorithms usually involve high complex hardware decompression circuits. This might increase the FPGA's (re)configuration time. In run-time reconfigurable applications, the required time of the decompression engine must be reduced. In this paper, we present a design and implementation of a newly developed bitstream decompression algorithm. The decompression circuit was implemented using Xilinx Vivado EDA design suite on a Zynq-based FPGA. While consuming only 118 CLB slices, 0.89% of the fabric, the decompression speed can reach the theoretical maximum reconfiguration frequency of 400 MB/s on 100 MHz clock as verified by hardware implementation. Furthermore, the effect of the FIFO buffer size and DMA configuration parameters on the decompression speed were studied.

## Session C5L-C: Diagnostics and Fault Tolerant Control System II

**Chair:** Roozbeh Razavi-Far, *University of Windsor*
**Time:** Wednesday, August 8, 2018, 15:30 - 17:00
**Location:** Luna



This study is devoted to robust state estimation and fault detection for nonlinear discrete fractional order systems using a novel fractional order filter algorithm. While noise and disturbance effects can suppress or even disturb the state estimation, the proposed filter can preciously estimate the states of nonlinear fractional order systems. Disturbance decoupling approach is the fundamental basis for the proposed filter to make it robust against unknown inputs. Simulation results illustrate the advantages of the proposed filter for state estimation and fault detection of nonlinear fractional order systems in the presence of both noise and disturbance.

**Design and Implementation of an Ultrasonic Link for Concurrent Telemetry of Multiple Data Streams to Implantable Biomedical Microsystems** ..... 1090
*Keivan Keramatzadeh (K.N. Toosi University of Technology), Amir M. Sodagar (York University)*

This paper reports on the design, implementation, and test of an ultrasonic data telemetry link. The link benefits from the combination of on-off keying (OOK) modulation and frequency-division multiplexing (FDM) in order to enhance the telemetry data rate, while using regular transducers. As a result of using the FDM scheme, multiple data streams will be telemetered via the link concurrently. Each one of the data streams is OOK-modulated with a specific sub-carrier frequency. Covering the breadth of the effective bandwidth of the link, the subcarrier frequencies are chosen to be located at the local maxima of the link frequency response. To further increase the data rate, the OOK-modulated data streams are amplitude-equalized to compensate for the non-flat frequency response of the link. Designed using two ultrasonic transducers with a resonance frequency of 1MHz placed with a spacing of 3cm, a prototype link with 8 concurrent sub-channels was developed, characterized, and tested for a bit rate of 120kbps.

**A Non-Invasive Characterization Method for MEMS based Devices** ..... 1094
*A Panahi (University of Tehran / York University), E. Ghafar-Zadeh (York University), S. Magierowski (York University), M. Sabour (University of Tehran)*

In the MEMS industry, it is imperative to characterize the fabricated die and test the functionality of its mechanical subcomponents. This paper presents a novel noninvasive characterization method for MEMS devices using aerodynamic forces. These forces are applied onto a desired part of a MEMS sensor to stimuli the moveable components and subsequently analyze its functions. In this approach, we use a micro-fabricated cantilever array chip as a case study of our proposed method. In this paper, we outline the proposed method and then demonstrate and discuss its multiphysics simulation results. The research results and discussions in this paper pave the way towards the development of a noninvasive rapid and low complexity air-based characterization system for MEMS devices.

**FPGA-Based DNA Basecalling Hardware Acceleration** ..... 1098
*ZhongPan Wu (York University), Karim Hammad (York University / Arab Academy for Science, Technology and Maritime Transport), Robinson Mittmann (York University), Sebastian Magierowski (York University), Ebrahim Ghafar-Zadeh (York University), Xiaoyong Zhong (Shanghai Aerospace Ltd. Co.)*

Modern DNA sequencing technologies have greatly reduced their physical dimensions while still being able to process large numbers of molecules. Under ideal conditions the raw throughput of such devices may peak at the equivalent of 1 human genome per 3.5 hours. Such outputs present a large burden on the ensuing computing devices tasked with processing the raw data and completing the sequence. To approach the power and spatial footprint of the measurement devices, hardware-accelerated embedded computers are needed. The design of an FPGA-based accelerator customized for one aspect of this task – basecalling – is described herein. Simulations indicate a system capable of basecalling the equivalent of one human genome in 35 minutes within an estimated power budget of 10 W.

## Session C6P-E: Late Breaking News

**Chair:** Masud Chowdhury, *University of Missouri at Kansas City*
**Co-Chair:** Arezoo Emadi, *University of Windsor*
**Time:** Wednesday, August 8, 2018, 15:30 - 17:00
**Location:** Poster Area

**Majority and Minority Voted Redundancy for Safety-Critical Applications** .....
*P. Balasubramanian (Nanyang Technological University), D.L. Maskell (Nanyang Technological University), N.E. Mastorakis (Technical University of Sofia)*

A new majority and minority voted redundancy (MMR) scheme is proposed that can provide the same degree of fault tolerance as N-modular redundancy (NMR) but with fewer function units and a less sophisticated voting logic. Example NMR and MMR circuits were implemented using a 32/28nm CMOS process and compared. The results show that MMR circuits dissipate less power, occupy less area, and encounter less critical path delay than the corresponding NMR circuits while providing the same degree of fault tolerance. Hence the MMR is a promising alternative to the NMR to efficiently implement high levels of redundancy in safety-critical applications.

**Novel CNTFET and Memristor based Unbalanced Ternary Logic Gate** ..... 1106
*Mahmood Uddin Mohammed (University of Missouri – Kansas City), Rakesh Vijjapuram (University of Missouri – Kansas City), Masud H Chowdhury (University of Missouri – Kansas City)*

Multi-valued logic (MVL) gates are expected to be the future platforms for the beyond-binary circuits and systems. We propose a novel standard ternary inverter (STI) design based on carbon nanotube FET (CNTFET) and memristor. One of the advantages of the proposed design is the fact that the threshold voltage of the CNTFET can be adjusted by varying the chirality vector. Memristor behaves like a resistor outside a certain frequency range and it has the potential to offer significantly lower leakage and power dissipation compared to the conventional resistor. Performance and stability of the proposed design have been compared to the existing CNTFET based design. Power delay product of the proposed STI has been improved by 16.37 times and 65.48 times, and the static noise margin of the proposed STI is 96.28% and 95.43% better compared to designs proposed in [4] and [7], respectively.