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Chair: Mohammad Haider, *University of Alabama at Birmingham*

Co-Chair: Mitra Mirhasani, *University of Windsor*

Time: Monday, August 6, 2018, 8:30 - 10:00

Location: Mercuri

Behavioral Model for a High-Speed 2:1 Analog Multiplexer 1

Christian Schmidt (Fraunhofer Heinrich Hertz Institute / Technical University of Berlin), Patrick Zielonka (Fraunhofer Heinrich Hertz Institute / Technical University of Berlin), Volker Jungnickel (Fraunhofer Heinrich Hertz Institute), Ronald Freund (Fraunhofer Heinrich Hertz Institute / Technical University of Berlin), Tobias Tannert (University of Stuttgart), Markus Grözing (University of Stuttgart), Manfred Berroth (University of Stuttgart), Friedel Gerfers (Technical University of Berlin)

A novel concept for digital-to-analog converters (DACs) has been introduced recently, to overcome their bandwidth limitations by combining the outputs of multiple DACs with an analog multiplexer (AMUX). In this paper, a behavioral model for a high-speed 2:1-AMUX is introduced, which significantly reduces the simulation time for a 2:1-AMUX-DAC system. The behavioral model is implemented in Matlab and fitted with simulation data from an electronic design automation tool for a high-speed 2:1-AMUX integrated circuit with a normalized mean square error < -20 dB. Eventually, multiple model parameters are varied in order to study their impact on the system's behavior.

A 30 Gb/s High-Swing, Open-Collector Modulator Driver in 250 nm SiGe BiCMOS 5

Alexandru Giuglea (Technische Universität Dresden), Guido Belfiore (Technische Universität Dresden), Mahdi Khafaji (Technische Universität Dresden), Ronny Henker (Technische Universität Dresden), Frank Ellinger (Technische Universität Dresden)

This paper presents a modulator driver realized as a breakdown voltage doubler which can provide a high output swing of 7.6 V_{pp,diff} for load impedances as low as 30 Ohm, thus overcoming the limitation imposed by the collector-emitter breakdown voltage. The open-collector design gives an important degree of freedom regarding the modulator load to be driven, while significantly reducing the circuit's power consumption. The driver is capable of running at 30 Gb/s while dissipating 1 W of DC power. Thanks to the inductorless design, the active area occupied by the circuit is only 0.28 mm x 0.23 mm. The driver was realized in a 250 nm SiGe BiCMOS technology.

On a Class of Quadrature Phase Oscillators using Differential Pairs 9

B.J. Maundy (University of Calgary), A.S. Elwakil (University of Sharjah), C. Psychalinos (University of Patras)

A new class of quadrature phase oscillators based on cross-coupled differential pairs is introduced. This class contains eight possible circuits which produce four output voltages with phase differences of ± 90 or ± 180 degrees, depending on the choice of output node, and does not require balanced differential-pair loads. Phase error analysis is provided along with experimental and simulation results using discrete MOS and BJT transistors as a proof of concept.

Synthesis of a Family of Differential Cross-Coupled Oscillators and Design Application 13

B.J. Maundy (University of Calgary), A.S. Elwakil (University of Sharjah), M.B. Elamien (University of Calgary), A. Al-Hammadi (University of Sharjah)

A class of differential oscillators comprising ten possible circuits is introduced in this work. Half of the members of this family are LC-based oscillators and the other half are RC-based ones. While all oscillators are second-order, a maximum of four resistors was imposed as a restriction on possible oscillators that belong to the proposed architecture. Only two of the found oscillators are canonical but all members of the this family have unique and attractive design features. Experimental results using discrete components verify the operation of selected circuits designed for short distance citizen band communication devices. Further, a MOS-C version of one of the oscillators is designed and tested in a CMOS 90nm technology.

Ultra Low Power Class-AB Voltage Mode Line Driver for Fast Ethernet 17

Simon Buhr (Technische Universität Dresden), Martin Kreißig (Technische Universität Dresden), Florian Protze (Technische Universität Dresden), Frank Ellinger (Technische Universität Dresden)

A low power CMOS voltage mode line driver for Fast Ethernet has been designed in a 180nm low cost technology from GlobalFoundries. Very low power consumption is achieved by using a voltage mode approach with a low power rail-to-rail operational amplifier (opamp). Using a Class-AB output stage further reduces the power consumption. While transmitting pseudo random data the power consumption is measured to be only 24mW which is to the best of the authors knowledge the lowest power consumption reported to date for such a line driver.

Session A1L-B: VLSI Low Power Digital Circuits

Chair: Arezoo Emadi, *University of Windsor*

Time: Monday, August 6, 2018, 8:30 - 10:00

Location: Martis

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Hader E. El-hmaily (Badr University), Rabab Ezz-Eldin (Beni-Suef University), A.I.A. Galal (Minia University), Hesham F.A. Hamed (Minia University)

Robust GNERFET/MOSFET Conjunction is employed to build various power gating structures using 16nm technology. The evolved Power Gating (PG) structure is composed of GNERFET as a footer sleep transistor and Silicon CMOS logic power gated module. The proposed structure resolves the main drawbacks of the traditional PG design from the point of view increasing the propagation delay and wake-up time in low-voltage regions. Leakage power, rush current, wake-up time and power delay product are used as the performance circuit parameters for the evaluation. The performance results of the proposed power gating structure with single footer reveals a reduction in leakage power, delay time, and wake-up time, on average up to 88%, 44%, and 24%, respectively, for different logic circuit modules compared to the MOSPG structure.

Comparative Performance Analysis of Dual-Rail Domino Logic and CMOS Logic under Near-Threshold Operation 25

Tsuyoshi Maruyama (Keio University), Mototsugu Hamada (Keio University), Tadahiro Kuroda (Keio University)

This paper compares designs of an asynchronous dual-rail domino logic (DRDL) and the conventional CMOS logic under near-threshold operation. The delay time and energy consumption of an 8-bit full adder are simulated by HSPICE with a 180nm CMOS technology. The results show, considering the process variations, DRDL is faster than CMOS below 1.1V. The delay performance of DRDL at 0.25V is equivalent to that of CMOS at 0.4V, when the energy-delay product of DRDL is 40% smaller than that of CMOS.

Low Power Digital Temperature Sensor using Modified Inverter Interlaced Cascaded Delay Cell 29

Yun Seok Hong (Northeastern University), Yong-Bin Kim (Northeastern University)

Sensing temperature for localizing hot spots provides additional observability in modern integrated circuits. A digital temperature sensor with modified inverter interlaced cascaded delay cells (IICDCs) is presented in this paper. Temperature is sensed using a temperature-to-pulse generator that produces pulse with an XOR gate and a temperature dependent delay line with the modified IICDCs. A D flip-flop based T flip-flop is used to produce a pulse used as the input signal of the delay line, and the inverted input signal is used to reduce the offset of temperature sensor. The output of the temperature-to-pulse generator is applied to a time-to-digital converter (TDC) to achieve digital codes of the sensed temperature. By using the modified IICDCs, it is possible to consume lower power than the conventional approach using the inverter-based delay lines. The temperature sensor is designed with 180 nm CMOS technology and 1.8 V supply voltage. This temperature sensor circuit consumes 324 μ W and monitors -20 $^{\circ}$ C to 110 $^{\circ}$ C with a good linearity.

All Digital Low Power Aging Sensor for Counterfeit Detection in Integrated Circuits 33

Enahoro Oriero (Tennessee Technological University), Syed Rafay Hasan (Tennessee Technological University)

The globalization of the integrated circuit (IC) design flow has led to increased security vulnerabilities. Modern IC supply chain consists of multiple untrusted entities which makes it vulnerable to potential compromise by attackers, who can insert counterfeit ICs at any stage in the supply chain. The deployment of counterfeit ICs threatens the security and reliability of electronic components and systems. For this reason, it is imperative to mitigate these risks by developing robust counterfeit IC detection techniques. In this paper, we investigated the viability of a completely digital design technique for identifying counterfeit ICs by exploiting changes in the threshold voltage. We introduce a solution that is based on the premise that a recycled/remarked or reused IC exhibits a degraded threshold voltage (V_t) that leads to changes in the timing characteristics of CMOS designs. In contrast to currently available counterfeit IC detection techniques, the proposed method measures IC degradation after it has been used and does not require a reference IC to provide a baseline signature. We propose a robust aging sensor for detecting changes in V_t with a sensitivity of about 5%.

An Adaptive Dynamic-Element PTA Method for Solving Nonlinear DC Operating Point of Transistor Circuits 37
*Zhou Jin (China University of Petroleum), Meiping Liu (China University of Petroleum),
Xiao Wu (Waseda University)*

Pseudo-transient analysis (PTA) method has been researched for many years from the practical viewpoint since it is considered as the most promising method to find DC operating point for transistor-level circuits, which is the most fundamental and difficult task in circuit simulation. However, in many cases, especially for some large-scale circuits or combination circuits which contain different kinds of sub-circuits, different nodes may require different pseudo-capacitor values to converge. Same-rate of step size and capacitor values for all nodes may lead to nonconvergence. In this research, an adaptive dynamic-element algorithm is proposed for PTA method, which inserts dynamic pseudo-element to each transistor respectively, and the values vary according to the simulation states independently and automatically. Numerical examples are shown to illustrate the effectiveness and efficiency of proposed algorithm.

Session A1L-C: Bioengineering Systems and Biochip

Chair: Mohamad Sawan, *Polytechnic Montreal*

Co-Chair: Ming-Dou Ker, *National Chiao Tung University, Taiwan*

Time: Monday, August 6, 2018, 8:30 - 10:00

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A MEMS Outer Hair Cell (OHC) Implant to Improve Sensorineural Response of a Damaged Cochlea 41
*Mahsasadat Seyedbarhagh (University of Windsor), Sazzadur Chowdhury (University of Windsor),
Mehrddad Saif (University of Windsor)*

This paper presents the design of a MEMS based Outer Hair Cell (OHC) for use as a prosthetic implant on the top of the basilar membrane in the Cochlea to improve the hearing conditions for persons with damaged OHC. The MEMS hair cell (OHC) is designed to have a set of 6 variable length microfabricated cantilever beams that can be excited to deform like normal healthy OHC using electrostatic actuation. A 3D Finite Element Analysis (FEA) of the developed OHC has been carried out using IntelliSuite. The FEA results are in 17% agreement with an analytical model published elsewhere. The design eliminates the use of electrode as used in conventional cochlear implants (CIs) and has the potential to improve the hearing condition for patients suffering from sensory neural hearing loss due to cochlear outer hair cell damage.

H-Field Probe with Active Balun for MRI-Conditional Testing of Medical Devices 45
Ali Attaran (Western University), William B. Handler (Western University), Blaine A. Chronik (Western University)

This work presents the design and construction of a H-field probe with active balun for MRI (magnetic resonance imaging) conditional testing of medical devices. The H-field probe was designed using a small loop antenna with 2 mm radius to have high spatial resolution and sensitivity. It was tuned and matched at a center frequency of 128 MHz, which corresponds to 3 T MRI systems or equivalent RF exposure systems. An active balun with a gain 18.28 dB and noise figure of 0.5 dB was employed to boost the detected H-field signal level. The designed Hfield probe and active balun have been fabricated on a double sided printed circuit board (PCB), FR4 thickness of 1.57 mm and a copper thickness of 35 μm , with overall footprint of 22 mm \times 11 mm.

Design of Multi-Channel Monopolar Biphasic Stimulator for Implantable Biomedical Applications 49
Chia-Chi Hsieh (National Chiao Tung University), Ming-Dou Ker (National Chiao Tung University)

Neuro-stimulators have been widely used in neural disorder control. This work presents a four-channel stimulator with adjustable positive and negative stimulus voltage from +/- 0.5V to +/- 8V. In the proposed stimulator, circuit operation with negative voltage has been successfully realized in a 0.25- μm 2.5V/5V/12V CMOS process with the grounded p-type substrate, and without suffering the p-n junction breakdown or electrical overstress issues. The proposed stimulator has been also practically verified with in-vivo animal test. By integrating the stimulator circuit with other circuit blocks together, the close-loop neuromodulation treatment can be implemented by an implantable system-on-chip (SoC) with low-power consumption.

Arterial Viscoelastic Model using Lumped Parameter Circuit with Fractional-Order Capacitor 53
*Mohamed A. Bahloul (King Abdullah University of Science and Technology), Taous Meriem Laleg-Kirati (King
Abdullah University of Science and Technology)*

In this work, we explore the fractional viscoelastic properties of the arterial blood vessel, and present a fractional-order lumped parameter model. We refer to this model as arterial fractional order visco-elastic (AFV) model. A novel feature of this characterization is that the ideal analog parameter displaying the arterial compliance in the well known windkessel model, has been replaced by a fractional order element (Fractional Capacitor). It displays the complex and frequency dependent total arterial compliance by combining both resistive and capacitive properties that exhibit the fractional viscoelastic behavior of the vessel wall. The contribution of both characteristics is controlled by a fractional differentiation order parameter (α) enabling an accurate and real physiological description. The proposed model offers a pioneer way for the better interpretation of the viscoelastic effect on the arterial hemodynamic. In addition, it can be investigated as a reliable computer-based simulation platform for cardiac pathophysiology diagnosis and treatment.

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<i>Sina Parsnejad (Michigan State University), Yousef Gtat (Michigan State University), Tung-Yi Lin (Michigan State University), Xiyuan Liu (Michigan State University), Peter B. Lillehoj (Michigan State University), Andrew J. Mason (Michigan State University)</i>	

This paper presents a self-ranging, multichannel, multi-technique electrochemical instrument with the size, power, and performance suitable for wearable applications, such as point-of-care sensing. It comprises a custom analog interface and a commercial low-power microcontroller and hosts two independent readout channels that are capable of dynamically adjusting to a wide range of input currents exhibited by various electrochemical sensors. To evaluate its functionality and versatility, the system was tested with multiple sensors using multiple electrochemical methods and was benchmarked against two commercial electrochemical instruments. While occupying only 8.5 cm³ and consuming an average active power of 250 mW, the instrument provides nearly 10-bit accuracy over a 115 dB dynamic operational range and matches benchtop instrument results within 1.8%, demonstrating its capability to serve as a universal wearable electrochemical instrument.

Session A1L-D: Hardware Implementation of Neural Network and Neuromorphic Computing

Chair: Vishal Saxena, *University of Idaho*

Co-Chair: Ayman Fayed, *The Ohio State University*

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Location: Saturni

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<i>Karlheinz Ochs (Ruhr-University Bochum), Dennis Michaelis (Ruhr-University Bochum), Sebastian Jenderny (Ruhr-University Bochum)</i>	

Neuromorphic circuits are seen as a potential candidate to mimic the behavior of biological networks. Memristive devices for such networks are hard to find for a specified functionality. We exploit an emulation technique that enables for parameter optimization, supporting the finding of hardware realizations and reducing development efforts. In this paper, we demonstrate this by digitally replicating a Morris-Lecar neuron with the wave digital concept. The parameters of this model are optimized with respect to hyperpolarization. Although we focus on a small neuromorphic circuit here, our procedure is also suited to emulate larger circuits in real-time.

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<i>Jafar Shamsi (Iran University of Science and Technology), Shahriar B. Shokouhi (Iran University of Science and Technology), Karim Mohammadi (Iran University of Science and Technology)</i>	

Brain-inspired computing uses the human brain capability to introduce tools for high performance and robust computing. Recently, a brain-inspired associative memory with large capacity and robust retrieval has been introduced, which is called Columnar Organized Memory (COM). It comprises spiking winner-take-all (WTA) networks, that is a basic building block of the neocortex. The upper bound capacity of a COM has been calculated previously. However, the simulation result is not provided to show the actual capacity of an implemented COM. In this paper, the capacity of a COM is evaluated through the simulation. The simulation results show that the capacity of a COM is linearly related to the capacity of the spiking WTA.

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<i>Niusha Gomar (Kermanshah University of Technology / University of Windsor), Behzad Moradi (Kermanshah University of Technology), Majid Ahmadi (University of Windsor)</i>	

Central Pattern Generator (CPG) plays a key role in controlling the locomotion part of the animals. Bio-inspired CPGs can be employed in many robotic and control applications. A digital hardware implementation of a central pattern generator based on Hindmarsh-Rose (HR) neuron model is presented in this paper. Aiming an efficient implementation, the neuron module is implemented using multiplier-less Piecewise Linear (PWL) method. The CPG network is built by coupling HR neuron modules to produce the anti-phase patterns in the output of the network. The system has been developed by Hardware Description Language (HDL) and synthesized based on an Altera FPGA. Synthesis results for a block of CPG indicate that it takes less than 1% of the resources of a Stratix IV Altera FPGA for the proposed system. The results have been compared for the proposed digital hardware and the original CPG implementation. Also, hardware implementation results verify that the system

Mimicking Gait Pattern Generators 73

*Karlheinz Ochs (Ruhr-University Bochum), Dennis Michaelis (Ruhr-University Bochum),
Sebastian Jenderny (Ruhr-University Bochum)*

An important question when replicating biologically inspired networks is to model the synaptic interconnections between neurons. Biological representations often use unidirectional couplings between neurons. This waives problems on electrical models since electrical circuits are in general not free from feedback. We propose a solution based on a four-port circulator to overcome this issue. The method involves attaching appropriate resistances to this circulator, depending on the desired coupling. The wave digital representation of this approach reveals that our modeling enables true unidirectional interconnections between neurons. We use this method to investigate multiple gait pattern generators of a four-legged animal.

Session A2P-E: Analog Design Applications

Chair: Mitra Mirhasani, *University of Windsor*

Co-Chair: Igor Filanovsky, *University of Alberta*

Time: Monday, August 6, 2018, 8:30 - 10:00

Location: Poster Area

A Monotonically Linear DCO for 77 GHz Automotive Radars 77

Iman Taha (University of Windsor), Mitra Mirhassani (University of Windsor), Arezoo Emadi (University of Windsor)

This paper presents a 77 GHz CMOS Monotonically Linear Digitally Controlled Oscillator (ML-DCO) that is derived from a Colpitts topology. A new tuning mechanism is developed that alleviates the need for an ideal switch and assures linearity. Large nonlinear varactors are avoided, and the ML-DCO achieves 5 GHz linear tuning range that fulfills the requirements for short range and long range automotive radar sensors. The ML-DCO consumes a maximum of 9.12 mW and achieves a phase-noise of -98.53 dBc/Hz at a 1MHz offset frequency. The ML-DCO demonstrates

Modifying the Wideband Amplifier Step Response using “Phantom Immittances” 81

I.M. Filanovsky (University of Alberta)

The paper considers a new method of modifying the transfer function denominator polynomial of a wideband amplifier to obtain a desirable overshoot. The method assumes that this initial polynomial is stable, and, using even and odd parts of this polynomial, one finds the ladder impedance or admittance which is called “phantom immittance”. The modification of this immittance by introducing the resistances in series with the coils or in parallel with the capacitors changes the oscillating properties (damping and transient duration) of the immittance. The modified immittance numerator may be used as the transfer function denominator of the modified amplifier. The examples which illustrate the approach are taken from adapting for amplifier design the Butterworth or Bessel polynomials. In addition, a new property of immittance two-ports involving the Bessel polynomials is formulated.

Relationship Between Time-Constants and 3dB Cutoff of High-Order Damped LTI Systems 85

Vladimir Prodanov (California Polytechnic State University),

Katherina Prodanov (California Polytechnic State University)

This paper deals with linear time-invariant (LTI) systems and examines the link between the 3dB cutoff and time-constants. It shows that the cutoff frequency of a low-pass damped network can be estimated from the reciprocal of a p-norm calculated from the system’s time-constants. Furthermore, to achieve good accuracy the p factor must have a fractional value, for example, $p = 1.7$. Two formulas are derived, and their performance evaluated using Monte Carlo simulations which reveal a sub-3% error for most cases.

Influence of CMOS CCII Parasitics in Realization of Two-Integrator Band-Pass Filter 89

Edi Emanovic (University of Zagreb), Drazen Jurisic (University of Zagreb),

George S. Moschytz (Bar-Ilan University)

In this paper we examine the influence of CMOS CCII non-idealities in an IC realization of a two-integrator Biquad. We compare two CMOS-CCII realizations of the Biquad; the same basic topology of the translinear CCII, but the W/L ratios of their transistors are optimized differently. One CCII possesses fewer non-idealities, while the other operates at higher frequencies. It is shown how the CCII nonidealities, causing lossy integrators, are applied in the Biquad design. Realizability constraints are given. With the example of a fourth-order 1MHz/100kHz BP filter, post-layout simulations with AMS 0.35-micron technology using Cadence, show close agreement with our analysis.

A 2.8 GHz to 12.8 GHz UWB LNA using Transformer Wide-Band Input Matching for IR-UWB Radar Applications 93

Xin An (Technische Universität Dresden), Jens Wagner (Technische Universität Dresden), Frank Ellinger (Technische Universität Dresden)

A cascode ultra-wideband (UWB) low noise amplifier (LNA) with a transformer for input matching was implemented in 45nm RF-SOI CMOS technology. The transformer is applied with high coupling ($k = 0.7$ to 0.8) for acquiring a stable wide band input impedance and so that a flat gain, return loss, noise figure, etc. in the whole UWB band is provided. The LNA affords a maximal power gain (S_{21}) of 12.5 dB and a -3 dB bandwidth of 10 GHz from 2.8 GHz to 12.8 GHz. It possesses low noise ($NF_{min} = 2.9$ dB) and a high 1 dB input compression point (IP_{1dB} is -6 dBm to 2 dBm). The LNA occupies a small chip area of 0.14 mm² without bond pads and consumes 11.7 mW from a 1 V supply.

A Comparative Study of Injection Locked Frequency Divider using Harmonic Mixer in Weak and Strong Inversion 97

Yushi Zhou (Lakehead University), Jared Mercier (Lakehead University), Fei Yuan (Ryerson University)

This paper presents a comparative study of a divide-by-4 injection locked frequency divider with the injection transistor operating in both the weak and strong inversion regions. The relation between the maximum lock range of the frequency divider and the nonlinearity of the injection transistor is investigated. We show that the strong nonlinear characteristics of the injection transistor induce the wider lock range. We further investigate the existence of the optimum biasing point in the weak inversion region, which leads to the maximum lock range given the same injection power. The injection locked frequency divider designed in GF 130 nm 1.2 V CMOS technology, is validated using the simulation results.

A Third-Order Band-Pass Fully-Passive Noise-Shaping Modulator based on a Time-Interleaved SAR ADC 101

Zhiyuan Dai (Fudan University), Hang Hu (Fudan University), Yimin Wu (Fudan University), Fan Ye (Fudan University), Junyan Ren (Fudan University)

This paper proposes a third-order band-pass fully-passive noise shaping modulator based on a time-interleaved successive approximation register (SAR) ADC for ultrasonic imaging. It combined SAR ADC with time-interleaved ADC to transfer the centre frequency from DC to $fS/4$ where fS is the sampling rate of ADC in passive way with low power consumption. It achieves SNDR of 75.81dB with the bandwidth from 40MHz to 60MHz and its FoMw is only 10.91fJ/conv.step in simulation which is lower than conventional band-pass modulators.

A 28 GHz Q-Tunable Fully Differential Bandpass Filter in 65-nm CMOS Technology 105

M.B. Elamien (University of Calgary), B.J. Maundy (University of Calgary), L. Belostotski (University of Calgary), A.S. Elwakil (University of Sharjah)

In this paper, we present a fully differential band-pass filter design topology. It is based on the generic two transistor differential pair, common-drain structure and three surrounding impedances Z_1 , Z_2 and Z_L . Ten selected samples of possible bandpass filters based on various choices of $Z_{1,2,L}$ are also presented. Selected designs with Q-tunable features are constructed and experimentally verified at low-frequency. Furthermore, simulation results in Cadence using 65-nm CMOS technology are also provided at a 28GHz center frequency.

A Fully Integrated Floating Gate Driver with Adaptive Gate Drive Technique for High-Voltage Applications 109

Zekun Zhou (University of Electronic Science and Technology of China), Junyuan Rong (University of Electronic Science and Technology of China), Jianwen Cao (University of Electronic Science and Technology of China), Dengwei Li (University of Electronic Science and Technology of China), Bo Zhang (University of Electronic Science and Technology of China), Yue Shi (Chengdu University of Information Technology)

This paper presents a fully integrated floating gate driver using adaptive gate drive technique (AGDT). Without the breakdown risk of thin-gate-oxide devices in high-voltage applications and the requirements for complex bootstrap structures in dual NMOS power trains, the proposed floating gate driver, based on current source driving with active-clamping-module (ACM), can shift up driving signal from low voltage range to wide range high voltage output. Compared with previous designs, it consumes no static current and requires no off-chip capacitor for bootstrap nor off-chip power diode for asynchronous rectification, which can enhance efficiency of whole system. Implemented in standard $0.35\mu\text{m}$ 30V BCD process and using thin-gate-oxide PMOS as high-side power transistor, measurement results demonstrate that the proposed gate driver can provide effective output signals in 8~25V wide range output.

Excess Bias Voltage Monitoring Circuit 113

Nenad Lilic (ams AG), Robert Kappel (ams AG), Georg Roehrer (ams AG), Horst Zimmermann (Technische Universität Wien)

For time-of-flight applications where Single Photon Avalanche Photodiode is used as optical sensor, the control of the excess bias voltage (VEX) is very important. All SPAD parameters are function of temperature and VEX. If this voltage is not controlled, it can happen that SPAD devices are in off state, or that distance measurements are different for different temperature conditions. To avoid this, an excess bias voltage monitoring circuit is described. This circuit is integrated as part of the excess bias voltage monitoring system, that adjusts VEX to predefined value for all temperature conditions.

A Cascaded Thermometer-Coded Current-Steering Digital-to-Analog Converter 117

Nenad Lilic (ams AG), Peter Speer (ams AG), Horst Zimmermann (Technische Universität Wien)

A digital to analog current steering converter suitable for low voltage applications is described. The power and layout area reduction compared to state of the art, show outstanding advantages of the described topology.

A 47mW Two-Dimensional Eye Opening Monitor for Multi-Protocol SerDes 121

Wenhuan Luan (Tsinghua University), Ting Chen (Digital Switching System Engineering and Technological Research Center), Shuai Yuan (Tsinghua University), Peijie Li (Digital Switching System Engineering and Technological Research Center), Ziqiang Wang (Tsinghua University), Xin Lin (Tsinghua University), Mao Li (Tsinghua University), Dengjie Wang (Tsinghua University), Hong Chen (Tsinghua University)

This paper presents an eye opening monitor (EOM) architecture designed for multi-protocol serial link applications, which is operated at the data rate of 1.25-10Gb/s. The proposed two dimension EOM provides the variable 248 different masks, based on the phase interpolators (PIs) and the digital-to-analog converters (DACs). The horizontal asymmetric masks are also closer to the real eye. The EOM is achieved in 40nm CMOS technology and supplied with 1.1V. The simulated results show that this design can output a frequency corresponding to the bit error rate (BER). The algorithm that is controlled by digital control logic block V_Control and PI_Control can implement traversal of the variable asymmetric sizes of masks. The total power consumption of the EOM is 47 mW at 10Gb/s in this design.

A Comprehensive Nodal/Branch Circuit Analysis Including Fixator-Norator Pairs in Analog Circuits 125

Reza Hashemian (Northern Illinois University)

A generalized approach is proposed to solve for analog circuits, analysis and design. By directly introducing fixator-norator pairs (FNP) into the branch conductance matrix of a linear analog circuit we integrate analysis and design into one process. This approach is different from the traditional Modified Nodal Analysis (MNA) in two aspects. First, it includes FNPs as well as independent voltage sources into the nodal/branch solution. In fact, FNPs bring the design constraints right into the analysis making the two combined, and one single process. The second difference is that, here we choose a tree-branch approach rather than nodal one. This results in computational efficiency.

All-Pass Time Delay Circuit Magnitude Response Optimization using Fractional-Order Capacitor 129

Norbert Herencsar (Brno University of Technology), Aslihan Kartci (Brno University of Technology), Esteban Tlelo-Cuautle (National Institute of Astrophysics, Optics and Electronics / CINVESTAV), Bilgin Metin (Bogazici University), Oguzhan Cicekoglu (Bogazici University)

Paper presents the integer- and fractional-order cases of a voltage-mode all-pass time delay circuit, or more frequently called as all-pass filter, employing a single negative-type current-controlled current inverting transconductance amplifier and a floating capacitor. Utilization of a fractional-order capacitor (FoC) $C_{0.96}$ with $12 \text{ pFsec}^{-0.04}$ value for magnitude response optimization of the filter is investigated. FoC was emulated via 4th-order Valsa RC network and values optimized using modified least squares quadratic method. In frequency range 1 MHz - 1 GHz it shows only ± 0.5 degree phase angle deviation and the relative pseudo-capacitance error varies from -1.85 % to +0.73 %. SPICE simulations are given to prove the theory.

New Low-Voltage CMOS Differential Difference Amplifier (DDA) and an Application Example 133

Roman Sotner (Brno University of Technology), Norbert Herencsar (Brno University of Technology), Vilem Kledrowetz (Brno University of Technology), Aslihan Kartci (Brno University of Technology), Jan Jerabek (Brno University of Technology)

The paper presents a newly designed structure of a low-voltage differential difference amplifier (DDA). The novel implementation brings significant reduction of complexity in comparison to readily available operational amplifiers-based approach. It was designed in Cadence IC6 Spectre in $0.18 \mu\text{m}$ TSMC technology operating correctly with only $\pm 0.9 \text{ V}$ supply voltages and fabricated in EURO PRACTICE IC Service. Designed DDA features wide linearity and dynamics of output voltage together with operational bandwidth up to 100 MHz. Detailed simulation results and new voltage-mode second-order all-pass/notch filter are included to prove its superior behavior.

Low Power Low Noise Amplifier with DC Offset Correction at 1 V Supply Voltage for Ultrasound Imaging Systems 137

Longheng Luo (Fudan University), Yimin Wu (Fudan University), Jianguo Diao (Fudan University), Fan Ye (Fudan University), Junyan Ren (Fudan University)

Conventional low noise amplifier (LNA) used in ultrasound imaging systems consumes large power and die area for lower noise figure. It is not suitable for multichannel and portable ultrasound imaging applications. This paper presents a low power LNA with dc correction which restrains the low-frequency noise and dc drifting from transmit/receive switch. The core amplifier is composed of a source degenerated input stage and a class AB output stage using a translinear loop. Besides, a current feedback topology is used to reduce the noise figure by enhancing the input impedance of the LNA. The LNA is designed in 28 nm CMOS process. Simulation results show that the noise efficiency factor (NEF) of the proposed LNA is 3.57, and the LNA achieves 100 MHz bandwidth, 20 dB voltage gain with 2 mW power consumption at the supply voltage of 1 V, which is quite lower than prior works.

Gain-Boosted Complementary Dynamic Residue Amplifier for a 160 MS/s 61 dB SNDR Noise-Shaping SAR ADC	141
<i>Hanie Ghaedrahmati (Shanghai Jiao Tong University), Jianjun Zhou (Shanghai Jiaotong University), Lukang Shi (Oregon State University)</i>	

This paper proposes a power-efficient high-gain and high-speed single-stage complementary dynamic residue amplifier for using in noise-shaping successive-approximation-register (SAR) analog-to-digital converter (ADC). A complementary input pairs and a cross-coupled cascode topology are presented to increase the performance and boost the gain of dynamic residue amplifier. The proposed dynamic amplifier achieves the voltage gain of 16 at a 1 GS/s sampling frequency and 20.5 μ Vrms input noise. Total power consumption of the prototype residue amplifier is 45.8 μ W at 1.1 V supply voltage in 40 nm CMOS technology.

A Novel Time-Domain Phase Quantization Noise Extraction for a VCO-Based Quantizer	145
<i>Hamidreza Maghami (Oregon State University), Hossein Mirzaie (Oregon State University), Pedram Payandehnia (Oregon State University), Kartikeya Mayaram (Oregon State University), Ramin Zanbaghi (Cirrus Logic Inc. / University of Texas at Austin), Terri Fiez (University of Colorado Boulder)</i>	

A highly linear SAR-VCO MASH delta-sigma ADC architecture is presented. OTA based analog integrators are not needed whereby the ADC is mostly digital and process scaling friendly. A new technique is introduced to extract the quantization noise of the VCO-based quantizer as a PWM signal using digital circuitry. This technique is independent of the OSR and the input signal amplitude of the VCO-based quantizer making it attractive for higher bandwidth applications. The proposed technique is demonstrated with a 0-1-1 MASH delta-sigma architecture. Behavioral simulations show second order noise shaping with 75dB SNDR for an OSR of 20.

Single-Loop Delta-Sigma ADC using Noise-Coupled VCO Quantizer	149
<i>Mahmoud Sadollahi (Oregon State University), Lukang Shi (Oregon State University), Yanchao Wang (Oregon State University), Gabor C. Temes (Oregon State University)</i>	

A single-loop two-step 3rd order $\Delta\Sigma$ ADC with voltage-controlled-oscillator (VCO) quantizer employing noise coupling technique is presented. The noise-coupling technique improves the order of noise-shaping by one or more in VCO quantizer, and makes it power efficient. Third-order noise shaping has been achieved with only one active integrator, and the required output swing, gain and bandwidth requirements for the integrator are relaxed. The digital noise-canceling filter is simplified in the proposed architecture, and the specifications of the dynamic element matching are relaxed. Simulation results verify the effectiveness of the proposed structure.

A 13b-ENOB Noise Shaping SAR ADC with a Two-Capacitor DAC	153
<i>Lukang Shi (Oregon State University), Yi Zhang (Analog Devices / Oregon State University), Yanchao Wang (Oregon State University), Manjunath Kareppagoudr (Oregon State University), Mahmoud Sadollahi (Oregon State University), Gabor C. Temes (Oregon State University)</i>	

This paper presents an active noise-shaping successive-approximation-register analog-to-digital converter. Instead of binary-weighted capacitors, it uses two equal-valued capacitors as a digital-to-analog converter (DAC). Thus, the capacitance spread in the DAC is 1, much smaller than that of the conventional binary-weighted capacitor array, and hence the mismatch error can be greatly reduced. The circuit provides first-order noise shaping, which can improve the ADC's linearity even for a small oversampling ratio (OSR). Also, the proposed architecture uses a monotonic switching procedure which allows fewer conversion steps than for a conventional SAR ADCs.

Session A3L-A: Special Session on Computer Arithmetic in Honor of Drs. Graham Jullien and William Miller – Part I

Chair: Kenneth Jenkins, *Pennsylvania State University*

Time: Monday, August 6, 2018, 13:30 - 15:00

Location: Mercuri

Contributions of Graham Jullien and William Miller to Residue Number System Arithmetic Technology	157
<i>W. Kenneth Jenkins (Pennsylvania State University)</i>	

Dr. W. K. Jenkins' association with Dr. Graham Jullien and Dr. William Miller began in 1978 when they were working to develop Residue Number System (RNS) arithmetic techniques for digital signal processing. They began working on certain projects, one of which was the IEEE Press Book that they co-edited with two other colleagues in 1986. Dr. Jullien was a pioneer in the theory and development of Residue Number System (RNS) arithmetic for the emerging area of digital signal processing in the 1970's and 1980's. His interest in VLSI for RNS arithmetic steered him in the general direction of VLSI circuit design for special purpose digital signal processors.

Contributions of Graham Jullien and William Miller to Modified Quadratic Number System Arithmetic 161

Michael A. Soderstrand (University of California, Davis)

Quadratic Residue Number System (QRNS) arithmetic became very popular in the early 1980's for its ability to compute the multiplication of two complex numbers with only two real multiplies as compared to the four multiplies required in normal complex multiplication. This is particularly useful in the computation of Fast Fourier Transforms (FFT), Complex Numerical Transforms (CNT) and digital filters with complex coefficients. However, QRNS requires the RNS moduli to be prime numbers of the form $4k+1$ or composite numbers with prime factors of that form. This restriction eliminates some of the most desirable moduli for RNS number systems. In 1986, Graham Jullien and William Miller introduced what they called Modified Quadratic Number Systems (MQRNS) which allowed any set of valid RNS moduli to be used in an MQRNS system in which two complex numbers could be multiplied with three real multiplications: one more than QRNS, but one less than normal complex multiplication. This MQRNS system lent itself well to applications in FFT, CNT and digital filters with complex coefficients including complex heterodyne tunable filters.

Parallelism in Computer Arithmetic: A Historical Perspective 165

Behrooz Parhami (University of California, Santa Barbara)

Many early parallel processing breakthroughs emerged from the quest for faster and higher-throughput arithmetic operations. Additionally, the influence of arithmetic techniques on parallel computer performance can be seen in diverse areas such the bit-serial arithmetic units of early massively parallel SIMD computers, pipelining and pipeline-chaining in vector machines, design of floating-point standards to ensure the accuracy and portability of numerically-intensive programs, and prominence of GPUs in today's top-of-the-line supercomputers. This paper contains a few representative samples of the many interactions and cross-fertilizations between computer-arithmetic and parallel-algorithms communities by presenting historical perspectives, case studies of state of art and practice, and directions for further collaboration.

Exploring Parallelism in the Deep Learning Arena 170

Mohsin M. Jamali (University of Texas of the Permian Basin)

Deep learning is the re-incarnation of artificial neural networks. It is popular due to availability of high performance computing as it may have thousands of hidden layers in its neural network architecture. Big data consisting of large volume of information is also a driving factor for popularity of deep learning. Large volume of data need to be processed with deep neural networks requires training which may be in the order of days. Exploitation of parallel processing with available high performance computational platforms can reduce training time. This paper addresses various opportunities that can be exploited to reduce computation time.

Computing at the Atomic Scale with Quantum Dots Not Available at Time of Publication

Konrad Walus (University of British Columbia)

Today we are able to pattern circuits based on quantum dots with atomic precision, an example of that is the patterned silicon atomic dangling bonds pioneered by Wolkow et al. at the University of Alberta, which can be structured into custom arrays with atomic precision using scanning probe fabrication techniques and which demonstrate complex single electron behaviour. We are interested in modelling computing systems at the nano- and atomic- scale based on locally interacting few-electron devices, sometimes called quantum dot cellular automata (QCA). In order to understand these systems, we have developed a set of computer aided design tools and techniques which allow for numerical experimentation of complex circuits and systems using these emerging technologies.

Session A3L-B: CMOS Implementation of Analog Circuits

Chair: Vishal Saxena, *University of Idaho*

Co-Chair: Rashmi Jha, *University of Cincinnati*

Time: Monday, August 6, 2018, 13:30 - 15:00

Location: Martis

A100MS/s 9-Bit Companding SAR ADC with On-Chip Input Driver in 65nm CMOS for Multi-Carrier Communications 174

Anindya Saha (University of Minnesota), Saurabh Chaubey (University of Minnesota), Ramesh Harjani (University of Minnesota)

This paper presents a 100MS/s 9b companding SAR ADC which exploits the statistical properties of broadband multi-carrier signals to reduce the dynamic range requirement for the ADC. The architecture emulates the performance of a higher resolution ADC by reducing the PAPR of a multi-carrier signal to that of a single carrier. Additionally, gain-before-sampling results in reduced sampling capacitor size which lowers power and area. A prototype implemented in TSMC's 65nm GP CMOS process consumes 12.27 mW at 100 MS/s while extending the dynamic range of the sub-ADC by 13 dB, and resulting in a Schreier FOM of 150.7 dB.

Design of Multi-Layers DGS Resonator for Phase Noise Improvement of K-Band VCOs in 0.18 μm CMOS Technology 178

Islam Mansour (Kyushu University / Egypt-Japan University of Science and Technology / Benha University), Mohamed Aboualalaa (Kyushu University / Egypt-Japan University of Science and Technology), Nusrat Jahan (Kyushu University), Adel Barakat (Kyushu University), Ramesh K. Pokharel (Kyushu University), Ahmed Allam (Egypt-Japan University of Science and Technology), Adel B. Abdel-Rahman (Egypt-Japan University of Science and Technology), Mohammed Abo-Zahhad (Egypt-Japan University of Science and Technology)

A novel technique for a low phase noise and compact K-band Voltage-Controlled Oscillator using multi-layers DGS resonator is proposed. The DGS resonator realizes an additional series resonance at the higher side of parallel resonance frequency, and improved both the active and loaded quality factor of the resonator. The proposed resonator has active quality factor of 130 and a compact size of $0.009\text{mm}^2(0.000459\lambda^2)$. Using this DGS resonator in the VCO causes 9dB improvement in the phase noise compared the VCO implemented using the conventional LC resonator. Two VCOs are implemented in $0.18\mu\text{m}$ CMOS technology have FTR of 8.3 , 6.1%, phase noise of -113.2, -114dBc/Hz and FoM of -194.4 and -195.2dB, respectively.

OTRA based Log and Antilog Amplifiers 182

Rajeshwari Pandey (Delhi Technological University), Neeta Pandey (Delhi Technological University)

In this paper single Operational Transresistance Amplifier (OTRA) based log and antilog amplifiers are proposed. These structures make use of exponential dependence of current on voltage of an n-MOSFET operating in subthreshold region. The resistor connected to the input terminals of OTRA can also be implemented using n-MOSFETs operating in linear region resulting in a complete MOS realizable structure. Circuit techniques to get temperature independent output for both the amplifiers are presented. The amplifiers are also analyzed in the presence of non-idealities of the active blocks. The functionality of the proposed amplifiers is verified through SPICE simulations using $0.18\mu\text{m}$ technology parameters.

A Compact 65nm CMOS Sub-1-V All-MOSFET Voltage Reference with Low Average Temperature Coefficient of 13.9ppm/ $^{\circ}\text{C}$ 186

Kaijie Ma (Shenzhen University), Yuan Cao (Hohai University), Xiaojin Zhao (Shenzhen University)

In this paper, we present a novel CMOS sub-1-V voltage reference design without any resistor or bipolar junction transistor. By forming a closed feedback loop, the temperature stability of the proposed voltage reference is significantly enhanced. In addition, a dedicated operational amplifier is introduced to improve the power supply rejection ratio (PSRR) and line regulation (LR). Moreover, the proposed voltage reference, which is implemented by using a 65nm 1.2V standard CMOS process, features a compact silicon area of $609\mu\text{m}^2$. According to our 300 runs Monte Carlo simulation results, the average and minimum temperature coefficient (TC) from -40C to 100C is calculated to be 13.9ppm/C and 4.2ppm/C, respectively. The PSRR is reported to be 38dB and 61dB at DC and 10MHz, respectively. Meanwhile, the proposed implementation's operational power supply range is from 0.9V to 2.6V, with a calculated line regulation of 2.29%/V.

A Compact CMOS Memristor Emulator Circuit and its Applications 190

Vishal Saxena (University of Idaho)

Conceptual memristors have recently gathered wider interest due to their diverse application in non-von Neumann computing, machine learning, neuromorphic computing, and chaotic circuits. We introduce a compact CMOS circuit that emulates idealized memristor characteristics and can bridge the gap between concepts to chip-scale realization by transcending device challenges. The CMOS memristor circuit embodies a two-terminal variable resistor whose resistance is controlled by the voltage applied across its terminals. The memristor 'state' is held in a capacitor that controls the resistor value. This work presents the design and simulation of the memristor emulation circuit. Furthermore, the memristor emulator circuit can be designed and fabricated using standard commercial CMOS technologies and opens doors to interesting applications in neuromorphic and machine learning circuits.

Session A3L-C: Wireless Communications

Chair: Hassan Mostafa, *Cairo University*

Co-Chair: Ibrahim M. Elfadel, *Khalifa University, Abu Dhabi*

Time: Monday, August 6, 2018, 13:30 - 15:00

Location: Luna

LTE Handover Parameters Optimization using Q-Learning Technique 194

Assem Abdelmohsen (Cairo University), Mohamed Abdelwahab (Cairo University), Mohamed Adel (Cairo University / Institute of Aviation Engineering and Technology), M. Saeed Darweesh (Institute of Aviation Engineering and Technology / Zewail City of Science and Technology), Hassan Mostafa (Cairo University / Zewail City for Science and Technology)

Optimization of the LTE network is crucial to obtain the best performance. The handover margin (HOM) and time to trigger (TTT) should be chosen so that the system will have minimum number of handovers per user per second, minimum system delay, and maximum throughput. In this paper a new handover optimization algorithm for long term evolution (LTE) network based on Q-learning optimization is presented. The proposed algorithm operates by testing different values of HOM and TTT then observes the output performance corresponding to the values of these parameters, and it eventually selects the values that produce the best performance. The proposed handover optimization technique is evaluated and compared to previous work. Q-learning achieves minimum average number of handover per user and also has maximum throughput than the fuzzy logic optimization technique.

Multiplatform Spectrum Sensing Prototype 198

Danilo Corral-De-Witt (University of Windsor / University of Louisiana at Lafayette), Aarron Younan (University of Windsor), Dewan Ariful (University of Windsor), Lining Zhang (University of Windsor), Kemal Tepe (University of Windsor)

We propose a multiplatform spectrum sensing prototype, which is capable to sense the UHF TV frequency bands from 500 MHz to 698 MHz (Channels 19 to 51) and identify the characteristic features of the primary users. Combining a high accurate spectrum sensing device, an open source RF Explorer and an RTL SDR receptor we collected critical information of the TV spectrum and know its usability. Results obtained shows the availability of white and gray spaces in the Centre for Engineering Innovation of the University of Windsor.

A Compact UWB Antenna Design for Indoor Wireless Applications 202

Mohamed Shehata (Cairo University), Mohamed Sameh Said (Cairo University), Hassan Mostafa (Cairo University / Zewail City for Science and Technology)

Ultrawide band (UWB) signals are extremely power limited due to the severe power spectral density (PSD) constraints obligated by the Federal Communications Committee (FCC). Therefore, the design of radiation efficient antennas for UWB signalling is a challenging step in the design and development of UWB communication systems, especially when these signals co-exist with previously standardized narrowband (NB) wireless services. This work presents a compact microstrip-based UWB antenna design that is capable of suppressing narrowband interference (NBI) signals. The immunity of the proposed design to NBI is tested both experimentally and through simulations. Moreover, the experimentally measured spectral characteristics are employed in simulating the impact of the proposed UWB antenna on a typical UWB signalling waveform. Both experimental and simulation results confirm the capability of the proposed design to suppress NBI signals at six different frequencies, corresponding to the most frequently used wireless services at these frequencies, while introducing an almost negligible distortion to the UWB signalling waveforms.

Area Efficient 4Gb/s Clock Data Recovery using Improved Phase Interpolator with Error Monitor

Gyunam Jeon (Northeastern University), Yong-Bin Kim (Northeastern University)

The paper presents area efficient 4Gbps clock and data recovery (CDR) by using improved phase interpolator (PI) with error monitor. The proposed CDR architecture has only two sets of phase interpolator while the conventional CDR has eight sets of phase interpolators. Each set of the PI is comprised of eight inverters to get 11.25° phase interpolation from 0° to 348.75° by using the proposed phase error monitor. The outputs of the phase error monitor are composed of 9 bits sampled from early pulse. The monitor chooses four clock phases among 0° , 45° , 90° , 135° , 180° , 225° , 270° , and 315° from an analog voltage controlled oscillator (VCO) by sending 3 bits to the multiplexer. Then, the other 6 bits determine the interpolation phase of each block by using the inverter switches. V_{cp} (Charge Pump Output Voltage) is pre-charged to 345mV for fast locking time. The time for frequency locking and phase selection are 23.35ns with pre-charge time (1.1ns). The design is simulated with a 180nm CMOS technology node at 1.8V power supply. The total power consumption of the proposed CDR is 4.35mW.

Hierarchical Cluster-Based Cooperative Spectrum Sensing in Cognitive Radio Networks using Adaptive Threshold	210
<i>Abeer F. Alqawasmeh (University of Windsor), Farooq A. Awin (University of Windsor), Esam Abdel-Raheem (University of Windsor), Kemal Tepe (University of Windsor)</i>	

Energy detector (ED) is the most favorable detection approach for cognitive radio (CR) system. Selecting a proper detection threshold for ED is significant to satisfy the target CR's detection performance. This work proposes an adaptive threshold energy efficient multi-level hierarchical cluster-based cooperative spectrum sensing (MH-CBCSS) algorithm with low computational complexity. The proposed algorithm enables a CR to dynamically adapt its detection threshold to meet the target overall detection error rate. Moreover, an optimal detection threshold that minimizes the overall detection error rate is determined. Finally, the detection performance of the proposed algorithm is presented and evaluated through simulation results.

Session A3L-D: Image Processing I

Chair: Wasfy Mikhael, *University of Central Florida*

Co-Chair: Vasily Moshnyaga, *Fukuoka University, Japan*

Time: Monday, August 6, 2018, 13:30 - 15:00

Location: Saturni

A Wavelet Domain Implementation of Sparse Representation Method for Face Recognition	214
<i>Taif Alobaidi (University of Central Florida), Wasfy B. Mikhael (University of Central Florida)</i>	

Recently, a new discriminative sparse representation method for robust face recognition via l2 regularization (NDSRFR) was published. In this paper, a Wavelet domain (WDNDSRFR) is presented. In particular, the Two-Dimensional Discrete Wavelet Transform implementation is given and shown to considerably reduce the computational complexity and the storage requirements while maintaining the recognition accuracy of the NDSRFR. Extensive simulations were performed on five face databases, namely, ORL, YALE, FERET, Cropped AR, and Georgia Tech and the enhanced properties of the WDNDSRFR are confirmed as shown in the given sample results.

New Method for Medical Intake Detection by Kinect	218
<i>Sho Yamanaka (Fukuoka University), Vasily Moshnyaga (Fukuoka University)</i>	

This article describes a new technique for unobtrusive detection of medication intake in a non-wearable system equipped by Kinect. Unlike existing methods that rely on skeletal modeling, the proposed technique fuses the depth image data with the RGB image data, and makes decision based on both the spatial coordinates and the mouth features. Experiments show that such formulation significantly improves the accuracy of real-time medication intake recognition in comparison to existing methods.

Real-Time Algorithm for Simultaneous Vehicle Detection and Tracking in Aerial View Videos	222
<i>Ahmed Gomaa (Egypt-Japan University of Science and Technology), Moataz M. Abdelwahab (Egypt-Japan University of Science and Technology), Mohammed Abo-Zahhad (Egypt-Japan University of Science and Technology)</i>	

Automatic detection and tracking of multiple vehicles in airborne videos is still a challenging problem due to camera movement, vehicle occlusion and the need for computational resources. This paper presents a robust and efficient real-time method for automatic detection and tracking of vehicles in airborne videos. The detection process is based on a combination of Top-hat and Bot-hat transformation aided by the morphological operation. Background objects are removed through analyzing feature points motion of the obtained object regions using K-means clustering and KLT tracker. The obtained vehicles features are grouped and clustered into separate vehicles based on their motion properties. Finally, a connecting scheme is presented to determine the connectivity of vehicle cluster with the corresponding cluster in the vehicles trajectories. Experiments conducted on videos representing airborne cameras verify the excellent overall performance compared to other existing approaches.

Adaptive Feature Extraction Algorithm using Mixed Transforms for Facial Recognition	226
<i>Genevieve Sapijaszko (University of Central Florida), Taif Alobaidi (University of Central Florida), Wasfy B. Mikhael (University of Central Florida)</i>	

An essential first step in facial recognition is the extraction of unique and reliable features that can identify faces from images. Feature extraction algorithms have evolved in recent years, with Discrete Wavelet Transform (DWT) and Discrete Cosine Transform (DCT) in particular showing good results. This paper utilizes the DWT and the DCT in sequence and iteratively to best find the features that represent the facial image. The proposed facial recognition system will use the ORL, Yale and the Ferret-Fc databases to compare the proposed system to different published results as well as a simplified version of the proposed system. Each of the feature extraction matrix for each image will be compared using the \$ L1 \$ norm classifier, and the best recognition rate will be determined.

Session A4P-E: Analog Circuit Designs

Chair: Yehia Massoud, *Stevens Institute of Technology*

Co-Chair: Mona Zaghoul, *National Science Foundation*

Time: Monday, August 6, 2018, 13:30 - 15:00

Location: Poster Area

Portable and Low Power Efficient Pre-Fall Detection Methodology 230

Neeraj Rathi (Indiana University – Purdue University Indianapolis), Monika Kakani (Indiana University – Purdue University Indianapolis), Maher Rizkalla (Indiana University – Purdue University Indianapolis), Mohamed El-Sharkawy (Indiana University – Purdue University Indianapolis)

Fall in recent years have become a potential threat to elder generation. Looking at the problems faced by people and cost of treatment after falling, we have designed and developed a dependable and low power embedded system device with easy to wear capabilities and optimal sensor structure. The designed system is triggered on interrupts from motion sensor to monitor users balanced, and unbalanced states. Near 100% sensitivity, 96% accuracy, and 95% specificity for fall detection were measured. The system can detect Front, Back, Side and Stair fall with consumption of 100uA (650uA with BLE consumption) in deep sleep mode, 6.5mA in active mode with no fall, and 14.5mA, of which 8.5 mA is consumed via the BLE when fall is declared in active mode.

High-Speed ADC Quantization with Overlapping Metastability Zones 234

Jiajun Ren (University of Texas at Dallas), Jiu Xiong (University of Texas at Dallas), Jin Liu (University of Texas at Dallas)

This paper presents a new ADC quantization method. Instead of using digitally valid comparator outputs as the basis for quantization, the proposed approach uses comparator metastability zones as the basis for quantization. The required comparator regeneration time is significantly reduced to improve the ADC speed. Meanwhile, using overlapping metastability zones reduces the number of required reference levels to about half, leading to a lower ADC power consumption. Simulation results of a 2GS/s 6b flash ADC with the proposed quantization method in 0.13 μ m CMOS show 25%-50% improvement in ADC bandwidth, while using about half the power.

A Coupled Schmitt Trigger Oscillator Neural Network for Pattern Recognition Applications 238

Ting Zhang (University of Alabama at Birmingham), Mohammad R. Haider (University of Alabama at Birmingham), Iwan D. Alexander (University of Alabama at Birmingham), Yehia Massoud (Stevens Institute of Technology)

This paper demonstrates a coupled Schmitt trigger oscillator based ONN (SMT-ONN) for pattern recognition applications. Unlike previous ONN models, the SMT-ONN can be easily realized in both hardware and software levels. A mathematical model of the Schmitt Trigger Oscillator and the corresponding CMOS circuit are presented to validate the mathematical model. The SMT-ONN can realize the pattern recognition task by considering the convergence time and frequency as the recognition indicators. A Kuramoto model based frequency synchronization approach is utilized, and simulation results indicate less than 160 ms convergence time and close frequency match for a simplified pattern recognition application.

A High-Resolution Time-Based Resistance-to-Digital Converter with TDC and Counter 242

Shuya Nakagawa (Keio University), Kaito Horikoshi (Keio University), Hiroki Ishikuro (Keio University)

This paper presents a high resolution time-based resistance-to-digital converter for amp-less high-precision sensor application. In order to solve the trade-off between resolution and bandwidth, a time-to-digital converter (TDC) is combined with a resistance-controlled-oscillator. The TDC is used to measure the fractional part of oscillation period, which realize a high resolution and conversion rate with moderate oscillation frequency. Proposed fractional period estimation technique reduce the required number of TDC and save power consumption. A prototype system was developed and 23 ppm resolution of resistance change at conversion rate of 5kSps was experimentally demonstrated.

Continuous-Time Optimization using Sub-Threshold Current-Mode Growth Transform Circuits 246

Ahana Gangopadhyay (Washington University in St. Louis), Oindrila Chatterjee (Washington University in St. Louis), Shantanu Chakrabarty (Washington University in St. Louis)

Analog circuits have long been used for solving various mathematical optimization problems due to their lower latency when compared to their digital counterparts. This paper presents a novel continuous-time analog optimization circuit based on a growth transform-based fixed-point algorithm. The circuit uses translinear MOSFET circuits to implement the multiplication and normalization functions using only 5 transistors, where as continuous-time updates and recursion is implemented using current mirrors. The circuit does not require any additional components to enforce optimization constraints and naturally converges to a steady-state solution corresponding to a local minimum of an objective function. We show that the proposed circuit is generic enough to encompass a multitude of objective functions simply by changing the external circuitry and the power dissipation of circuit can be adjusted according to the desired latency. For this paper we present simulation results for specific forms of quadratic and linear cost functions with tunable coefficients, subject to a normalization constraint, and the results show excellent match to floating-point software simulation results.

Analysis of Package Impedance Effects on the Linearity of Source Series Terminated DACs 250

Helia Ordouei (Technical University of Berlin), Hossein Ghafarian (Technical University of Berlin), Friedel Gerfers (Technical University of Berlin)

This paper proposes a digital pre-distortion compensation technique canceling the package impedance effect on a 10-bit source series terminated (SST) digital-to-analog converter (DAC) implemented in 28nm CMOS with a 1.8V power supply. Given the data-dependent power supply current of a source series terminated DAC, any power supply and package impedance introduces non-linearity behavior fundamentally limiting the achievable SFDR. In order to be able to cancel this impact, first of all the package impedance as well as the power supply grid is analyzed and a parametric expression is derived for the oscillation frequency and damping of the power supply. Based on this model, a hardware-efficient pre-distortion cancellation technique using an 5-bit auxiliary DAC is proposed which improves the SNDR by 8 dB at low input frequencies and >4 dB at Nyquist frequency. In addition, a pure digital correction method is introduced and compared to the AUX-DAC solution.

Memristor Emulator Applications using the MOS-Only Technique 254

Bilgin Metin (Bogazici University), Norbert Herencsar (Brno University of Technology), Oguzhan Cicekoglu (Bogazici University)

The aim of this paper is to present a work towards a MOS transistor memristor emulator. The starting circuit employs an opamp, negative capacitors and loaded with a nonlinear resistor. The final aim is to design a memristor with only MOS transistors which is easily integrable. To implement the negative capacitance several possible potential circuit examples of MOS-Only type are given. These capacitors realize floating negative capacitances and the ac small signal form is shown. Some simulation results are included to verify theory.

Review and Analysis of Instrumentation Amplifier for IoT Applications 258

Tsz Ngai Lin (Hamad Bin Khalifa University), Bo Wang (Hamad Bin Khalifa University), Amine Bermak (Hamad Bin Khalifa University)

Instrumentation amplifier (IA) is the core circuit for precision sensor readout. With the development of Internet of Things (IoT) that requires a vast of sensing nodes, IA, that directly links the sensor device and other circuits will be more important during the sensing node design. This paper reviews the major IA topologies and techniques proposed in the last two decades. In IoT applications, all the on-chip circuit blocks should be low-cost (no trimming) and energy-efficient, which is a challenge for most IA design and is the focus of this review. In this paper, trade-offs between gain precision, energy consumption, noise, etc. are discussed in detail. Moreover, the IA startup process, which is not considered in most IA design is also discussed in this paper.

On-Chip Impedance Evaluation with Auto-Calibration based on Auto-Balancing Bridge 262

Takaaki Shirakawa (University of Kitakyushu), Ryosuke Sakai (University of Kitakyushu), Shigetoshi Nakatake (University of Kitakyushu)

We propose a circuit mechanism with an auto-calibration in the impedance measurement circuit based on the auto-balancing bridge method. In the auto-balancing bridge method, an inverting amplifier circuit using an operational amplifier is used. Since the measurement accuracy depends on the feedback resistance of the inverting amplifier circuit, it is necessary to replace the feedback resistor each time as checking the measured value of the resistance of the DUT (device-under-test) so as to match the value. In this work, by employing a current type D/A converter as a feedback resistor, we design a circuit with calibration of the resistance value and attain highly accurate measurement by simulation.

3 dB Bandwidth Enhancement using Miller Attenuation Technique 270

Shivam Agarwal (Indian Institute of Technology Ropar), Kumar Harsh (Indian Institute of Technology Ropar), Vinayak Hande (Indian Institute of Technology Ropar)

In this paper, we propose a novel approach to increase the -3 dB Bandwidth of a two stage operational amplifier (opamp) by adding a Voltage Attenuator (VA) in the compensation path. This technique reduces the Miller Effect by a factor K, which improves the -3 dB point by the same factor. Here, K is equal to the gain of the attenuator. Results indicate that the proposed technique achieves -3 dB Bandwidth improvement of 38.6 times over the Miller Compensation technique and 20 times over the state-of-the-art FFVF Compensation technique.

An N-Shaped I-V Characteristic Circuit with a Mem-Impedance Feature 270

Todd Wey (Lafayette College)

A circuit built from readily available integrated circuits is shown to have a nonlinear first quadrant current-voltage characteristic with a negative differential resistance region similar to the tunnel diode. With a slight modification, it is shown that a memory impedance feature can be added that has interesting dynamic consequences. The circuit shows great potential in the study of negative resistance oscillators and chaotic circuits.

A Dual-Path Open-Loop CMOS Slew-Rate Controlled Output Driver with Low PVT Variation 274

Xiaoyan Gui (Xi'an Jiaotong University), Kai Li (Xi'an Jiaotong University), Xiaoli Wang (Xi'an Jiaotong University), Li Geng (Xi'an Jiaotong University)

A dual-path open-loop slew-rate controlled CMOS driver is presented. The proposed output driver incorporates a delay-locked loop (DLL) to minimize the slew-rate variation over process, voltage and temperature (PVT). A dual-path open-loop structure is introduced to cancel the high-frequency components of the output signal. Simulation using the Global Foundry 0.18um CMOS process shows that the driver achieves less than 0.6V/ns slew-rate variation operating at 500 Mbps over 16 corners, corresponding to 26% reduction compared with that of a conventional output driver.

A Cascode Switching Technique for Highly Efficient Stacked Class E PA 278

Ahmed Zamzam (Analog Devices)

In this paper, technology fundamental limits on the performance of double stacked class E power amplifiers are studied, and the drawbacks of the conventional topology are highlighted. A novel cascode switching technique is proposed in order to mitigate the loss caused by these drawbacks. The theory is carried to design a power amplifier (PA) at 15 GHz using 0.13u CMOS technology. A comparison is performed with a classic double stacked design. Simulation results show enhancement in both output power and power added efficiency by about 9% and 10.6% respectively.

Design of a Low-Supply Sensitivity LC VCO with Complementary Varactors 282

Bingjun Tang (Xi'an Jiaotong University), Xiaoyan Gui (Xi'an Jiaotong University), Li Geng (Xi'an Jiaotong University)

Analysis of the effect of supply-induced frequency variation on the LC VCO is described. According to the results of the analysis, the first-order impact on the supply sensitivity is that the varactor's effective capacitance varies with the supply voltage. A novel compensation technique based on complementary varactors to reduce the supply sensitivity of the LC VCO is proposed with no extra power dissipation, nor phase noise degradation. Simulation results show that this compensation technique reduces the periodic jitter by more than 93%.

A Digital PLL based 2nd-Order $\Delta\Sigma$ Bandpass Time-Interleaved ADC 286

Sanjeev Tannirkulam Chandrasekaran (University at Buffalo), Arindam Sanyal (University at Buffalo)

This paper presents a time-interleaved (TI) VCO-based band-pass ADC with a second-order bandstop noise transfer function. The proposed ADC uses a digital phase-locked-loop (PLL) based architecture and employs current starved ring-oscillator as integrator which provides inherent multi-bit quantization. Thus, the proposed band-pass ADC does not need op-amps for integration and consumes low power and area. The proposed ADC is designed in 65nm CMOS and Matlab and Spectre simulations were performed to characterize the ADC. The proposed ADC achieves 61dB SNDR while consuming 0.44mW and has a Walden FoM of 63fJ/conv. step.

A Hybrid $\Delta\Sigma$ /Nyquist Rate Switched Capacitor Power Amplifier in 65nm CMOS 290

Qiuyan Xu (Washington State University), Subhanshu Gupta (Washington State University), Ali Azam (University of Utah), Zhidong Bai (University of Utah), Jeffrey S. Walling (University of Utah)

This paper presents a new hybrid-mode SCPA that segments a traditional SCPA into two segments. An LSB C-2C sub-array is modulated using a $\Delta\Sigma$ modulator (DSM) connected in parallel with a Nyquist-rate unary MSB array. This technique enables a hybrid SCPA (H-SCPA) that can achieve a higher bandwidth than a traditional DSM DAC, while achieving a higher resolution than a traditional Nyquist DAC. A prototype design is implemented in 65nm CMOS and post-extracted simulation results validate the performance of the H-SCPA. The H-SCPA achieves a peak output power of 23.5 dBm and a peak system efficiency of 48% at an operating frequency of 2.8 GHz. When amplifying a 20 MHz, 64 QAM, OFDM signal, the average output power and system efficiency at 2.8 GHz are 17.4 dBm and 24.9 %, respectively, while achieving an EVM of 1.9 %-rms and meeting the spectral mask requirements.

Random Number Generation from Unbounded Chaos Synthesized by a Practical Phase-Locked Loop 294

Emre Ulusoy (TÜBİTAK), Salih Ergün (TÜBİTAK)

This study exhibits a design of a random number generator (RNG) circuit, which uses no additional component to a simple phase-locked loop (PLL) device. The designed circuit has been benchmarked with both chaotic signal observations and statistical randomness tests provided by NIST without any post-processing step. The fabricated circuit contains no additional entropy source to generate random bit sequences. Needed randomness is acquired by PLL's itself in form of white noise shape. Required white noise is measured demonstrating flat power spectrum over 1.505MHz central oscillation frequency. Compared to previous works, it is first of its kind while it has no additional source of randomness.

A High Resolution MCML-Based Time-to-Digital Converter Implementation

Tianshuo Zhao (Carleton University), Leonard MacEachern (Carleton University)

A new high-resolution time-to-digital converter (TDC) architecture based on MOS-Current-Mode-Logic (MCML) is described. Aiming at high resolution and large dynamic range, the prototype is implemented with 0.13 um CMOS technology. A time domain resolution of 10.6 ps and a respectively large dynamic range of 100 ns was achieved.

A CMOS Perimeter Gated SPAD based Mini-Digital Silicon Photomultiplier 302

Mst Shamim Ara Shawkat (University of Tennessee), Nicole McFarlane (University of Tennessee)

In this paper, a CMOS perimeter gated single photon avalanche diode (PGSPAD) based mini-digital silicon multiplier (SiPM) is presented. A PGSPAD's additional terminal tunes the dark count, efficiency, and measurement range of the device. Spatial and temporal data compression schemes, reduce the total readout electronics and improve fill factor (FF). For a more compact, low power implementation, a single analog counter provides temporal integration of PGSPAD avalanche events. An event generator realizes the digital asynchronous address event representation readout at the top level of the detector. The SiPM is implemented in standard 0.5 μm CMOS process and simulation results show temporal compression and dead time improvement by 10 and 25%. The designed PGSPAD mini-digital SiPM is suitable as the pixel of PGSPAD digital SiPM for nuclear imaging applications.

Ultra Low-Energy Active Charge Restoration DAC for SAR Analog-to-Digital Converter

Japesh Vohra (Indian Institute of Technology Ropar), Vinayak Hande (Indian Institute of Technology Ropar)

A novel architecture for Digital-to-Analog converter (DAC) used in successive approximation register Analog-to-Digital converters (SAR ADCs) is proposed. It reduces the energy consumption as well as required on-chip capacitor area. A single unit capacitor section using charge from a previously charged capacitor is added to the circuit in series after every comparison and any charge lost is partially restored. Using a single capacitor and charge sharing method reduces the energy consumption for capacitor switching, capacitor area and total capacitance to a small fraction of the conventional SAR ADC.

Robust Continuous-Time MASH Delta Sigma Modulator 310

Yanchao Wang (Oregon State University), Lukang Shi (Oregon State University), Tao He (Oregon State University), Yi Zhang (Oregon State University), Chia-Hung Chen (Oregon State University), Gabor C. Temes (Oregon State University)

A continuous time (CT) multi-stage noise-shaping (MASH) delta sigma modulator (DSM) with reduced noise leakage is proposed. In this structure, there is no matching requirement between the digital noise cancellation filter (DNCF) and the analog noise transfer function (NTF) of the DSM. Therefore, the circuit is insensitive to element variations, and no complex digital calibration is needed. The residual shaped quantization noise leakage caused by integrator non-idealities can easily be calibrated to relax the design requirements of the integrators. The proposed MASH can use more aggressive NTF than traditional MASH, using a simpler noise cancellation filter and calibration. Simulation results and theoretical analysis verify the effectiveness of this structure.

Session A5L-A: Special Session on Computer Arithmetic in Honor of Drs. Graham Jullien and William Miller – Part II

Chair: Earl Swartzlander, *University of Texas at Austin*

Time: Monday, August 6, 2018, 15:30 - 17:00

Location: Mercuri

Memristor Adder Design 314

Nagaraja Revanna (University of Texas at Austin), Earl E. Swartzlander Jr. (University of Texas at Austin)

In this paper, the design of adders implemented with memristors is discussed. Memristor based designs for standard adder architectures (ripple carry adder, carry look-ahead adder and parallel prefix adders) are explained. The area and latency are compared. Surprisingly, the Radix-2 CLA has a complexity very similar to the parallel prefix adders. It is shown that the Kogge-Stone design has the best metric in terms of delay and area among the parallel prefix adders.

A Hardware Obfuscation Technique for Manufacturing a Secure 3D IC 318

Siroos Madani (University of Louisiana at Lafayette), Mohammad R. Madani (University of Louisiana at Lafayette), Indira Kalyan Dutta (University of Louisiana at Lafayette), Yamini Joshi (University of Louisiana at Lafayette), Magdy Bayoumi (University of Louisiana at Lafayette)

3D Integrated Circuit (3D-IC) is an emerging technology that can address many challenging problems threatening the security of the chip by split manufacturing \cite{split}. One of the disadvantages of split manufacturing is the uncertainty in the reliability of the last foundry that is responsible for the complete bonding of tiers. In this work, we present an innovative approach that safeguard the outsourcing of the entire 3D IC manufacturing including the last bonding stage. The proposed technique not only obfuscates the design functionality but immunizes the IC against Trojan insertion.

Review of Arithmetic Operations using the Continuous Valued Number System	324
<i>Babak Zamanlooy (University of Windsor), Mitra Mirhassani (University of Windsor), Majid Ahmadi (University of Windsor)</i>	

In this paper, various arithmetic operations that are based on the Continuous Valued Number System (CVNS) are reviewed. The number system has been employed in implementing a series of mixed-signal, feed-forward neural networks. The CVNS digits, named analog digits in their original form do not have a grid and share and overlap information of the original number with each other. This chain-like relation between the digits allows for detection and correction of the digits if some values get distorted by the implementation medium. The information overlap is adjustable and is based on the power and area requirements of the circuit. Higher overlap requires more area and consequently consumes more power. In this paper, additions, multiplication, and storage structures are reviewed, and a new structure for addition is proposed.

Autonomous Multi-Robot Platoon Monitoring	328
<i>Ratheesh Ravindran (University of Detroit Mercy), J. Patrick Mills (General Motors), Mohan Krishnan (University of Detroit Mercy)</i>	

Ensuring the safety of soldiers on foot in a platoon formation is an important goal for the military. Accomplishing this with the use of protective encirclement of autonomous robots is an important application of human-machine collaboration. A key task for the robots in this regard is automatic optimal positioning with respect to a shifting platoon perimeter created by the motion of soldiers. This work formulates and evaluates an algorithm for optimal positioning of protective robots as soldiers in the platoon moves for their task. Convex hull with GPS information, helps to determine evolving positioning goals and paths for protective robots.

Session A5L-B: Oscillators and Modulators

Chair: Igor Filanovsky, *University of Alberta*
Co-Chair: Ebrahim Ghafar-Zadeh, *York University*
Time: Monday, August 6, 2018, 15:30 - 17:00
Location: Martis

Sub-THz Tunable Push-Push Oscillators with FinFETs for Wireless NoCs	332
<i>Yunus Kelestemur (Ohio University), Soumyasanta Laha (Ohio University), Savas Kaya (Ohio University), Avinash Kodi (Ohio University), Hao Xin (University of Arizona), Ahmed Louri (George Washington University)</i>	

The characteristics of an ultra-compact tunable push-push oscillator using FinFET technology are presented. The use of an independent-gate FinFET bestows the oscillator with a simple and efficient tunable performance up to 250GHz. Tuning range of 7GHz originates from the higher gate-source capacitance of the FinFET replacing the external capacitor, thus reducing parasitics. The phase noise of the oscillator varies from -82 to -76 dBc/Hz at 1 MHz offset between 0 V and 1 V back gate bias. The compact and tunable characteristics of the proposed sub-THz oscillator make it suitable for applications such as on-chip wireless interconnects required for kilo-core computing.

A Balanced Hybrid Ring Oscillator for Precise Temperature Compensation	336
<i>Kanglin Xiao (Peking University Shenzhen Graduate School), Bo Wang (Peking University Shenzhen Graduate School), Xiaoqi Lin (Peking University Shenzhen Graduate School), Changpei Qiu (Peking University Shenzhen Graduate School)</i>	

A balanced hybrid ring oscillator (RO) is proposed for the precise temperature compensation. The proposed RO consists of both the delay cells with PTAT characteristics and those with CTAT characteristics. The optimal temperature compensated point can be found by adjusting the number of PTAT and CTAT delay cells and the load capacitance of each delay cell. Both ideal and non-ideal models are developed to explain this temperature compensation mechanism. Finally, combining the opposite temperature characteristics of normal RO and current-starved RO, a 13.4 MHz on-chip clock circuit is implemented with 14.6 ppm/°C over the temperature range from -40°C to 80°C.

Analysis and Design of 60-GHz Switched Injection-Locked Oscillator with up to 38 dB Regenerative Gain and 3.1 GHz Switching Rate	340
<i>Ali Ferchichi (Technische Universität Dresden), Hatem Ghaleb (Technische Universität Dresden), Corrado Carta (Technische Universität Dresden), Frank Ellinger (Technische Universität Dresden)</i>	

This paper presents the design of a 60-GHz switched injection-locked oscillator (SILO). Furthermore, an analysis of the phase-sampling concept in SILO is performed, in order to be able to recognize phase-locked oscillations in the frequency domain. The SILO design is based on a cross-coupled oscillator topology to provide the positive feedback needed for creating the regenerative gain. The SILO has been fabricated in a 130-nm SiGe BiCMOS process. The pulsed oscillator consumes a dc power of 107 mW and sustains a maximum switching rate of 3.1 GHz, i.e. a relative switching rate of 5.17%, which is the highest reported. The SILO delivers a free-running output power of 7.3 dBm and reaches a maximum regenerative gain of 38 dB.

Incremental Delta Sigma Modulation with Dynamic Weighted Integration 344

William Guicquero (Université Grenoble Alpes, CEA-Leti), Arnaud Verdant (Université Grenoble Alpes, CEA-Leti), Dominique Morche (Université Grenoble Alpes, CEA-Leti)

This paper presents a technique to reduce the required number of cycles to reach a given quantization resolution of conversion performed by incremental Delta Sigma ADCs. Thanks to a specifically designed dynamic weighting of the modulator's coefficients combined with a dedicated digital filter, the OverSampling Ratio (i.e. OSR) can be reduced compared to conventional structures thanks to a more efficient quantization noise shaping. This dynamic weighted integration (DWI) technique is first motivated in the context of a first order modulator supported with a mathematical proof. In the second part, the proposed technique is extended to the specific case of a complex fourth order modulator with four different examples of topology regarding the position of the dynamic weighting.

Design and Modeling of Silicon Photonic Ring-Based Linearized RF-to-Optical Modulator 348

Md Jubayer Shawon (University of Idaho), Rui Wang (University of Idaho), Vishal Saxena (University of Idaho)

In this article, a Ring-Assisted-Mach-Zehnder Interferometer (RAMZI) based RF-to-Optical Modulator with excellent spurious-free-dynamic-range (SFDR) performance has been presented. The performance of this silicon-based RAMZI device has been analyzed and verified with a commercial Photonic Circuit simulation tool. A compact Verilog-A model of RAMZI is also developed for hybrid CMOS circuit in Cadence environment. An SFDR of 129.97 dB/Hz^(2/3) has been obtained for this type of modulator.

Session A5L-C: Image Processing II

Chair: M. Omair Ahmad, *Concordia University, Montreal, Canada*

Time: Monday, August 6, 2018, 15:30 - 17:00

Location: Luna

Content-Based Image Retrieval using Perceptual Image Hashing and Hopfield Neural Network 352

F. Sabahi (Concordia University), M. Omair Ahmad (Concordia University), M.N.S. Swamy (Concordia University)

Unlike the regular cryptographic usage, hashing methods can be used to extract signatures in relation to the similar images detection. However, finding a hashing function for detecting image similarity seems to be a challenging task, as the hash code needs to represent the content rather than encrypt it. In this paper, a novel content-based image retrieval method using image hashing is proposed that generated a signature per image based on image rotation and DCT. The acquired hash code is used to train a memory model to find similar images. We evaluate our method by comparing it with some state-of-the-art methods.

Fire Detection using Computer Vision 356

Taha Zaman (NED University of Engineering and Technology), Muhammad Hasan (NED University of Engineering and Technology), Saneeha Ahmed (NED University of Engineering and Technology), Shumaila Ashfaq (NED University of Engineering and Technology)

This paper provides a computer vision based technique for automatically detecting and classifying fire by processing the video data generated by an ordinary camera. While there are a copious amount of publications in fire detection with images, distinguishing hazardous fire from non-hazardous is a problem that is still unsolved. The proposed technique uses the color and fluctuation characteristics of fire to detect it. Initially, the algorithm locates regions of the video where there is motion; from these regions fire colored pixels are extracted and then wavelet transform is applied to confirm that the moving object is fire. The proposed technique tracks the rate of increment of fire region to distinguish between hazardous and controlled fire. Experimental results demonstrate that the proposed technique is effective in detecting the fire and classifying it as hazardous or controlled flame. The performance of the technique was observed in terms of true positive rate which was observed to be 85.57% while the average delay in detection of hazardous fire was 66.2 frames at a frame rate of 10 frames per second or 6.62 seconds.

A Novel Curb Detection Method for Advanced Driver Assistance Systems 360

Melvin P. Manuel (University of Detroit Mercy), Karthika Balan (University of Detroit Mercy), Mohannad Murad (University of Detroit Mercy), Mohan Krishnan (University of Detroit Mercy)

Curb detection is an important research topic in environment perception, which is an essential part of Autonomous Land Vehicles (ALV) and Unmanned Ground Vehicle (UGV) operations. Also, curb detection is specifically a component in Advanced Driver Assistance Systems (ADAS) that are assisting drivers in parking their cars without hitting the concrete curbs/parking blocks. In this paper, a novel curb detection algorithm is developed by using Canny edge detection along with Hough transform.

A Low-Cost Slice Interleaving DSC Decoder Architecture for Real-Time 8K Video Decoding 364

Shifu Wu (University of California, Davis), Bevan Baas (University of California, Davis)

Demands for high resolutions such as 4K and 8K and high frame rate have been increasing. However, the throughput requirements for real-time decoding is challenging. To achieve the required throughput, video decoders of H.264 and HEVC have high hardware cost due to the computation complexity and memory requirement. In this paper, a low-cost slice interleaving architecture of Display Stream Compression (DSC) video decoder is proposed. Three designs are implemented based on the proposed architecture. The design that supports 4 slices per line for 16 bits per component 8K video has a gate count of 282K and main memory of 54.7KB. The design is synthesized in ST FD-SOI 28nm standard cell library and reported a maximum achievable frequency of 1.04GHz, which is able to decode 8K UHD (7680×4320) video up to 94 frames per second in real-time.

Reduction of Circuit Scale for General Maximally Flat FIR Digital Filters 368

*Takashi Yoshida (Tokyo Metropolitan College of Industrial Technology),
Naoyuki Aikawa (Tokyo University of Science)*

Recently, Wang et al. proposed a general structure for maximally flat FIR digital filters, which can dynamically adjust frequency response only by changing derivative constraints. However, Wang’s structure requires large circuit scale to realize the variable structure. To reduce the circuit scale, the present paper proposes a novel general structure for such filters that can also dynamically adjust frequency response. The proposed structure can realize exactly the same frequency response as Wang’s structure with fewer multipliers, adders, and delays. Furthermore, the proposed structure can realize more types of frequency response than Wang’s structure.

Session A5L-D: Control I

Chair: Roozbeh Razavi-Far, *University of Windsor*

Co-Chair: Maher Azzouz Abdekkhalek, *University of Windsor*

Time: Monday, August 6, 2018, 15:30 - 17:00

Location: Saturni

Optimal Control Design of Large Scale Systems with Uncertainty 372

*Shahah Almutairi (Wichita State University), V. Thenmozhi (Wichita State University),
John Watkins (Wichita State University), M. Edwin Sawan (Wichita State University)*

Model order reduction techniques are used to design optimal control strategies with low sensitivity to model uncertainty. Different sources of uncertainties are investigated. Performance sensitivity is reduced by adding a sensitivity measure to the performance index that represents the cost. This results in a larger matrix which will be double the size of the original system. Thus, developing reduced order model will alleviate this problem. Then the design is completed based on the reduced order model and the same is used to obtain an appropriate design of the full order system.

Development of a Multi-Stage Control Strategy for Omnidirectional Mobility in the Presence of Slip 376

Jinghan Fu (University of Detroit Mercy), Richard C. Hill (University of Detroit Mercy)

This paper develops and evaluates in simulation a novel ground mobility concept that employs three independent pods which can be attached to an arbitrary object for movement and positioning. The bulk of this paper is focused on the development of a multi-stage, force-based control strategy for “driving” the target object with attached pods such that good performance is achieved even in the presence of significant wheel slip, that is, in low-friction environments. The overall mobility concept is demonstrated in simulation with the ultimate conclusion being that the proposed concept appears to be feasible and should be pursued further.

A Distributed Fault Detection and Isolation Method for Multifunctional Spoiler System 380

*Mojtaba Kordestani (University of Windsor), M. Foad Samadi (University of Windsor),
Mehrdad Saif (University of Windsor)*

The increasing complexity of aircraft subsystems and control structure invoke new fault diagnosis methodologies for these vehicles. Multifunctional spoiler (MFS) is an essential part of an aircraft spoiler control system that can be easily deteriorated due to faults which could consequently compromise the safety of the aircraft. The MFS consists of several components with highly nonlinear dynamics. This paper presents a new fault detection and isolation (FDI) system using dynamic neural networks (DNN) to deal with incipient faults at their early stages. For this purpose, an intelligent distributed FDI framework consisting of three DNNs is employed for generating residual set in the system to observe any discrepancy in the states of the system. Furthermore, the dynamic structure of the designed neural networks helps the observers tackle the non-linearity of the system and provides the fault isolation in the whole operating range. Simulation results are conducted to demonstrate the ability and effectiveness of the proposed FDI system.

Motor Speed Control Signals for Multirotor Flights in the Presence of Complete Propeller Motor Failures 384

Hideaki Okazaki (Shonan Institute of Technology), Siyuan Yin (Shonan Institute of Technology), Kaito Isogai (Shonan Institute of Technology), Hideo Nakano (Shonan Institute of Technology)

In the presence of complete propeller motor failures, motor speed control signals for multirotor flights are discussed. First the mathematical description for a multirotor as a rigid body is introduced. Secondly definitions for multirotor operating points, (or flight states), are summarized. Thirdly in the presence of complete motor failures, definitions of multirotor remaining motor speed control signal vector, and especially theorem of directly providing motor speed control signals for quadrotor flights are provided. Finally the theorem is applied to the problem of a quadrotor vehicle experiencing motor failures. The simulation results are also illustrated.

Modeling and Flight Control Simulation of Multirotors 388

Kaito Isogai (Shonan Institute of Technology), Hideo Nakano (Shonan Institute of Technology), Hideaki Okazaki (Shonan Institute of Technology)

A theorem for flight controls of multirotors is discussed. First the mathematical foundation for describing the motion of a multirotor as a rigid body is summarized. Secondly definitions and theorems for multirotor operating points, (or flight states), and flight controls are summarized. Thirdly a theorem of the motor speeds to realize the desired multirotor flight states including constant altitudes and hovering flights, is provided. Finally by using some implementations of the theorem on Maple symbolic computations, MATLAB matrix calculations, and MATLAB numerical simulations with ODE solvers, the examples of flight control simulations for a quadrotor are presented.

Tuesday, August 7, 2018

Session B1L-A: Analog to Digital Converters

Chair: Igor Filanovsky, *University of Alberta*

Co-Chair: Mitra Mirhasani, *University of Windsor*

Time: Tuesday, August 7, 2018, 8:30 - 10:00

Location: Mercuri

A 12-Bit ENOB 8MHz BW Noise-Shaping SAR ADC using High-Speed Switches 392

Zhiyuan Dai (Fudan University), Hang Hu (Fudan University), Yongzhen Chen (Fudan University), Fan Ye (Fudan University), Junyan Ren (Fudan University)

Successive approximation register Analog-to-digital converter (SAR ADC) with a passive noise-shaping modulator is an appropriate choice to increase the ENOB and save power consumption compared with conventional SAR ADC. This paper proposed a third-order noise-shaping SAR ADC with high speed switches in modulators to complete the charge sharing for reducing the time cost of noise shaping process in one sampling cycle and used a foreground calibration to calibrate the value of the capacitors in DAC array. The whole ADC can realize 12.11-Bit ENOB in 8MHz bandwidth (BW).

The HotSpot Compensation in High Speed Data Converters

Satyajit Mohapatra (Indian Institute of Technology Gandhinagar), Nihar Ranjan Mohapatra (Indian Institute of Technology Gandhinagar)

With 3D integration of ICs, the thermal hot spots are no longer limited to digital chips. Sensitive analog arrays in high performance data converters are prone to vertical temperature gradients and hotspots of adjacent dies. Though various techniques exist to compensate for systematic errors, none of them address issues related to local hotspot. In this work, we have proposed a technique to compensate hotspot induced errors over the array. An array extension algorithm is also provided to make the technique applicable for higher resolution converters. The performance of proposed array in presence of hotspots is verified on the model of a 16-bit 10-Msps pipelined ADC with 3.5 bit/stage using Matlab. The proposed technique improves the effective resolution of converter by ~1.25 bits (corresponding SNDR improvement is ~8db) with respect to the existing techniques. It also provides additional advantages of gradient compensation, parasitic matched routing and is tolerant to edge effects. Strategies to develop such arrays is discussed in details.

A MDAC Common-Mode Shifting Technique enabling Power Consumption Reduction in Pipeline ADCs 400

Nima Lotfi (Technical University of Berlin), Marcel Runge (Technical University of Berlin), Friedel Gerfers (Technical University of Berlin / NiederRhein Technologies)

This paper presents a common-mode shifting 1.5-bit/stage pipeline architecture, that enables both high dynamic range and a reduced power consumption at the same time considering nm CMOS technologies. The design approach enables a maximum differential output signal swing of 1.8 V ppp by proper common-mode and reference voltage selection. This common-mode shifting approach enables 40 % power savings within the reference buffer using the 1.2V core supply instead of the 2V analog power supply. The total power consumption drawn from both supplies is only 125mW, resulting in an excellent FOM of 161 dB.

Compact Time-Mode SAR ADC with Capacitor Flipping Bit-Cycling Operation 404

S. Zaniar Hoseini (University of Akron), Kye-Shin Lee (University of Akron)

This work describes an area efficient time-mode SAR ADC with capacitor flipping bit-cycling operation. The proposed SAR ADC can be realized with a single-capacitor and a single-current source where the capacitor flipping scheme eliminates multiple current sources used for the capacitor charging and discharging operation. Furthermore, the charge sharing error caused by parasitic capacitance is reduced by pre-charging the parasitic capacitor before the capacitor flipping operation. As a result, the SAR ADC can be implemented with extremely small area and low power consumption due to the reduced number of circuit components. An 8-bit 364.9kS/s time-mode SAR ADC is designed with CMOS 0.18 μ m technology where the ADC operation and performance are verified through circuit level simulations.

A Consideration on LUT Linearization of Stochastic ADC in Sub-Ranging Architecture 408

Parit Kanjanavirojkul (University of Tokyo), Nguyen Ngoc Mai-Khanh (University of Tokyo), Ikeno Rimon (University of Tokyo), Takahiro J. Yamaguchi (University of Tokyo), Tetsuya Iizuka (University of Tokyo), Kunihiro Asada (University of Tokyo)

A stochastic ADC is naturally a non-uniform nonlinear quantizer, in which post-correction is typically needed. In addition, even though it can achieve high precision, the range of a stochastic ADC is limited. Therefore, it is beneficial to use the stochastic array as a fine-stage in a sub-ranging architecture. In this work, look-up-table linearization with full mapping and sigma-based mapping for a stochastic ADC and sub-ranging stochastic ADC are examined and compared experimentally by Monte Carlo simulation and measurement. A test chip is fabricated for 4-bit coarse flash stage and 127 comparator arrays on 0.18 μ m CMOS. Measurements confirmed simulation results, and it is shown that full mapping can improve equivalent number of bit by 2 bits compared to sigma-based mapping. Furthermore, the results suggest that the coarse stage comparator with 5 times better input offset variation than fine stage comparator is suitable for sub-ranging implementation.

Session B1L-B: VLSI Digital Integrated Circuits I

Chair: Masud Chowdhury, *University of Missouri at Kansas City*

Co-Chair: Hassan Mostafa, *Cairo University*

Time: Tuesday, August 7, 2018, 8:30 - 10:00

Location: Martis

A Disturb Free Read Port 8T SRAM Bitcell Circuit Design with Virtual Ground Scheme 412

Mahmood Uddin Mohammed (University of Missouri-Kansas City), Nahid M. Hossain (University of Missouri-Kansas City), Masud H. Chowdhury (University of Missouri-Kansas City)

This paper presents new 8T SRAM design that avoids the stability and reliability issues of the conventional 6T and other existing SRAM cells. The proposed 8T SRAM is as good as the 10T design without the overheads of the 10T cell. In the proposed design, virtual ground technique weakens the positive feedback and improves the write ability of the cell. Precharging circuit is not required for read operation, which reduce the area overheads of the SRAM memory system. The design isolates the storage node from the read path, which improves the read stability. For reliability study, we have investigated the static noise margin (SNM) of the proposed 8T SRAM and compared with the conventional designs at different process corners. The delay of the proposed bitcell is reduced to 69.67% during write and 52.87% during read compared to conventional 6T bitcell. In addition to this, leakage currents of the proposed 8T bitcell reduced to 4.24%, 9.5% and 18.65% in hold, read and write operations in contrast to conventional 6T bitcell. We have also analyzed the impact of the process and parametric variations in the proposed 8T SRAM using Monte Carlo simulations.

New Reverse Converters for the Four-Moduli Set $\{2^n, (2^n)-1, (2^n)+1, (2^{(N-1)})-1\}$ for N Even

Phalgun P.S. (Manipal Academy of Higher Education), Dattaguru V. Kamat (Manipal Academy of Higher Education), Ananda Mohan P.V. (Centre for Development of Advanced Computing)

In this paper, two reverse converters for the four-moduli set $\{2^n, (2^n)-1, (2^n)+1, (2^{(n-1)})-1\}$ are described. One of these is based on Mixed Radix Conversion (MRC). Another converter is based on two-stage MRC in which two pairs of moduli are considered and intermediate results are obtained using MRC. A second stage uses MRC to obtain the final decoded number from these intermediate results. Both the converters are compared with previously reported converter for this moduli set regarding hardware resources and conversion time. Synthesis results on FPGA and ASIC are also presented.

Full Adder Circuit Design using Lateral Gate-All-Around (LGAA) FETs based on BSIM-CMG Model 420

Muyu Yang (Illinois Institute of Technology), Erdal Oruklu (Illinois Institute of Technology)

The Gate-All-Around (GAA) FET device structure is expected to become the next widely used evolution of FET architecture in the near future. In this paper, full-adder datapath circuits using Lateral GAA FETs (LGAA FETs) based on BSIMCMG model are analyzed. Full adder designs include minimum count (10 transistor) adders such as 13A adder, the SERF adder, the CLRCL adder as well as the standard mirror adder and Ultra-Low-Power Full Adder (ULPFA). To better characterize the operation of LGAA FETs, their performance is compared against multi-gate FinFETs, such as double-gate FinFETs, triplegate FinFETs and quadruple-gate FinFETs.

Modified CONNECT: New Bufferless Router for NoC-Based FPGAs 424
Marwa Shaheen (Cairo University), Hossam Fahmy (Cairo University), Hassan Mostafa (Cairo University) / Zewail City for Science and Technology

As Chip Multiprocessors (CMPs) scale to tens or hundreds of nodes, the interconnect becomes a significant factor in cost, energy consumption and performance. Energy efficiency of the underlying communication framework plays a major role in the performance of multi-core systems. Recent work proposes buffer-less deflection routing as a cost effective alternative. A modified version of CONfigurable NETwork Creation Tool (CONNECT) is proposed as a buffer-less router to be lightweight and efficient. Modified CONNECT is based on parallel port allocation mechanism within the routers, that allows maximum number of flits to be deflected in a productive direction. Modified CONNECT is evaluated using uniform, transpose and inverse traffic workloads against CONNECT, BLESS and CheapInterconnect Partially Permuting Router (CHIPPER) on a 4x4 mesh network. Modified CONNECT saves 30% area compared to CONNECT while employing lower performance. Modified CONNECT also saves 24% in area against BLESS keeping the same performance.

A Low-Complexity Hardware AWGN Channel Emulator on FPGA using Central Limit Theorem
Arathy B. Nair (Indian Institute of Science), Arijit Mondal (Indian Institute of Science), Shayan Srinivasa Garani (Indian Institute of Science)

We present a flexible, low-complexity additive white Gaussian noise (AWGN) channel emulator. The proposed generator employs multiple improved Tausworthe generators to generate uniform random numbers, which are then summed up and manipulated based on the central limit theorem to generate Gaussian random numbers. We simulated the hardware design with 12 and 48 Tausworthe random number generators (RNGs) with different seed sets. The proposed design provides one sample per clock useful towards high speed channel emulation.

Session B1L-C: Energy Harvesting

Chair: Mohamad Sawan, *Polytechnic Montreal*

Co-Chair: Po-Hung Chen, *National Chiao Tung University, Taiwan*

Time: Tuesday, August 7, 2018, 8:30 - 10:00

Location: Luna

A 1.65 to 2.5 GHz Wide-Band RF Energy Harvester 432
Eslam Helal (Ain Shams University), Mohamed El-Nozahi (Ain Shams University), Sameh Ibrahim (Ain Shams University), Hani Fikry Ragai (Ain Shams University)

This paper presents an automatic-frequency-tuning RF energy harvester. The proposed self-startup system tracks the frequency of maximum input power automatically within its wide frequency range of operation from 1.65 GHz to 2.5 GHz. The system is mainly composed of two rectifying paths and a frequency tuning control loop. Implemented in a 130-nm CMOS technology, simulation results show power conversion efficiency (PCE) of the main path rectifier of 62% at 10-k Ω load resistance. The input power sensitivity of the main path is -18 dBm for output voltage of 0.5 V and a load resistance of 100 k Ω .

A 5.2 GHz RF Energy Harvester System using Reconfigurable Parallel Rectenna 436
Hamed Abbasizadeh (Sungkyunkwan University), Sang Yun Kim (Sungkyunkwan University), Truong Thi Kim Nga (Sungkyunkwan University), Danial Khan (Sungkyunkwan University), Seong Jin Oh (Sungkyunkwan University), Sung Jin Kim (Sungkyunkwan University), Kwan Tae Kim (Sungkyunkwan University), Dong In Kim (Sungkyunkwan University), Kang Yoon Lee (Sungkyunkwan University)

This paper presents a 5.2 GHz band, 67 % efficiency at the input power of +20 dBm RF Energy Harvester (EH) for IoT/wearable devices. In order to keep the high efficiency over the wide RF input range, the reconfigurable 6-parallel rectenna is proposed. The configuration of rectenna is automatically changed depending on the RF input power level. Also, adaptive matching is proposed to adjust the matching network automatically depending on the number of stages of rectenna, RF input frequency, and load current. Each RF-DC converter in rectenna is implemented by two Schottky diodes in a package and with a harmonic control scheme to produce a reasonable output DC voltage. Buck-boost converter is integrated to provide a constant voltage to the IoT/wearable devices. By using reconfigurable structure, different values of efficiency and the output DC voltage can be achieved. The measured efficiency of RF EH is 67 % with an output DC voltage of 6.1 V when the RF input power level is +20 dBm at the frequency of 5.2 GHz single-tone signal. It can charge the wearable devices such as G Watch, Mi band, and SmartThinQ.

A 13.56MHz Wireless Power Transfer System with Dual-Output Regulated Active Rectifier for Implantable Medical Devices	440
<i>Fu-Bin Yang (National Chiao Tung University), Jonathan Fuh (National Chiao Tung University), Po-Hung Chen (National Chiao Tung University)</i>	

In this paper, a 13.56 MHz wireless power transfer system with dual-output regulated active rectifier is developed for implantable medical devices. The rectifier employs pulse-skip modulation (PSM) to regulate two output voltages without using power consuming low dropout regulators (LDOs). The proposed automatic digital offset compensation (ADOC) adjusts both turn-on timing and turn-off timing to compensate the turn-on and turn-off delays of the comparator. The simulation results show that the proposed active rectifier achieves 94% efficiency. The entire wireless power transmission system including power amplifier, resonant tanks, and rectifier, has 67.2% maximum power conversion efficiency (PCE). Compared to the conventional approach with ideal LDOs, 19.2% efficiency improvement is obtained.

Efficient Dual-Band Ultra-Low-Power RF Energy Harvesting Front-End for Wearable Devices	444
<i>Seyed Mohammad Noghabaei (Polytechnique Montréal), Rafael L. Radin (Polytechnique Montréal), Mohamad Sawan (Polytechnique Montréal)</i>	

A new dual-band ultra-low-power RF-EH front-end, designed in standard IBM 130 nm CMOS technology has been presented. An efficient power summation is introduced to combine the available input power from two different frequencies 915 MHz and 1.85 GHz. The post-layout results show a high sensitivity of -33 dBm for 1 V at a capacitive load. The proposed harvester with new power summation scheme achieves maximum PCE of 43.2 % at -18 dBm (assuming two frequency bands are available). As a significant advantage, the proposed dual-band RF-EH design increases system availability performing harvesting from two different frequencies.

Optimizing the Inductance Time-Constant Ratio of Polygonal Integrated Inductors	448
<i>Ahmed H. Shaltout (University of Guelph), Stefano Gregori (University of Guelph)</i>	

This paper optimizes the inductance time-constant ratio of integrated inductors in order to improve the energy conversion efficiency of fully-integrated power converters. An inductance model is proposed and all the self and mutual partial inductances between segments are calculated. Multiple inductors were designed and simulated in TSMC 65-nm technology to validate the analytical model and the simulation results show a good agreement with the analysis.

Session B1L-D: Control II

Chair: Maher Azzouz Abdekkhalek, *University of Windsor*
Co-Chair: Mohan Krishnan, *The University of Detroit Mercy*
Time: Tuesday, August 7, 2018, 8:30 - 10:00
Location: Saturni

Person Following Robotic Suitcase	452
<i>Daryl Peralta (University of the Philippines Diliman), Manuel Ramos Jr. (University of the Philippines Diliman), Nicolette Ann Arriola (University of the Philippines Diliman)</i>	

The project aims to build a robotic suitcase capable of vision-based person following using a single camera. A mechanical drive system was designed and attached to a normal suitcase to allow autonomous movement. Person following algorithm was implemented by tracking the person's shirt based on the color and using PID controller on the centroid position of the red region for heading control and its bounding rectangle contour height for distance control.

A Bottom-Up, Top-Down Approach to Formal Control Synthesis for Multi-Agent Systems	456
<i>Juliana Vilela (University of Detroit Mercy), Richard Hill (University of Detroit Mercy)</i>	

This paper develops an approach for synthesizing the cooperative control of multiple agents. Typically, the design of the control for this type of system requires a high level of complexity and is based on heuristics. To avoid the use of heuristics, formal supervisory control theory is applied to generate control logic that is correct-by-construction. This paper combines the bottom-up approach of [1] with a novel top-down refinement step to further reduce the complexity of the control synthesis process. The method of this paper is validated using the example of [1] and is shown to provide significant further reduction in computation time.

Multi-Sensor Attitude and Heading Reference System using Genetically Optimized Kalman Filter	460
<i>Meron Gessesse (Carleton University), Mohamed M. Atia (Carleton University)</i>	

This paper proposes a systematic method of EKF parameters optimization using a hybrid statistical and genetic algorithms (GA) approach. The proposed approach has been tested on real data collected by an inertial measurement unit (IMU). Results showed that convergence of Q and R values can be obtained within few GA iterations leading to a robust and accurate EKF design. The results confirmed that the method can be applied successfully to real-world environment.

Collaborative Attacks on Autonomous Vehicle Platooning 464
Soodeh Dadras (Utah State University), Sara Dadras (Utah State University), Chris Winstead (Utah State University)

In this paper, we show that multiple, maliciously controlled vehicles can destabilize a vehicular platoon, to catastrophic effect, through local modifications to the longitudinal control law. We propose a systematic method that illustrates how multiple attackers can change their control configuration in tandem with each other in order to create a successful attack. We determine the range of gains based on the changes the other attacker initiated that allow an attacker to violate the stability criteria at different positions in the platoon. Finally, we demonstrate the impact of the designed collaborative attack on the vehicular platoon through an example.

Session B2P-E: Circuits and Systems I

Chair: Hassan Mostafa, *Cairo University*

Co-Chair: Sherif Michael, *Naval Postgraduate School*

Time: Tuesday, August 7, 2018, 8:30 - 10:00

Location: Poster Area

Bio-Impedance Measurements with Phase Extraction using the Kramers-Kronig Transform: Application to Strawberry Aging 468

A.A. Al-Ali (University of Calgary), A.S. Elwakil (University of Sharjah), B.J. Maundy (University of Calgary)

Fruit quality control is receiving increasing attention as an important application of bio-impedance measurements, which is a non-invasive technique. However, to effectively monitor fruit samples in the market, cheap and portable bio-impedance analyzers are needed while maintaining the accuracy of measurements over a wide frequency range. In this work, we report on the results obtained from a portable bio-impedance measuring device that relies on a modified Kramers-Kronig transform for calculating the phase from the measured impedance magnitude. This means that no actual hardware phase measurement takes place. The aging effect of strawberries is shown to be detected clearly via the change in impedance.

A Flexible Simulation and Design Environment for IMU/GNSS Sensors Integration 472

Soroush Sheikhpour (Carleton University), Mohamed M. Atia (Carleton University), Steven Waslander (University of Waterloo)

Due to the complexity of stochastic random errors of inertial measurements units (IMU) and Global Navigation Satellite Systems (GNSS), the design of IMU/GNSS fusion filters is challenging. Conventional approaches collect IMU/GNSS data and tune filter parameters against a ground-truth trajectory. However, this process does not verify the ability of the integration filter to correctly estimate hidden errors of sensors. Another challenge is the design of different dynamic models and error models for different moving platforms. To test a dynamic model, linearization and approximation of the dynamic model are commonly performed manually. This conventional design method is not flexible and prone to errors. To address these design challenges, this paper introduces a flexible simulation and design environment for IMU/GNSS integration. A MATLAB implementation of the environment is given. While the current implementation of the environment is handling IMU/GNSS integration for vehicular dynamic models, other dynamic models and additional sensors can be easily integrated in the environment.

A Predictive Model for Force-Sensing Resistor Nonlinearity for Pressure Measurement in a Wearable Wireless Sensor Patch 476

Shanshan Xie (Worcester Polytechnic Institute), Devdip Sen (Worcester Polytechnic Institute), John McNeill (Worcester Polytechnic Institute), Yitzhak Mendelson (Worcester Polytechnic Institute), Raymond Dunn (University of Massachusetts Medical School), Kelli Hickie (University of Massachusetts Medical School)

Implementation of a Pressure Ulcer Prevention System would prevent pressure ulcers, ease workload on caregivers, enabling patient treatment and monitoring outside a hospital setting, and reduce health care costs. Accurate measurement of pressure is an important criteria in order to achieve the above said goals. A challenge associated with using Force-Sensing Resistors (FSRs) as a pressure sensor is the part-to-part variability of up to +/-25%. This paper presents a novel modeling technique for correcting force sensor nonidealities, without requirement of prior knowledge of material parameters, and enabling measurement accuracies of +/-2% over a pressure range of 1N to 5N.

Energy Efficient ApproxSIFT Implementation for Image Mosaic with Approximate Computing Technologies	480
<i>Zheyu Liu (Tsinghua University), Erxiang Ren (Beijing Jiaotong University), Yanming Zhang (Beijing Jiaotong University), Fei Qiao (Tsinghua University), Qi Wei (Tsinghua University), Li Luo (Beijing Jiaotong University), Huazhong Yang (Tsinghua University)</i>	

Image mosaic could generate wide-angle images by stitching regional images with their overlapped portions, which is widely used technology in image signal processing. During the procedure, SIFT-feature based approaches are proven to perform best in such methods. However, traditional implementations of SIFT algorithm would consume the most of the processing time and energy. By balancing the processing quality and the design specifications of such applications of image mosaic, approximate computing hardware implementations have been adopted in this work to improve the energy-efficiency with ignorable quality degradations. Moreover, the approximate adders of LOA have been used to replace the exact adder to carry out the Gaussian convolution process of the algorithms, which further boost the SIFT operation performance, so-called ApproxSIFT. Simulation results of logic level show that, compared with the traditional method of exact computing, the ApproxSIFT hardware implementation with approximate adders significantly improve the image mosaic system, which achieves 2.4X and 3.5X in speed and power consumption, respectively.

A Novel Defuzzification Method for Type-II Fuzzy Set	484
<i>Farnaz Sabahi (Urmia University), Fahimeh Rookhosh (ISART Digital), Farzad Sabahi (Concordia University)</i>	

The foundation of most defuzzification approaches for Type-II fuzzy set are based on iterative algorithms. Although these approaches have been reported to be successful, many real-time applications still suffer from being computationally expensive. This issue seems more critical when general type-II fuzzy sets (GT2FS) are used. In this paper, we use two remarkable concepts in fuzzy set, i.e., alpha-plane and alpha-cut to propose a novel method for computing the centroid defuzzification of a GT2FS. As results show, the proposed method has a low computation load, while showing the comparable or superior outcomes in comparison with other leading competitive approaches.

Design, Synthesis and Application of a Novel Approximate Adder	488
<i>Tian Ban (Nanjing University of Science and Technology), Baokun Wang (Nanjing University of Science and Technology), Lirida Naviner (Télécom ParisTech)</i>	

Approximate computing is a new design paradigm in VLSI design and test. It can improve the performance of error-tolerant applications at the expense of slight loss in computational accuracy. In this paper, we propose a novel approximate adder with a hybrid structure (HYB-adder) which produces results of different precision. The proposed adder is synthesized by utilizing 28nm FD-SOI (fully-depleted silicon-on-insulator) technology. The proposed HYB-adder outperforms existing approximate adder designs regarding mean error distance with comparable area, delay and power consumption. The efficiency is also validated by its application in DCT/IDCT procedures.

An Approximate Multiplier based Hardware Implementation of the Izhikevich Model	492
<i>Salma Hassan (Cairo University), Khaled N. Salama (King Abdullah University of Science and Technology), Hassan Mostafa (Cairo University / Zewail City for Science and Technology)</i>	

This paper proposes the use of approximate multipliers in the hardware implementation of Izhikevich spiking neuron model. The accuracy of the model is investigated by calculating various types of errors on a single neuron and this analysis shows that the proposed model follows the original model. It also shows that the proposed model reproduces the same firing patterns as the original model. The network behavior is also studied and proved that the model has the same activity patterns of the original one. Moreover, the proposed neuron exhibits better accuracy than the piecewise linear approximation of the Izhikevich model.

Design of Approximate Dividers for Error Tolerant Applications	496
<i>Manikantta Reddy K. (National Institute of Technology Goa), Vasantha M.H. (National Institute of Technology Goa), Nithin Kumar Y.B. (National Institute of Technology Goa), Devesh Dwivedi (National Institute of Technology Goa)</i>	

This paper explores architectural designs of approximate unsigned integer dividers based on restoring and non-restoring algorithms. As the subtractor cell is the basic building of a divider, three designs of approximate subtractors are proposed. These approximate subtractors when used in divider reduce the complexity, power consumption and speed up the division operation at the cost of lower accuracy. The efficiency of proposed dividers are evaluated by simulating the circuits in 45-nm CMOS technology. The results indicate that the third design of approximate non-restoring and restoring dividers are consuming only 31% and 33% delay and power respectively as compared to conventional design. The accuracy of proposed designs is analyzed with several error metrics. The approximate restoring dividers are performing superior to non-restoring dividers both in-terms of design parameters and error metrics.

Low Power Approximate Multipliers with Truncated Carry Propagation for LSBs 500

Praveen Yadav (National Institute of Technology Goa), Anirudha Pandey (National Institute of Technology Goa), Manikantta Reddy K. (National Institute of Technology Goa), Ravi Prasad K.J. (National Institute of Technology Goa), Vasantha M.H. (National Institute of Technology Goa), Nitin Kumar Y.B. (National Institute of Technology Goa)

This paper proposes 8×8 bit multiplier architecture which focuses only on the carry generated from first 8 More Significant Bits (MSBs) of the final output. This proposed architecture design is divided into two blocks, one of which maintains the accuracy of the design and another block significantly reduces area, power and delay. Three approximate full adders are presented and placed in a specific manner to increase the performance of proposed multiplier architecture. Four multipliers using the proposed architecture are simulated in standard CMOS 180 / 65 nm technology node. Maximum delay in the proposed multiplier is 1.04 / 0.42 ns in 180 / 65 nm technology with a total power dissipation of 454.50 / 41.86 μ W respectively. The worst case Power-Delay-Product (PDP) of the proposed multiplier is 422.68 / 15.07 fJ which is 65.5 / 74.7 % less as compared to the conventional (Dadda multiplier) design. In the proposed designs 41.7 % less number of transistors are used while in the worst case scenario the normalized error in the output of the proposed designs is 0.0257.

ASIC Oriented Comparative Analysis of Biologically Inspired Neuron Models 504

Ahmed J. Abd El-Maksoud (Cairo University), Youssef O. Elmasry (Cairo University), Khaled N. Salama (King Abdullah University of Science and Technology), Hassan Mostafa (Cairo University / Zewail City for Science and Technology)

This paper introduces the hardware and the ASIC implementations of the four most popular biologically inspired neuron models. The models are quartic, Izhikevich, Hindmarsh Rose and Fitzhugh-Nagumo. Moreover, some approximate computing techniques are applied on these models to reduce the area and power consumption. In addition, ASIC implementations of these models and their approximate versions are carried out. Also, spiking behavior error between these models and the Hodgkin Huxley model, the reference accurate model, is presented. Finally, a fair comparative analysis is discussed to help the Spiking Neural Networks designers to select the best neuron model hardware implementation from the power, area and accuracy perspectives.

1-Transistor-1-Memristor Multilevel Memory Cell

Rishabh Govli (Indian Institute of Technology Kharagpur), Vivek Dixit (Indian Institute of Technology Kharagpur), Bibhu Datta Sahoo (Indian Institute of Technology Kharagpur)

CMOS-hybrids with memristors is an upcoming memory technology with advantages like high-density, non-volatility, and low power consumption. Memory density can be increased by realizing memory cells that can store more than 2 levels, i.e., multiple bits per cell. Realizing a multi-level memory cell using only one memristor falls into the category of analog application and hence, requires gradual resistance tuning (GRT). This paper proposes GRT based one-transistor-one-memristor (1T1M) multi-level memory cell. Designed and simulated in UMC 180nm technology with memristor modeled using VTEAM [7], an 8 Kbits memory is realized as a 64 × 64 memory array using the proposed 1T1M-memory cell (2-bits/cell). The proposed architecture has the advantages of zero-static power dissipation, low transient power consumption during read and write, and non-destructive read operations. The proposed 1T1M-memory cell can be extended to store more than 2-bits with high-accuracy sense amplifiers.

Error Analysis and Reliability Metrics for Software in Safety Critical Systems 512

Jonathan Lockhart (University of Cincinnati), Carla Purdy (University of Cincinnati), Philip A. Wilsey (University of Cincinnati)

As critical embedded systems become more complex, design and implementation becomes time consuming and costly. Simultaneously, physical limits to increase hardware performance lead to increased reliance on software. Formal methods, which are effective for hardware verification, are not yet mature enough to support comprehensive software testing, so traditional methods such as “test to exhaustion” are still heavily used. The goal of our work is to improve software testing for critical embedded systems, decreasing the testing time and strengthening software reliability. Here we demonstrate our process on one of a set of benchmark components we have defined. Our results can be used to compare our method with competing software testing methods.

Hardware Implementation of the Dual-Channel Spectral Subtraction Method for Lung Sounds Denoising 516

Mohammed Bahoura (Université du Québec à Rimouski), Hassan Ezzaidi (Université du Québec à Chicoutimi)

In this paper, a hardware architecture of dual-channel spectral subtraction method has been proposed for real-time lung sounds enhancement. The proposed architecture has been implemented on field programmable gate array (FPGA) chip using a high-level programming tool. Dual-channel spectral subtraction technique allows a dynamic estimate of the noise spectrum for an adaptive and robust lung sounds enhancement. The denoising performances of the proposed hardware architecture are compared to those obtained by MATLAB simulation, using subjective and objective evaluation tests. Resource utilization, maximum operating frequency, and total power consumption are presented for a low-cost Artix-7 FPGA chip.

Automatic Crop Furrow Detection for Precision Agriculture

Manpreet Kaur (University of St. Thomas), Cheol-Hong Min (University of St. Thomas)

The development in the robotics equipped with machine vision sensors applied to Precision agriculture is a demanding solution for various applications in the agriculture. This paper proposes an automatic furrow detection system based on identifying crop furrows from different growth stages of maize plants in the presence of weeds. The proposed image processing method consists of four different processes. First, image segmentation based on HSV (Hue, Saturation, Value) decision tree which discriminates crops, weeds, sky, and soil. Then, the noises in the images are eliminated by selecting pixel values. Further, mathematical morphological processes, that is, erosion to remove smaller objects followed by dilation to enlarge the boundaries of regions of foreground pixels are applied. To detect the position of furrows, ROI was defined by creating a binary mask. The Hough Transform and blob analysis were applied to detect crop furrows. The experimental results show that the method is effective.

An Open-Source Test-Bench for Autonomous Ultrasound Imaging 524

Alex Roman (Case Western Reserve University), Parisa Dehghanzadeh (Case Western Reserve University), Vida Pashaei (Case Western Reserve University), Abhishek Basak (Case Western Reserve University), Swarup Bhunia (Case Western Reserve University), Soumyajit Mandal (Case Western Reserve University)

Due to the need for development of customized transmission, reception, and processing algorithms, low-cost programmable ultrasound imaging devices are desirable for a variety of research applications. This paper describes a programmable 64-channel system-on-chip (SoC)-based test bench for research on autonomous wearable and implantable medical ultrasound imaging. The setup consists of a custom transmitter, a custom high-voltage (HV) multiplexer, an off-the-shelf receiver, and embedded software on the SoC. This results in a modular design that can be easily updated with improved hardware and software for different applications. This paper describes the system design and initial imaging results on tissue phantoms.

Utilizing Inherent Randomness in Stochastic Computing 528

Xiaojia Wang (Clemson University), Yingjie Lao (Clemson University)

Nowadays, low-cost and efficient integrated circuit (IC) design is of great interest due to the proliferation of computing devices, the resource-constrained nature of these systems, the desire to improve computing capability, and the need to reduce the cost. Stochastic computing has emerged as a promising alternative computing paradigm to binary deterministic computing, which enables very low-cost implementations of arithmetic operations using standard logic elements while achieving a higher degree of fault-resistance. However, it exhibits inherent randomness owing to its stochastic representation of data, which degrades the accuracy of the computation. Instead of trying to eliminate the inherent randomness to improve accuracy, this paper introduces the idea of utilizing the inherent randomness to enhance the performance of stochastic computing applications. We show that the inherent noise in stochastic computing can be utilized to perturb neural networks to escape local optima or saddle points, reduce over-fitting, and augment data. For example, the proposed methodology could improve the test accuracy of a multi-layer convolutional neural network on the CIFAR-10 dataset by 5%.

An Error Analysis Model for Floating-Point DFT Algorithms 532

Violeta Reyes-Rodríguez (University of Puerto Rico at Mayagüez), Manuel Jiménez (University of Puerto Rico at Mayagüez), Domingo Rodríguez (University of Puerto Rico at Mayagüez)

This paper presents a study of accuracy and hardware performance of floating-point (FP) implementations of the Discrete Fourier transform (DFT) and its fast algorithms. The studied formulations include Cooley-Tukey's and Pease's. Approximation and statistical methods were used to assess the accuracy of the FP treatments, while quantifying their normwise relative error. A hardware performance analysis was carried via FPGA synthesis, allowing for quantifying resource consumption and latency of each treatment. The results of the study showed significant differences in accuracy in the different treatments and to interesting accuracy-space-speed trade-offs when transform sizes were scaled.

Session B2P-F: Live Demos and M.Sc./PhD Forum

Time: Tuesday, August 7, 2018, 8:30 - 10:00

Location: Poster Area

Antenna Design for Magnetic Energy Transmission to Low Frequency RFID Tags in Small Aquaculture Tanks 536

Judith Santana Abril (University of Las Palmas de Gran Canaria), Graciela Santana Sosa (University of Las Palmas de Gran Canaria), Juan A. Montiel-Nelson (University of Las Palmas de Gran Canaria)

This work is focused in the antenna design of a RFID reader operating at low frequency. The RFID system is for transmitting magnetic energy between a tag located on a free-swimming fish in an aquaculture tank and a base station located outside the tank. It operates at the frequency of 134.2 kHz. In particular, the ad-hoc antenna design and the transmission stage of the proposed system is optimized for maximum distance and energy transmission efficiency.

Power Division in Multi-Receiver Wireless Power Transfer Systems 538

Graciela Santana Sosa (University of Las Palmas de Gran Canaria), Judith Santana Abril (University of Las Palmas de Gran Canaria), Juan Antonio Montiel-Nelson (University of Las Palmas de Gran Canaria)

The Wireless Power Transfer (WPT) is an increasingly important research topic which has been widely studied in the past few years. Achieving high efficiency in the WPT links is of critical importance and has been the main research topic of several previously published studies. We propose two methods to design adaptation networks based on quarter-wavelength transmission lines or impedance inverters. These adapt the load impedances of the receivers in a multi-receiver system so that a fair power division between all the participants takes place.

A High Speed Dynamic StrongARM Latch Comparator 540

Mohammed Al-Qadasi (King Abdullah University of Science and Technology), Abdullah Alshehri (King Abdullah University of Science and Technology), Abdullah S. Almansouri (King Abdullah University of Science and Technology), Talal Al-Attar (King Abdullah University of Science and Technology), Hossein Fariborzi (King Abdullah University of Science and Technology)

A new scheme for a high speed, low power StrongARM latch comparator has been proposed and simulated in 65nm CMOS technology. The baseline of the proposed idea is turning on the differential transistors during the evaluation phase and turning them off in the reset phase. This way, the amplification gain will be enhanced in the evaluation phase, resulting in a faster separation of the output signals. An improvement of 18% and 16% in the latching speed have been achieved over the conventional StrongARM latch and an improved version of the StrongARM latch in the literature.

Secure Network-on-Chip Architectures for MPSoC: Overview and Challenges 542

Luka Daoud (Boise State University)

Network-on-Chip (NOC) is the heart of data communication between processing cores in any Multiprocessor-based Systems on Chip (MPSoC). Packets transmitted on the NoC are exposed to snooping, which makes NoC-based systems vulnerable to security attacks. Additionally, Hardware Trojans (HTs) can be deployed in some of the NoC nodes to apply security threats of extracting sensitive information or degrading system performance. In this paper, an overview security attacks in NoC-based systems and the countermeasure techniques giving prominence on malicious nodes are discussed. We also present work in progress for secure routing algorithms.

Experimental Verification of a Fractional-Order Wien Oscillator Built using Solid-State Capacitors 544

Aslihan Kartci (Brno University of Technology), Agamyrat Agambayev (King Abdullah University of Science and Technology), Ali H. Hassan (Cairo University), Hakan Bagci (King Abdullah University of Science and Technology), Khaled N. Salama (King Abdullah University of Science and Technology)

A new type of fractional-order capacitors (FOCs) is fabricated using a molybdenum disulfide (MoS₂)-ferroelectric polymer composite. The phase angle of this FOC's impedance remains constant between 100 Hz and 10MHz with only a small deviation of ± 4 degrees. The performance of the fabricated FOCs is further tested using the well-known Wien oscillator. The main motivation of this paper is to demonstrate the use of a broadband, and tunable FOC in a real world application.

A Floating Point Data Compression using Inter-Extrapolative Predictor 546

Shinya Imai (University of Fukui), Shinji Fukuma (University of Fukui), Shin-Ichiro Mori (University of Fukui)

In recent years, along with advances in processor technology, large-scale numerical simulation dealing with huge floating point data is an active research field. In the case of supercomputing using many processors via the network, the bottleneck is communication speed rather than the calculation one. Thus reduction of the communication cost is strongly required in the supercomputing and its straightforward technique is data compression.

Hardware Accelerated DNA Sequencing 550

ZhongPan Wu (York University), Karim Hammad (York University / Arab Academy for Science, Technology and Maritime Transport), Yunus Dawji (York University), Ebrahim Ghafar-Zadeh (York University), Sebastian Magierowski (York University)

Basecalling is a core function in DNA sequencing. It is responsible for the conversion of measured data to a text representation of the DNA's molecular make-up. Recent advances in sequencing machinery have greatly accelerated the rate at which DNA data can be gathered using miniaturized platforms. To keep up, the basecalling function requires substantial computing power. To ease this burden we demonstrate an FPGA-based hardware accelerator for basecalling.

Pulsed Power Network with Scalable Operating Procedure based on Potential Gradient 552

Hisayoshi Sugiyama (Osaka City University)

Pulsed power network is already proposed where electric pulses are directly transmitted among power sources and consumers on synchronized time structure. This scheme is suitable for distributed generations and reliable against partial failures of the network. In this exhibition, a miniature system of the pulsed power network is demonstrated that performs actual power distribution among two power sources and four consumers through eight power routers. Differing from the systems demonstrated before, a scalable operating procedure: potential gradient method is introduced that is applicable even to large scale pulsed power networks.

Session B3L-A: Low Power Design and Modelling

Chair: Mitra Mirhasani, *University of Windsor*

Co-Chair: Sebastian Magierowski, *York University*

Time: Tuesday, August 7, 2018, 13:30 - 15:00

Location: Mercuri

Review on Event-Driven Wake-Up Sensors for Ultra-Low Power Time-Domain Design 554

Nicolas Goux (Université Grenoble Alpes, CEA-Leti), Franck Badets (Université Grenoble Alpes, CEA-Leti)

This paper introduces a review of Event-Driven Wake-Up Sensors interfaces and investigates Time-Domain Injection-Locked Oscillator design solutions to reduce power consumption. Threshold-based sensing, digital classifying and analog feature extraction method are presented. To overcome the power consumption limits provided by State of the Art threshold detection methods, a novel threshold detection method based on Injection-Locked-Oscillator time-domain comparator is proposed. The proposed comparator architecture consumes 790 pW for an input full scale signal of 320 mV with a frequency of 1 KHz.

High-Accuracy, Low-Power Switched-Capacitor Differential-Capacitance-to-Time Converter 558

Satomi Ogawa (University of Yamanashi), Somi Shrestha (University of Yamanashi),

Takahide Sato (University of Yamanashi)

A high-accuracy switched-capacitor (SC) capacitance-to-time (C/T) converter for differential capacitive sensors is presented. In the proposed circuit the propagation delays and the offset voltage of the comparator, the finite gain of the op-amp, and the channel charge injection and clock feedthrough due to analog switches have negligible effect on the accuracy of the circuit. Therefore, the design constraints of op-amp and comparator can be relaxed even for high conversion accuracy. Performances of the proposed circuit are simulated by HSPICE using 0.18 micrometers CMOS process parameters. Simulated results have demonstrated that the gain error is 0.0035 % and the maximum nonlinear error is about 0.015 % of the full scale and indicate that 0.1% resolution is achievable even when low-gain amplifier is used. The power consumption of the proposed circuits was 41.3 microwatts for ± 0.9 V supply voltages.

An Integrated Low-Power Multi-Modal Wide-Dynamic-Range Potentiostat 562

Jifu Liang (Case Western Reserve University), Xinyao Tang (Case Western Reserve University),

Soumyajit Mandal (Case Western Reserve University)

Analyzing trace components in complex samples is important in many research fields. However, factors such as power consumption, input dynamic range, and non-portability limit the efficacy of the devices used for electrochemical analysis. This paper proposes an integrated low-power multi-modal wide-dynamic-range potentiostat to overcome these limitations. A continuous mode and a discontinuous mode are integrated in the circuit to increase its dynamic range. The operation mode and the programmable gain can also be set automatically by a microcontroller. The circuit is realized in the UMC 180 nm process and consumes 60 μ A from a 1.8 V supply with an active area of 350 μ m \times 150 μ m. Both simulations and experimental results prove the functionality of the proposed potentiostat.

Surrogate-Based Optimization-Aided Design for Low Power Analog Circuits 566

Sergio Soto-Aguilar (Texas A&M University), Adriana Sanabria-Borbón (Texas A&M University),

Edgar Sánchez-Sinencio (Texas A&M University)

Automatic analog integrated circuit design is still an open topic. Simulation-based optimization is accurate but relies on the efficacy of heuristics to find a solution. Equation-based optimization is faster but the accuracy depends on the set of equations. We propose an equation-based surrogate model that combines physics-based transistor model, curve fitting approximations for device parameters, and circuit analysis describing the metrics of the circuit to optimize. Two design examples are provided as proof of concept of the proposed optimization framework. The results prove this technique to be effective finding solutions for different processes technologies and flexible to the specifications.

Experimental Study and Modeling of the gm-I Dependence of Long-Channel MOSFETs 570

Michael Cheng (California Polytechnic State University), Vladimir Prodanov (California Polytechnic State University)

This paper describes an experimental study and modeling of the current-transconductance dependence of the ALD1106 and ALD1107 arrays. The study tests the hypothesis that the I-gm dependence of these 7.8 μ m MOSFETs conforms to the Advanced Compact Model (ACM). Results from performed measurements, however, do not support this expectation. Despite the relatively large length, both ALD1106 and ALD1107 show sufficiently pronounced 'short-channel' effects to render the ACM inadequate. As a byproduct of this effort, we confirmed the modified ACM equation. With an m factor of approximately 0.6, it captures the I-gm dependence quite well. The paper also introduces several formulas and procedures for I-gm model extraction and tuning. These are not specific to the ALD transistor family and can be applied to MOSFETs with different physical size and electrical performance.

Session B3L-B: VLSI Digital Arithmetic Circuits

Chair: Arezoo Emadi, *University of Windsor*

Time: Tuesday, August 7, 2018, 13:30 - 15:00

Location: Martis

Design-for-Error-Detection in Implementations of Cryptographic Nonlinear Substitution

Boxes Benchmarked on ASIC 574

Anita Aghaie (Ruhr-University Bochum), Mehran Mozaffari Kermani (University of South Florida),

Reza Azarderakhsh (Florida Atlantic University)

Achieving different security properties through lightweight cryptography has been the focus of recent research efforts. In this paper, we focus on the design criteria of S-boxes transformations (we note that for different ciphers, these transformations might be denoted by other yet similar terms), which provide diffusion and confusion properties in block ciphers, stream ciphers, and hash functions. We also present the results of our implementations for a set of S-boxes used in various block ciphers benchmarked on application-specific integrated circuit (ASIC). The proposed assessments for reliability and error detection of lightweight ciphers is a step forward towards design for error detection while achieving secure implementations.

Lightweight Error Detection Architectures through Swapping the Shares for a Subset of S-Boxes 578

Mehran Mozaffari Kermani (University of South Florida), Amir Jalali (Florida Atlantic University),

Reza Azarderakhsh (Florida Atlantic University)

In this paper, we propose reliable and error detection architectures for 4-bit and a subset of 8-bit strong S-boxes through swapping the shares. In proposing such efficient structures, we make sure that error detection is not a burden to the lightweight architectures of the respective structures. To the best of our knowledge, compared to the recent schemes which are based on error detection through TI concepts and shares for predictors which add area/power overhead comparable to simple redundancy, this paper is the first to propose error detection architectures for such already-protected strong 8-bit S-boxes or the 4-bit ones through recomputing with swapped shares (RESS).

MCML Dynamic Register Design

Neeta Pandey (Delhi Technological University), Kirti Gupta (Bharati Vidyapeeth's College of Engineering),

Bharat Choudhary (Delhi Technological University)

This paper proposes MOS current mode logic (MCML) dynamic register. The register employs tristate buffers working in master-slave configuration. The paper also investigates the behavior of the registers on clock overlap and finds that it do not comply with the desired functionality. Two techniques to achieve clock skew insensitive behavior are proposed. The first technique puts constraints on timing parameter whereas the second technique modifies the enabling mechanism of the buffer. The register operation and their insensitivity towards clock skew are examined through simulations using TSMC 0.18 μm CMOS technology parameters. Various timing waveforms to demonstrate the effectiveness of the proposed techniques are also included.

Asynchronous Early Output Block Carry Lookahead Adder with Improved Quality of Results

P. Balasubramanian (Nanyang Technological University), D.L. Maskell (Nanyang Technological University),

N.E. Mastorakis (Technical University of Sofia)

A new asynchronous early output, relative-timed block carry lookahead adder (BCLA) incorporating redundant carries is proposed. Compared to the best of existing semi-custom asynchronous carry lookahead adders (CLAs) employing delay-insensitive data encoding and following a 4-phase handshaking, the proposed BCLA with redundant carries achieves 14.9% reduction in cycle time and 12.3% reduction in area with no power penalty. A hybrid variant involving a ripple carry adder (RCA) in the least significant stages i.e. BCLA-RCA is also considered that achieves 15.2% reduction in cycle time and 11.2% reduction in area over the best of existing hybrid CLA-RCA variants without power penalty.

An In-Place Processor Design for Real-Value FFTs Targeting in-situ Dynamic ADC Test 591

Brendan Mullane (University of Limerick), Vincent O'Brien (University of Limerick)

This paper presents a processor architecture for Fast Fourier Transform computation of real-valued signals for on-chip analog to digital converter test and evaluation. The design performs a radix-2 technique optimized for low area overhead and easy integration into system on chips. The hardware logic supports variable transform lengths and accurate parameter extraction. The processor has been validated on 0.18 μm CMOS silicon and applied to a data converter test application for extraction of dynamic parameters that are SINAD, SFDR and THD. The architecture is suitable for safety-critical applications where spectral integrity of the converter signal path can be run at start-up or during interval down times.

Session B3L-C: Power Converters

Chair: Po-Hung Chen, *National Chiao Tung University, Taiwan*

Co-Chair: Ayman Fayed, *The Ohio State University*

Time: Tuesday, August 7, 2018, 13:30 - 15:00

Location: Luna

An Average Inductor Current Sensor with Enhanced Accuracy in DCM for Buck Converters 595
Yongjie Jiang (Iowa State University), Sita Asar (Ohio State University), Ayman Fayed (Ohio State University)

An average inductor current sensor with enhanced DCM accuracy for buck converters is proposed. The sensor eliminates sensing errors due to the sense amplifiers' finite bandwidth by employing sample-and-hold techniques to estimate the average inductor current. To enhance accuracy in DCM, the sensor employs DCM-scaling by measuring the conduction time and the switching period of the converter, and uses that information to scale the sensed inductor peak current. The sensor is implemented within a 2-MHz buck converter in 0.5- μm CMOS. Simulations show the error in the sensed average inductor current is only 2% in both CCM and DCM.

An Efficient Complementary Topology Switched-Capacitor based DC-DC Converter 599
Ruikuan Lu (University of Alabama at Birmingham), Mohammad R. Haider (University of Alabama at Birmingham), Yehia Massoud (Stevens Institute of Technology), Nasim Uddin (University of Alabama at Birmingham)

This paper proposes a complementary topology for SC DC-DC converter to enhance the dynamic response. For battery charging unit with faster charging time requirement, one of the major restrictions comes from the equivalent output resistance of the SC DC-DC converter. By connecting one completely symmetric SC converter as complementary topology with the original single converter, the proposed SC DC-DC converter topology decreases the equivalent output resistance down to half. Simulated in 0.13- μm standard CMOS process, the simulation results show that this complementary SC converter gains faster dynamic response, shorter charging time, and higher energy conversion efficiency.

Transient Response Improvement of DC-DC Converter by Current Mode Variable on Time Control 603
Shaowei Zhen (University of Electronic Science and Technology of China), Penghao Zeng (University of Electronic Science and Technology of China), Jiawei Chen (University of Electronic Science and Technology of China), Wanli Zhou (University of Electronic Science and Technology of China), Jiajia Wang (University of Electronic Science and Technology of China), Ping Luo (University of Electronic Science and Technology of China), Bo Zhang (University of Electronic Science and Technology of China)

Constant on Time (COT) control limits equivalent duty cycle due to the minimum off time. Thus the transient response and voltage scaling speed can be improved by changing on time based on COT control. The on time is adaptively controlled by charging capacitor with current of transconductance of error amplifier. The proposed DC-DC converter is designed with 5V input and 0.8V~1.8V output voltage. The load transient response is improved from 5 μs to 3 μs and the undershoot/overshoot are improved from 15mV/30mV to 8mV/20mV, respectively.

Impact Assessment of Electric Vehicle Charging on Distribution Transformers including State-of-Charge 607
Dima Alame (University of Windsor), Maher Azzouz (University of Windsor), Narayan C. Kar (University of Windsor)

The impact of electric vehicle battery chargers with different charging power levels and including state-of-charge on the total harmonic distortion is modeled and quantified through an analysis on the distribution transformer losses, temperature rise and lifetime reduction. In this study, the current harmonic distribution includes harmonic components produced by both conventional and electric vehicle charging loads.

A Fast-Response NMOS-LDO Voltage Regulator without On-Chip Compensated Capacitor
Ping Luo (University of Electronic Science and Technology of China), Zelang Liu (University of Electronic Science and Technology of China), Long Huang (University of Electronic Science and Technology of China), Shaowei Zhen (University of Electronic Science and Technology of China)

A NMOS type low-dropout (NMOS-LDO) voltage regulator with fast transient response is proposed in this paper. The NMOS-LDO is a dual-loop circuit whose inner loop can increase the regulating speed of the output voltage of the proposed LDO, and a NPN is adapted to move the dominant pole from the output point to the inner of the LDO chip without any miller capacitor or other on-chip compensated capacitor. In 0.35 μm CMOS process, the simulation results of the proposed LDO show that the rise time and fall time of LDO are about 2.11 μs and 4.26 μs for 10 μA ~10mA step change of load current.

Session B3L-D: Design, Modelling and Fabrication of Semiconductor Technologies

Chair: Vishal Saxena, *University of Idaho*

Co-Chair: Sudarshan Srinivasan, *North Dakota State University*

Time: Tuesday, August 7, 2018, 13:30 - 15:00

Location: Saturni

Area and Energy Efficient Diode based Spin Orbit Torque Non-Volatile Latch Design 615

*Karim Ali (Data Storage Institute / A*STAR / National University of Singapore), Fei Li (Data Storage Institute / A*STAR), Sunny Y.H. Lua (Data Storage Institute / A*STAR), Chun-Huat Heng (National University of Singapore)*

This paper proposes a compact diode based spin orbit torque non-volatile latch (D-SOT-NVL) design. The proposed NVL can accommodate two different operation schemes. Firstly, a nominal scheme at which the data is stored on the SOT-MTJs when an external enable signal is exerted. Secondly, a special scheme that is only initiated if supply instability is indicated, at which data is stored every clock cycle. In addition, our proposed NVL only needs one overhead (OH) transistor. This is due to the replacement of the read transistor by an oxide based diode. Hence, our NVL achieves only 20% area OH over conventional volatile latch, which is at least 60% smaller than other designs. It also offers at least 21% lower backup energy compared to others. Further study shows that our NVL is robust and stable even with process and device variations.

Design and Compact Modeling of Silicon-Photonic Coupling-Based Ring Modulators for Optical Interconnects 619

Rui Wang (University of Idaho), Md Jubayer Shawon (University of Idaho), Vishal Saxena (University of Idaho)

A compact time-domain Verilog-A modeling methodology is developed for PIC simulation in Cadence environment. With this methodology, basic building blocks for optical system are derived to form the model of coupling-based ring modulator. Parameters used in the developed models are extracted from IMEC Lumerical Interconnect model. One design example of the coupling-based ring modulator is discussed and both of its transmission and transient results are presented. The final Cadence simulation results show that coupling-based ring modulator can realize tunable coupling-coefficient and as a result, renders larger extinction ratio than regular ring modulator.

Design and Demonstration of a Compact Full Adder using Micro-Beam Resonators 623

Sally Ahmed (King Abdullah University of Science and Technology), Saad Ilyas (King Abdullah University of Science and Technology), Nizar Jaber (King Abdullah University of Science and Technology), Xuecui Zou (University of Electronic Science and Technology of China), Ren Li (King Abdullah University of Science and Technology), Mohammad Ibrahim Younis (King Abdullah University of Science and Technology), Hossein Fariborzi (King Abdullah University of Science and Technology)

We present the design, analytical and COMSOL simulations and experimental results of a full adder block using micro-electromechanical resonators with split electrodes. The device operation is based on modulating resonance characteristics by the digital DC inputs. The proposed full adder is implemented with only two devices, considerably less complex than standard CMOS designs which require 24 or more transistors. While the current device has a 0.1 kHz speed and energy/operation in pJ, we show that by scaling the device, higher speed (MHz) and lower energy consumption (sub-fJ) are attainable, which shows the potential of this technology for ultra-low power applications.

Ultra-Low Power Data Converters with BEOL NEM Relays 627

Ren Li (King Abdullah University of Science and Technology), Hossein Fariborzi (King Abdullah University of Science and Technology)

In this work, we explore the implementation of the I/O interface circuits, namely the analog-to-digital converter (ADC) and the digital-to-analog converter (DAC), using back-end-of-line Nano-electromechanical (NEM) relays, for ultra-low power VLSI and IoT applications. Our implementation utilizes multiple optimization strategies, such as custom tuning of the operation voltage of devices in comparators, eliminating static power by adapting a reference-less design, body biasing for low voltage operation, and device sharing for repetitive patterns in encoder and decoder. We show that the proposed design can achieve at least one order of magnitude improved FOM compared to CMOS counterparts.

Design and Fabrication of a Plasmonic Gas Sensor 631

Yangyang Zhao (George Washington University), Mona Zaghoul (George Washington University), Yigal Lilach (George Washington University)

This paper reports a nanohole array based plasmonic gas sensor. We modeled the device by Lumerical FDTD software and then fabricated the device based the simulation result. The fabricated device was verified based on an reflection optical setup. The measurement result matches with the simulation result.

Session B4P-E: Signal Processing Systems

Chair: Wasfy Mikhael, *University of Central Florida*

Co-Chair: Kenneth Jenkins, *Pennsylvania State University*

Time: Tuesday, August 7, 2018, 13:30 - 15:00

Location: Poster Area

Improving Alias Rejection in Two-Stage Comb Filter for Multiple-of-Three Decimation 635

Gordana Jovanovic Dolecek (National Institute of Astrophysics, Optics and Electronics)

This paper presents novel two-stage comb decimation filter for the multiple of three odd decimation factors. The novelty of this filter is the alias improvement in all folding bands at low cost. More specifically, like in comb-zero rotation method, the alias rejection improvement is obtained by placing additional zeros into comb folding bands. However, this is achieved by using simple multiplierless filters, placed in both stages of the comb structure. The second stage is decimated by three, while the first stage is decimated by one third of the overall decimation factor. The choice of multiplierless filters is discussed and the corresponding structures are presented. Finally, the comparisons with some methods, proposed in literature, are provided.

Using OFB and LDPC Coding to Decrease MSE Produced by Gaussian and Impulse Noise 639

L.M. Barba-Maza (National Institute of Astrophysics, Optics and Electronics), G. Jovanovic Dolecek (National Institute of Astrophysics, Optics and Electronics), J. Carmona-Suarez (National Institute of Astrophysics, Optics and Electronics)

This paper presents method to reduce Mean Squared Error (MSE) produced by additive Gaussian noise and impulse noise, using Oversampled Filter Banks (OFB) and Low-Density Parity-Check (LDPC) coding. Two methods are used for the OFB design: Discrete Cosine Transform (DCT) modulation and the Discrete Fourier Transform (DFT) modulation. The same lowpass prototype Finite Impulse Response (FIR) filter is used in both approaches. The polyphase decomposition of the analysis and synthesis filters bank is performed to obtain more efficient structure. The input signal, in the transmitter, is splitted into subbands using the analysis filter bank and coded with LDPC coding. On the receiver side, the inverse process is performed. The proposed method is compared with the similar approaches from literature, using Matlab simulations.

Pulse Compression Optimization by Reactance Transformation: Comparative Application to Different Signal Windows 643

Pietro Burrascano (University of Perugia), Stefano Laureti (University of Perugia), Marco Ricci (University of Calabria)

Pulse compression is a powerful tool to estimate the impulse response of a system in noisy measurement environment conditions. A direct application of this technique, however, implies the introduction of side-lobes that come together with the desired response. A reduction of these side-lobes can be obtained through appropriate windowing techniques: one of these techniques, based on the Reactance Transformation, has recently been proposed by the authors and applied to the Nyquist's Raised Cosine Window. In this paper, the Reactance Transformation technique is applied to a number of windowing techniques, among the most frequently used in NDT. The experimental results show that, when applied to bandpass signals, it always has a positive effect in reducing the side-lobes closer to the main peak, and therefore in improving the range resolution of Pulse Compression-based systems.

A Multi-Phase Detecting Method for Spurs Cancellation in All Digital Fractional-N Phase-Lock Loops 647

Tingbing Ouyang (Peking University Shenzhen Graduate School), Kanglin Xiao (Peking University Shenzhen Graduate School), Xiaoqi Lin (Peking University Shenzhen Graduate School), Changpei Qiu (Peking University Shenzhen Graduate School), Bo Wang (Peking University Shenzhen Graduate School)

The fractional spurs of All Digital Phase-lock Loops (ADPLL) is limited by the resolution and linearity of the time-to-digital converter (TDC). Although a high resolution narrow range TDC can be achieved in digital-to-time converters (DTC) assisted ADPLL, it actually shifts the nonlinearity issue to the DTC block, which may also bring unwanted spurs. In this paper a multi-phase detecting method is proposed for the cancellation of the spur caused by the nonlinearity both from DTC and TDC. The proposed multi-phase detecting architecture contains an inherent finite impulse response (FIR) filter to suppress the fractional spur. What's more, the FIR filter can adapt to the frequency variation of fractional spurs. The simulation results show that this method significantly eliminates fractional spur without adding other noise.

Time Series Generation using Nonlinear Autoregressive Model Artificial Neural Network based Nonlinear Autoregressive Model Design for the Generation and Prediction of Lorenz Chaotic System 651
Lei Zhang (University of Regina)

prediction of Lorenz chaotic system using different Artificial Neural Network (ANN) architectures. Electroencephalogram (EEG) signals captured from brain activities demonstrate chaotic features. In order to theoretically understand brain functionalities, the dynamic chaotic time series outputs of a chaotic system with known system equations can be used to train ANN. And the ANN based NAR model can be used for the simulation and analysis of the chaotic features of brain activities. The ANN architecture design and optimization of the NAR chaotic system model is part of the preliminary research of a multidisciplinary brain research program. The ANN training results of different ANN architectures with 3 to 16 neurons in the hidden layer and 1 to 4 input delays of the NAR model, using training data generated with different step sizes provide important information for the selection of optimal training configuration to optimize the training performance. The research outcome is beneficial for the study of brain activities using EEG.

Evaluation and Optimization of the Bit Rate - Distance Relationships in IR-UWBoF Systems 656
Mohamed Shehata (Cairo University), Mohamed Sameh Said (Cairo University), Hassan Mostafa (Cairo University / Zewail City for Science and Technology)

In this paper, the achievable bit rate as well as the maximum wireless reach of Gaussian and sech-based impulse radio ultrawide band (IR-UWB) signals are investigated. A typical UWB-over-fiber (UWBoF) system incorporating photonic generation and wireless transmission of these waveform types is considered and the performances of both waveform types are compared, with the bit rate - wireless transmission distance as the performance metric of interest. Transmission distances are maximized at the forward error correction (FEC) bit error rate limit under the severe spectral constraints of the Federal Communications Committee (FCC).

Neural Network Topology Formation using Memristive Jaumann Structures 660
Karlheinz Ochs (Ruhr-University Bochum), Dennis Michaelis (Ruhr-University Bochum)

The interconnection of neurons through synapses are essential in the context of learning behavior. This includes the topology formation process in neural networks, i.e., the synaptic coupling of neurons. Memristors are important devices in this context, especially since the formation process must be dynamic. Attaching memristors to a Jaumann structure allows for dynamic topologies that can contain unidirectional couplings. These memristors can be specifically and independently manipulated with this structure as well. Although this work investigates supervised topology formation, the proposed element is a potential candidate for self-organizing systems.

EMG-Based Hand Gesture Control System for Robotics 664
Jonathan Morón (Bradley University), Thomas Diprova (Bradley University), John Reaser Cochrane (Bradley University), In Soo Ahn (Bradley University), Yufeng Lu (Bradley University)

In this paper, a Electromyogram (EMG) based hand gesture control system is developed. A wearable human machine interface (HMI) device is designed for an in-home assistance service robot. An EMG-based control system utilizes MyoWave muscle sensor to acquire and amplify EMG signal. A microcontroller system is used to an artificial neural network (ANN) to classify the EMG signal. Based on different hand movements, commands are sent through WiFi to control the motor in a service robot. The on-board Camera system mounted the robot can capture video real-time. In addition, a web server is implemented to provide live video feedback for robot navigation and user instructions.

Neuromorphic Object Tracking Architecture, based on Compound Eyes, and Implementation on FPGA 668
Satrajit Chakraborty (Indian Institute of Science), Priyanka P (Indian Institute of Science), Sarthak Gupta (Indian Institute of Science), Saeed Afshar (Western Sydney University), Tara Hamilton (Western Sydney University), Chetan Singh Thakur (Indian Institute of Science)

As per recent findings in Neuroscience, a housefly/blowfly tracks a object with astonishing accuracy using its compound eye structure steered by the neural circuit distributed behind each photo-receptor. The working of these Neural circuits can be modeled as set of Leaky Integrate and Fire neurons connected in a special manner which gives rise to a competitive feedback control. Based on these, a neuromorphic competitive control circuit utilizing an inference neuron is modeled and simulated in software and then implemented on FPGA. The results show an observable decoherence phenomenon between the neurons and support the working principle of the model.

Controlling Robot Gripper Force by Transferring Human Forearm Stiffness using Force Myography 672
Mohammad Anvaripour (University of Windsor), Mehrdad Saif (University of Windsor)

This paper presents an approach for human-robot cooperation by transferring human forearm stiffness to the robot. The essential element of the proposed approach is Force Myography (FMG) of the forearm muscles that provide the robot with the human arm stiffness while picking up a part. Through this framework, the robot controller can adapt its gripper force to imitate human behavior facing different parts in weights and sizes during the cooperation. The proposed method is evaluated experimentally in picking-up and moving the pieces tasks that are common activities in industries. The results demonstrate that the robot can control its arm gripper force facing with different parts with the error less than 2%, that depicts the effectiveness of the proposed method.

Bit Error Probability Analysis for OFDM-IM over Faded Shadowing Channel 676

Ibrahim Aboharba (Western University), Quazi Rahman (Western University), Raveendra K. Rao (Western University)

Orthogonal frequency division multiplexing with Index Modulation (OFDM-IM) has been utilized to transmit extra bits by indexing subcarriers using the ON-OFF keying modulation. In this paper, performance of OFDM-IM system is studied, in terms of bit error probability, over a composite Nakagami-m Gamma (NG) shadowed fading channel. The closed form expressions of approximate and exact average BEP (ABEP) of M-ary QAM modulation and pairwise error probability (PEP) are derived for OFDM-IM over the aforementioned channel. The theoretical results are compared with existing research studies and verified using simulation.

A 45% PAE pMOS Power Amplifier for 28GHz Applications in 45nm SOI 680

Devon Thomas (University of California, San Diego), Narek Rostomyan (University of California, San Diego), Peter Asbeck (University of California, San Diego)

A power amplifier with peak power-added efficiency above 45% at output power of 19dBm implemented with pMOS in a 45nm SOI process is reported. The power amplifier operates over 25 to 31GHz, and employs two stacked FETs with gate width 306 μ m, using an accelerator capacitor to increase gain and efficiency. pMOS PAs are of interest because they provide higher immunity to hot-carrier injection than nMOS counterparts. To the authors best knowledge, the PA provides the highest reported PAE for 28GHz applications of any pMOS circuit, and has efficiency comparable to the best reported for nMOS, SiGe HBT and GaAs circuits.

2-Dimensional FIR Digital Filter Design using Teaching-Learning-Based Optimization 684

Hon Keung Kwan (University of Windsor), Miao Zhang (University of Windsor)

In this paper, weighted least-squares (WLS) design of 2-dimensional nonlinear phase circularly symmetric finite impulse digital filters using teaching-learning-based optimization is presented. To improve the performance of the teaching-learning-based optimization algorithm, an elitist replacement with mutation is applied to the worst solution in a population. Three 2-D nonlinear phase FIR lowpass digital filters are designed and the results indicate that lower mean squared complex errors can be obtained as compared to those obtained by another design method.

Group Delay Equalizer Design using Harmony Search Algorithm 688

Hon Keung Kwan (University of Windsor)

Allpass group delay equalizer design using harmony search algorithm is presented. Elliptic IIR lowpass and bandpass digital filters are first designed to meet given passband and stopband(s) magnitude response specifications. For each of the lowpass and bandpass digital filters, a cascaded allpass digital filter is then designed to equalize the IIR passband group delay such that the normalized group delay error of the combined passband group delay is minimized. The allpass equalizer design results indicate that the approach using harmony search algorithm can achieve slightly improved results as compared to other methods.

Using Mixed DCT and Haar Transforms for Efficient Compression of Car Trajectory Data 692

Masoumeh Kalantari Khandani (University of Central Florida), Wasfy B. Mikhael (University of Central Florida)

In this paper we propose a method for adopting the concept of mixed-transforms and evaluate it for vehicle trajectory data. In mixed-transform methods, compression residuals from the first representation of a signal are passed to a second transformation stage where further compression is applied in that domain. The final residual which represents error resulting from the compression and decompression process, is then used as a cost to be minimized by adjusting the configuration of each transformation stage. An adaptive algorithm from earlier works is adopted to iteratively adjust the configuration of each compression stage (selection of coefficients from each transform) to minimize the error. A hierarchical realization of the iterative adaptive algorithm is presented that uses preset compression ratios and optimizes the coefficient selection accordingly. We show that using DCT followed by Haar in the proposed method, it is possible to efficiently compress vehicle trajectory data. The results show that a higher quality for reconstructed data can be achieved using this method, compared to using a single transform compression.

Session B5P-E: System Architecture, Hardware, Software Co-Design

Chair: Sazzadur Chowdhury, *University of Windsor*

Co-Chair: Fathi Hassan Amsaad, *The University of Toledo*

Time: Tuesday, August 7, 2018, 15:30 - 17:00

Location: Poster Area

Modeling and Application for Negative-Differential-Conductance Devices with Single-Electron Technology 696

Lin Li (University of Windsor), Chunhong Chen (University of Windsor)

Negative-differential-conductance (NDC) devices can find many applications in both digital and analog circuit design. This paper presents an implementation of NDC using single-electron-tunneling technology with applications to memory cell and Schmitt trigger design. A piece-wise linear model is used to describe the I-V characteristics of the NDC for efficient performance analysis and optimization. Simulation results are shown to verify the effectiveness of the proposed model with considerations of temperature effects for circuit applications.

A Low Cost BCB based 77 GHz Microstrip Aperture Coupled Antenna Array for Automotive Radars 700

Sreejit Chatterjee (University of Windsor), Sazzadur Chowdhury (University of Windsor)

A BCB based 77 GHz aperture coupled microstrip antenna array for autonomous vehicle radars has been presented. The 5x8 elements array exhibits a broadside gain of 17.28 dBi and a directivity of 22.95 dBi that can cover a range of 150-200m to satisfy the requirements set forth by the auto industry. An innovative air-filled dielectric cavity has been introduced in the BCB layer to obtain a synthesized dielectric constant of 1.066. The array exhibits a return loss of -25 dB at 77 GHz with a HPBW of 10 degrees. The antenna can be batch fabricated using conventional microfabrication techniques.

Field Ionization Gas Sensors based on ZnO Nanowire 705

Sevin Samadi (Concordia University), Parsoua Abedini Sohi (Concordia University),

Javad Dargahi (Concordia University), Mojtaba Kahrizi (Concordia University)

In this work we report design and characteristics of a field-ionization gas breakdown sensor based on ZnO nanowires. ZnO nanowires fabricated using electrochemical technique on metal-coated silicon samples, were placed between two parallel plates separated by a small gap. Attention was paid to adjust growth parameters to produce nanowires which are most suitable for this purpose. The device was designed, fabricated and tested for Ar, N₂, O₂ and He gases in a pressure range of 0.1 < P < 10 Torr.

Random Number Generator based on Hydrogen Gas Sensor for Security Applications 709

Celal Erbay (TÜBİTAK), Salih Ergün (TÜBİTAK)

This paper presents RNG based on a hydrogen gas sensor which is fabricated by using microfabrication techniques. The proposed approach extracts the thermal noise information as an entropy source from the gas sensor which is non-deterministic during its operation. This non-deterministic noise is then processed to acquire a random number set fulfilling the NIST 800-22 statistical randomness test suite and it demonstrates that a gas sensor based RNG can provide high quality random numbers. Secure data transfer is possible by having this method directly without any other hardware where hydrogen gas sensor needs to be used such as petrochemical field, fuel cells, and nuclear reactors.

An Approach for Modeling Spatial Prepositions with RDF Reification and Blank Nodes based on the Environment Perception of a Simulated Mobile Robot 713

Nazeer T. Mohammed Saeed (University of Siegen), Christian Weber (University of Siegen), Madjid Fathi (University of Siegen), Klaus-Dieter Kuhnert (University of Siegen)

Today, thanks to the advancement of robotics and the achievements that are made in the light of the development of automated and intelligent technologies, we are increasingly witnessing the arrival of robotic devices and machines into different areas of human life. With all of the achievements and their intelligence, the degree of their proficiency relies in many cases on their ability to interact with human beings. To do so, for a mobile robot the ability to understand its surroundings and also to describe it in a way that human can easily understand is vitally important.

Knowledge-Based Production Documentation Analysis: An Integrated Text Mining Architecture 717

Johannes Zenkert (University of Siegen), Christian Weber (University of Siegen), André Klahold (University of Siegen), Madjid Fathi (University of Siegen), Kai Hahn (University of Siegen)

Across the landscape of high technology companies, knowledge is a vital core resource at the heart of the organization. The technological complexity is steadily rising, tightening the global demands which are leading to an aggravating conflict on the product: it has to be produced faster, cheaper, more customer related and all without failures, while the change of complexity is inviting new unseen potentials for faults. On top, a new need for an agile production is arising. While today's organizational knowledge is captured and managed by an increasing number of processes and methodologies, solutions to continuously re-integrate the captured knowledge into the overall process of design and production are still scarce. This paper presents an integrated and agile process that proposes an integrative text mining architecture for design and process analytics.

Age-Related Macular Degeneration Diagnostic Tools: Hardware and Software Development 721

N. Mohaghegh (York University), S. Munidasa (York University), Q. Owen (York University), X. Zihao (York University), S. Magierowski (York University), E. Ghafar-Zadeh (York University)

The paper proposes the design and implementation of hardware and software for visual assessment of patient suffering from macular diseases. In this method, a group of graphical patterns are displayed and the patient's responses are collected. The collected data is used to reveal the progress of macular degeneration. Herein we put forward the proposed software method along with various alternative hardware methods to display and collect the data from the patients. We demonstrated the development of devices including the human computer interface (HCI) smart glove. Also the characterization results for the measurement of response time to each pattern along with the systematic error were achieved using twenty human subjects. The proposed hardware /software platform is the best solution for the visualization assessment dedicated to the patients with a macular disease such as AMD.

Dynamics of ML Approaching Randomized Decoders on Graphs with Cycles 725

Saied Hemati (University of Idaho)

Randomized channel decoders are promising candidates for approaching maximum-likelihood (ML) decoding using low-complexity decoders when decoding latency is not a concern. This paper is focused on the dynamics of randomized decoders and divides these decoders to statically and dynamically randomized decoders. It is shown that some statically randomized decoders are ML achieving. For dynamically randomized channel decoders that are defined on graphs with cycles, it is shown that randomness can alleviate the impact of cycles.

Stochastic Computing based BCH Decoder for WBAN Systems 729

Kaining Han (McGill University), Junchao Wang (McGill University), Warren J. Gross (McGill University)

BCH codes have been accepted as the error correction coding scheme by the IEEE 802.15.6 standard for wireless body area networks (WBAN). Soft-decision BCH decoders are attractive for the reason that the decoding gains result in significant transmitting energy reduction. An approximate computing technology called stochastic computing is a promising low power and low hardware cost implementation candidate for BCH soft decision decoders. In this paper, a stochastic computing based soft decision decoder is presented for the BCH code defined in the IEEE 802.15.6 standard. According to the evaluation results, the proposed design has the advantages of energy consumption and hardware cost while approaching the decoding performance in terms of block error rate (BLER) compared to existing BCH soft decision decoders. In addition, the proposed design requires no noise power estimation for the soft decision demodulation module, which could further reduce the hardware cost and energy consumption of the WBAN receiver.

A Survey on Fault-Tolerant Supervisory Control

Mohammad Karimadini (Arak University of Technology), Ali Karimoddini (North Carolina Agricultural and Technical State University), Abdollah Homaifar (North Carolina Agricultural and Technical State University)

System fault occurrences are arbitrary, costly, and at times deadly. Therefore, it is important to systematically and robustly react to occurred faults in a timely manner to recover the system. In this paper, we survey the notion of fault in supervisory control of discrete event systems. This paper particularly reviews the results on fault-tolerant supervisory control, robust supervisory control and reliable supervisory control in order to investigate the functionality of distributed discrete event systems in faulty conditions. The insights help the designers to understand under what faulty conditions a cooperative supervisory control scheme remains valid and how to synthesize the supervisory control of discrete event systems as fault-tolerant as possible.

Dual-Mode Forward Collision Avoidance Algorithm based on Vehicle-to-Vehicle (V2V) Communication 739

Mohamed Yousef (Institute of Aviation Engineering and Technology), Ahmed Hosny (Institute of Aviation Engineering and Technology), Wessam Gamil (Institute of Aviation Engineering and Technology), Mohamed Adel (Institute of Aviation Engineering and Technology / Cairo University), Hazem M. Fahmy (Germany University in Cairo), M. Saeed Darweesh (Institute of Aviation Engineering and Technology / Zewail City of Science and Technology), Hassan Mostafa (Cairo University / Zewail City for Science and Technology)

This paper proposes a Vehicle-to-Vehicle (V2V) communication-based forward collision avoidance algorithm by alarming the driver for the normal driver mode and controlling the driving wheel for the self-governed (autonomous) driving mode. The proposed algorithm benefits from the information exchange between the host vehicle and the leading vehicle to calculate the safe distance between host vehicle and leading vehicle to guarantee the avoidance of the collision. The proposed system gives advisory and imminent warnings according to the predicted accident levels, using a three different levels of collision avoidance for the driver mode. Also, in the autonomous driving mode, it follows an alternative optimal path to avoid the collision. The simulation results are implemented using Prescan and MATLAB. The simulation results show that the proposed collision avoidance system makes a composite analysis of the collision risk and provides an accurate real-time warning and an alternative path for dual driving modes.

An Overview of Recent Convolutional Neural Network Algorithms for Image Recognition 743

Genevieve Sapijaszko (University of Central Florida), Wasfy B. Mikhael (University of Central Florida)

An important aspect of a guidance system in an autonomous vehicle is the detection of objects and extraction of reliable features that can identify the object from images. Object detection methods have evolved in the last 20 years, with convolutional neural network algorithms in particular showing promise. This paper compares and contrasts recent convolutional neural network algorithms using the BelgiumTS Dataset. The different convolutional neural networks used and compared are AlexNet, VGGNet, GoogleNet, and ResNet. The object detection methods will be used to find the best processing speed and recognition rate among the convolutional neural networks. A survey of published state-of-the-art, convolutional neural networks are evaluated against published results.

Session B6L-A: Low Power and Low Density Communication Systems

Chair: Arjuna Madanyake, *University of Akron*

Co-Chair: Magdy Bayoumi, *University of Louisiana*

Time: Tuesday, August 7, 2018, 15:30 - 17:00

Location: Mercuri

40 Gbit/s 4-PAM VCSEL Driver Circuit with Power Roll-Off Compensation 747

Guido Belfiore (Technische Universität Dresden), Ronny Henker (Technische Universität Dresden),

Frank Ellinger (Technische Universität Dresden)

This paper presents the design and measurements of a 4-level pulse-amplitude-modulation (4-PAM) vertical-cavity surface-emitting laser (VCSEL) driver integrated circuit for short-range, high-speed optical communications. The goal of this design is to compensate the power roll-off of VCSELs in order to exploit as much as possible their dynamic range. The circuit is manufactured in a 130 nm SiGe technology and achieves a transmitted optical data rate of 40 Gbit/s. The driver power consumption is only 177 mW including the VCSEL. Thanks to the inductorless design, the chip active area is limited to 0.2 mm². To the best of the authors' knowledge, this is the first multilevel laser driver designed to counteract the power roll-off effect of VCSELs.

Low-Power and High-Linearity Inductorless Low-Noise Amplifiers with Active-Shunt-Feedback in 65-nm CMOS Technology 751

Toshiyuki Inoue (University of Shiga Prefecture), Ryosuke Noguchi (University of Shiga Prefecture),

Akira Tsuchiya (University of Shiga Prefecture), Keiji Kishine (University of Shiga Prefecture),

Hidetoshi Onodera (Kyoto University)

We report a low-power and high-linearity inductorless low-noise amplifier (LNA) with active-shunt-feedback in 65-nm CMOS technology. Noise-cancelling was shown to be achieved by adding a coupling capacitor between NMOS and PMOS amplifiers and adjusting its capacitance in a circuit simulation. The measured frequency response of the power gain had good agreement with the post-layout simulated results. A linearity higher than that of the conventional active-shunt-feedback type LNA in 0.13-um CMOS technology was obtained.

The Probabilistic Finite Alphabet Iterative Decoder for Low-Density Parity-Check Codes

Khoa Le (École Nationale Supérieure de l'Electronique et de ses Applications), Fakhreddine Ghaffari (École Nationale Supérieure de l'Electronique et de ses Applications), David Declercq (École Nationale Supérieure de l'Electronique et de ses Applications)

This paper proposes a new concept in applying the Non-Surjective Finite Alphabet Iterative Decoder (NS-FAID) for the Low-Density Parity-Check (LDPC) decoding. Differently from the NS-FAID which applies a fixed nonlinear function by using a fixed Look-Up-Table (LUT) on the variable node messages, the proposed method, called Probabilistic FAID (PFAID), uses more than one LUTs and with a probabilistic way. By using the density evolution, we show that this method provide a significant improvement in performance compared to the NS-FAID and the traditional MS. The advantage of PFAID is shown by the fact that, a PFAID with low message quantization level can reach or even surpass the performance of the higher level quantization MS decoder. Furthermore, we show that PFAID can be efficiently implemented with no hardware overhead compared to MS or NS-FAID with the same message quantization level. The hardware complexity analysis and decoding simulation performance are provided as superiority evidences of PFAID over the reference benchmarks.

Power-Efficient Data Modulation for All-Mechanical ULF/VLF Transmitters 759

Md Tawhid Bin Tarek (University of Akron), Shamini Dharmasena (University of Akron), Arjuna Madanayake

(University of Akron), Seungdeog Choi (University of Akron), Jarred Glickstein (Case Western Reserve

University), Jifu Liang (Case Western Reserve University), Soumyajit Mandal (Case Western Reserve University)

Miniaturized and power-efficient ULF/VLF (0.3-30 kHz) transmitters are desirable for underground and undersea wireless communications. Transmitters based on rotating permanently-polarized dipoles are promising for such applications. This paper proposes a power-efficient data modulation scheme for such mechanical transmitters based on continuous frequency FSK (CF-FSK). Theoretical analysis and simulations show that 8-ary CF-FSK is optimal since it minimizes average mechanical torque for a given bit rate. Model predictive control (MPC) of a permanent magnet (PM) motor is proposed for robust implementation of the data modulation scheme. Preliminary results from an experimental prototype are also presented.

Sensor Readout Circuit with Integrated Baseband Modulation for Low Power Backscatter Tags 763

Andreas Brönnner (WIK A Alexander Wiegand SE & Co. KG), Frank Ellinger (Technische Universität Dresden)

A sensor readout circuit with integrated baseband modulation is implemented in 130nm BiCMOS for application in harsh environments. The circuit is optimized for the use in millimeter wave passive backscatter sensor tags, featuring low power consumption of 5.1 μ W and a minimized chip area of 0.004 mm², which to the knowledge of the authors is the lowest of its class. To benefit from the shorter read ranges in millimeter wave passive backscatter tags, we assume only one tag is in the penetrating field of the reader. Therefore it is possible to integrate the modulation into the readout circuit, minimizing the size and power consumption of the tag. The readout circuit is tested together with temperature sensing elements showing a resolution of 0.0085 K at a sampling frequency of 114 Hz while the standard deviation is 0.086 K.

Session B6L-B: VLSI Digital Integrated Circuits II

Chair: Nader Rafla, *Boise State University*

Co-Chair: Sudarshan Srinivasan, *North Dakota State University*

Time: Tuesday, August 7, 2018, 15:30 - 17:00

Location: Martis

An Equivalence Verification Methodology for Combinational Asynchronous PCHB Circuits 767

Ashiq A. Sakib (North Dakota State University), Scott C. Smith (North Dakota State University), Sudarshan K. Srinivasan (North Dakota State University)

Pre-Charge Half Buffer (PCHB) is a Quasi-Delay Insensitive (QDI) asynchronous design paradigm that has found commercial applications in the semiconductor industry. PCHB circuits use dual-rail signals instead of Boolean logic and are unique in that PCHB gates incorporate both registration and a handshaking scheme for synchronization. We have developed a methodology for formal equivalence verification of combinational PCHB circuits against their corresponding Boolean specification circuits. The methodology transforms the PCHB circuit into a Boolean circuit, which can then be checked against a Boolean specification circuit using an existing combinational equivalence checker. The methodology also checks for liveness and handshaking correctness of the original PCHB circuit. The proposed methodology has been demonstrated using several multipliers and ISCAS circuit benchmarks.

Novel 3D Monotonic Characterization of Standard Cell Liberty File Attributes w.r.t ASIC Tool Flow

Lalitha Mohana Kalyani Garimella (Intel Corporation), Sri Raga Sudha Garimella (New Mexico State University)

Standard library cells (STD cells) being basic building blocks for ASIC/CPU design, play a key role in PPA enhancement and hence in design perfection. This paper presents first of its kind research to bridge the gap between conventional STD cell monotonic characterization and resulted STD cell liberty format file (.lib file) attributes usage with respect to ASIC tool cost function in an ASIC/CPU design and proposes a novel 3 dimensional (3D) monotonic characterization method for PPA boosting. An Algorithm for characterizing 3D monotonic cells is defined. About 10% to 60% of library cells are observed to be non-3D-monotonic in various libraries, architecture of libraries, and technology of libraries. Primetime results proving that selecting 3D-monotonic cells in an existing library using the algorithm give excellent PPA gain. By repairing non-3d-monotonic cells to cells fitting 3D-monotonic characterization, summary of post-route, post-extracted, primetime results from study of several projects showed further PPA improvement. PPA gain and advantages varies with ASIC flow settings, ASIC tool vendors, size of CPU, performance target, etc... with no disadvantages.

Routing Aware and Runtime Detection for Infected Network-on-Chip Routers 775

Luka Daoud (Boise State University), Nader Rafla (Boise State University)

Network-on-Chip (NoC) has become a target to security attacks. By experiencing outsourcing design, NoC can be infected with a malicious Hardware Trojans (HTs) which potentially degrade the system performance or leave a backdoor for secret key leaking. In this paper, we propose a HT model that applies a denial of service attack by misrouting the packets, which causes deadlock and consequently degrading the NoC-based system. We provide a runtime HT detection and avoiding modules through a proposed secure routing algorithm. Results show that our proposed model has negligible overhead in area and power, 0.4% and 0.6%, respectively.

A Temperature and Process Corner Insensitive Design Method for Digital Circuits in 40nm CMOS

Marcel Runge (Technical University of Berlin), Sebastian Linnhoff (Technical University of Berlin), Friedel Gerfers (Technical University of Berlin)

This paper proposes a digital design method enabling a constant path delay across temperature and process corners in 40nm CMOS. Thus, timing analysis and logic synthesis is simplified significantly. The temperature dependency is eliminated by operating at the zero temperature coefficient supply voltage. Additionally, process corner adaptive body biasing compensates process corner dependent path delays. Extensive transistor level simulations for various standard cells show constant path delays across temperature and 6 sigma process corners. All applied body bias voltages lie within the transistor reliability. This method enables rapid digital synthesis without time consuming process and temperature analyses and optimization.

Session B6L-C: Digital Signal Processing for Medical Applications

Chair: M.N.S. Swamy, *Concordia University, Montreal, Canada*

Co-Chair: M. Omair Ahmad, *Concordia University, Montreal, Canada*

Time: Tuesday, August 7, 2018, 15:30 - 17:00

Location: Luna

On the Practicability of Images Processing Methods for xMR Arrays 783

Phil Meier (Ostfalia University of Applied Sciences), Kris Rohrmann (Ostfalia University of Applied Sciences), Marvin Sandner (Ostfalia University of Applied Sciences), Marcus Prochaska (Ostfalia University of Applied Sciences)

In field of angular position sensing MR sensors play a dominant role, because of their high accuracy and robustness. However, upcoming vehicle concepts lead to increasing requirements, which cannot be fulfilled by available sensors. Thus, in this paper promising signal processing methods for MR sensor array are investigated. Three well known image processing methods are adapted to magnetic field sensors arrays for angular detection. The presented methods are compared and judged regarding their applicability.

A Wearable ECG Monitoring System for Real-Time Arrhythmia Detection 787

Nicholar Clark (Bradley University), Edward Sandor (Bradley University), Calvin Walden (Bradley University), In Soo Ahn (Bradley University), Yufeng Lu (Bradley University)

This study develops a wearable medical system for real-time arrhythmia detection, which acquires electrocardiogram (ECG) data through a three-lead ECG sensor. It performs ECG signal processing and immediately alerts the patient's health care provider of an arrhythmia via wireless messaging. In particular, a common form of arrhythmia known as premature ventricular contractions (PVCs) are identified using the Pan-Tompkins and the wavelet-based template-matching algorithms. When three or more consecutive PVCs are detected, the device sends urgent report email to a patient's health care provider. In the experimental study, the design has been successfully validated using benchmark records from the MIT-BIH arrhythmia database. A low-cost Texas Instruments TMS320C5515 and Raspberry Pi 3 Model B are chosen to be the hardware platform. This study suggests a viable, low-complexity solution for real-time heart monitoring and arrhythmia detection.

Deep Structural and Clinical Feature Learning for Semi-Supervised Multiclass Prediction of Alzheimer's Disease 791

Emimal Jabason (Concordia University), M. Omair Ahmad (Concordia University), M.N.S. Swamy (Concordia University)

In recent years, the accurate early diagnosis of Alzheimer's disease (AD) using different biomarkers through machine learning techniques has been the hottest research in preventing, treating, and slowing down the progression of the disease. However, a common bottleneck of the diagnostic performance is overfitting due to having lot of irrelevant features in the training data. In view of this fact, we propose a novel classification framework which uses unsupervised autoencoder to select the subset from given structural and clinical features followed by a supervised layer to automatically identify the patients having AD, mild cognitive impairment, and cognitively normal.

Linear and Nonlinear Feature Extraction for Neural Seizure Detection 795

Mohamed A. Elgammal (Cairo University), Omar A. Elkhoully (American University in Cairo), Heba Elhosary (German University in Cairo), Mohamed Elsayed (Zewail City of Science and Technology), Ahmed Nader Mohieldin (Cairo University), Khaled N. Salama (King Abdullah University of Science and Technology), Hassan Mostafa (Cairo University / Zewail City for Science and Technology)

In this paper, both linear and nonlinear features have been reviewed with linear support vector machine (SVM) classifier for neural seizure detection. The work introduced in the paper includes performance measurement through different metrics: accuracy, sensitivity, and specificity of multiple linear and nonlinear features with linear support vector machine (SVM). A comparison is performed between the performance of different combinations between 11 linear features and 9 nonlinear features to conclude the best set of features. It is found that some features enhance the detection performance greatly. Using a combination of 3 features of them, a linear SVM classifier detects seizures with sensitivity of 96.78%, specificity of 97.9%, and accuracy of 97.9%.

Session B6L-D: Diagnostics and Fault Tolerant Control System I

Chair: Roozbeh Razavi-Far, *University of Windsor*

Time: Tuesday, August 7, 2018, 15:30 - 17:00

Location: Saturni

Discriminative Clustering of High-Dimensional Data using Generative Modeling 799

Masoud Abdi (Deakin University), Chee Peng Lim (Deakin University), Shady Mohamed (Deakin University), Saeid Nahavandi (Deakin University), Ehsan Abbasnejad (University of Adelaide), Anton Van Den Hengel (University of Adelaide)

We presents a novel approach to unsupervised clustering based on variational autoencoder and generative adversarial network using a shared latent variable. We have shown that our method is able to cluster the high-dimensional data effectively. In addition to the discriminative results, our method yields an effective generative model that is able to produce highly realistic samples from the data distribution.

A Critical Study on the Importance of Feature Extraction and Selection for Diagnosing Bearing Defects 803

Maryam Farajzadeh-Zanjani (University of Windsor), Roozbeh Razavi-Far (University of Windsor), Mehrdad Saif (University of Windsor)

This paper presents a general data-driven diagnostic scheme to classify bearing faults in induction motors. Case western reserve university bearing data center are used to create two scenarios with different fault diameters of 0.007 and 0.014 that are induced in the inner race, the ball and the outer race. The diagnostic system could successfully conduct signal processing and classification steps to achieve an accurate condition assessment of the motor. In this work, the vibration signal is decomposed into several number of components by means of five different state-of-the-arts signal processing techniques. The extracted features which belong to the Time-domain, the Frequency-domain and the Time-Frequency domain are employed to create a pool of diverse features. Moreover, a feature selection strategy based on the correlation of the features to motor operating conditions is assessed. The obtained result shows that the combination of the most correlated features could provide an informative feature set for the fault classification and improve the diagnostic accuracy.

Near-Optimal Design for Fault-Tolerant Systems with Homogeneous Components Under Incomplete Information 809

Jalal Arabneydi (McGill University), Amir G. Aghdam (Concordia University)

In this paper, we study a fault-tolerant control for systems consisting of multiple homogeneous components such as parallel processing machines. This type of system is often more robust to uncertainty compared to those with a single component. The state of each component is either in the operating mode or faulty. At any time instant, each component may independently become faulty according to a Bernoulli probability distribution. If a component is faulty, it remains so until it is fixed. The objective is to design a fault-tolerant system by sequentially choosing one of the following three options: (a) do nothing at zero cost; b) detect the number of faulty components at the cost of inspection, and c) fix the system at the cost of repairing faulty components. A Bellman equation is developed to identify a near-optimal solution for the problem. The efficacy of the proposed solution is verified by numerical simulations.

Torsional Vibration Identification using Electrical Signatures Analysis in Induction Machine-Based Systems 813

Shahin Hedayati Kia (University of Picardie Jules Verne), Roozbeh Razavi-Far (University of Windsor), Mehrdad Saif (University of Windsor)

This paper deals with a general approach to the feasibility study of the torsional vibration recognition through electrical signatures analysis in induction machine-based systems. The prior works on this specific topic have shown that in case of gear tooth localized fault, the amplitude of main torsional resonance frequency of the electromechanical system was amplified in the stator current space vector instantaneous frequency. Following this initial successful attempt, this work is conducted to establish a common procedure which defines the response of electrical signatures to the torsional vibrations induced by a fault located on the mechanical drive train. The most sensitive electrical signature can be considered for feature extraction and non-invasive torsional vibration analysis accordingly. An experimental setup based on a 250W three-phase squirrel-cage induction machine shaft-connected to a single-stage spur gear is utilized for validation of the proposed approach.

Robust Fractional-Order Lag/Lead Compensators 817

Reyad El-Khazali (Khalifa University)

this paper introduces a new design method of fractional-order robust lag/lead compensators. The proposed compensators are realizable and exhibit a frequency response of fractional-order dynamics. The structure of such controllers allows one to alternate between lag/lead forms by simply interchanging two parameters with each other. An analytical design method of these controllers is simplified to reduce the number of design parameters to two; the gain and one corner frequency of the compensator. It also ensures a robust flat phase response at their geometric mean, especially for those controllers of fractional-orders between $0.5 < \alpha < 1$. The proposed design method is straightforward and demonstrate a competitive performance to other existing ones as verified via set of numerical examples

Wednesday, August 8, 2018

Session C1L-A: Digital Signal Processing

Chair: Esam Abdel-Raheem, *University of Windsor*

Time: Wednesday, August 8, 2018, 8:30 - 10:00

Location: Mercuri

A Normalized Filtered-X Generalized Fractional Lower Order Moment Adaptive

Algorithm for Impulsive ANC Systems 821

Muhammad Tahir Akhtar (Nazarbayev University)

This paper proposes an efficient algorithm for impulsive active noise control (IANC) systems. The impulsive sources cannot be modeled by Gaussian distribution, and hence the standard adaptive algorithm based on second order statistics would give poor performance or even fail to converge. One solution is to derive adaptive algorithm by minimizing a fractional low order moment, resulting in the famous filtered-x least mean p-power (FxLMP) algorithm. The proposed algorithm discussed in this paper is based on a previously proposed generalized FxLMP algorithm. The key idea here is to introduce a variable step-size using a convex-combination approach. A large value is used at the start-up of IANC system to achieve a fast convergence speed. As the AINC system converges, the step-size automatically reduces to a small value to improve the steady-state noise reduction performance. Simulations demonstrate the effectiveness of the proposed algorithm.

An Audio Self-Recovery Scheme that is Robust to Discordant Size Content Replacement Attack

Juan Jose Gomez-Ricardez (Cinvestav), Jose Juan Garcia-Hernandez (Cinvestav)

One of the more severe attacks for self-recovery schemes is the discordant size content replacement attack. This attack substitutes a set of samples from an audio signal with another set of samples of different sizes. In this paper, a watermarking scheme for digital audio self-recovery that is robust to the discordant size content replacement attack is proposed. Our goal is to recover a tampered audio signal after such an attack. In particular, our scheme models the problem using source-channel coding. This method generates a watermarking where a lossy compressor is applied and the source coding output is protected with a channel coder. The coded data is then distributed into the original audio signal. In the recovery stage, a synchronization strategy is used to synchronize the watermark and this makes audio signal self-recovery possible. Our results shows that the propose scheme is robust to the discordant size content replacement attack for attacks of about 20% of the whole audio.

Load Impedance Digital Filter for Tuning the Resonance of a Composite Piezoelectric Transducer 829

Michael Santora (University of Detroit Mercy), David Egolf (University of Idaho)

This research involves the development of an active muffler, an Electromechanical Active Helmholtz Resonator (EMAHR), that suppresses the fundamental frequency being exhausted through an engine's tailpipe. The EMAHR is a tracking side-branch resonator terminated with a composite piezoelectric transducer. The EMAHR creates a notch that can be moved between 200-1000 Hz which can be moved with an impedance consisting of negative capacitance, an inductance varying from positive to negative, and positive or negative resistance. Described in this paper is the required electrical load, and the development and selection of a digital filter that is implemented in an impedance generation circuit.

Blind Source Separation as Pre-Processing to Unsupervised Keyword Spotting via an ICA Mixture Model

Muhammad Azam (Concordia University), Nizar Bouguila (Concordia University)

In this paper, we propose blind source separation (BSS) as pre-processing to unsupervised keyword spotting. We adopted our recently proposed keyword spotting and employed BSS framework to improve the detection rate in keyword spotting when speech signals are affected by mixing. BSS can improve the performance of keyword spotting, when intelligibility of speech signals is affected by mixing of noise or other speech signals. The TIMIT speech corpus is employed to examine the effectiveness and viability of proposed BSS framework as pre-processing to keyword spotting. It is observed that detection rate of keyword spotting framework is improved by applying BSS as pre-processing as compared to the framework without being pre-processed through BSS.

Variable Order Adaptation of LMS Lattice Predictors using Forward Residual Errors 837

Salem Alsaid (University of Windsor), Esam Abdel-Raheem (University of Windsor),

Khaled Mayyas (Jordan University of Science and Technology)

The filter tap-length is a significant structural parameter of adaptive filters that can influence both the complexity and steady-state performance characteristics of the filter. In direct form structure filtering, commonly known as a finite impulse response (FIR) adaptive filter, several schemes were used to estimate the optimum tap-length. Among existing algorithms, pseudo Fractional Tap-length (FT) algorithm is of particular interest because of its fast convergence rate and small steadystate error. Lattice structured adaptive filters, on the other hand, have attracted attention recently due to a number of desirable properties. In this paper a Fractional Order Lattice Predictor (FO-LP) algorithm is formulated using forward residual errors to update the lattice order at each iteration and hence obtain the structural optimum filter order adaptively.

Session C1L-B: Hardware and Cyber Security I

Chair: Yingjie Lao, *Clemson University*

Co-Chair: Rashmi Jha, *University of Cincinnati*

Time: Wednesday, August 8, 2018, 8:30 - 10:00

Location: Martis

Variation Enhancement of Arbiter PUFs with Asymmetric Layout 841

Yunxi Guo (Iowa State University), Timothy Dee (Iowa State University), Akhilesh Tyagi (Iowa State University)

Arbiter PUF (APUF) is a popular style of physical unclonable function (PUF) that has been used in many security applications. The amount of process variation of an APUF is an important parameter strongly influencing its resolution. Although various attempts have been made to increase APUFs' random variation from the circuit design prospective, little work has been done to enhance manufacturing mismatch through transistor-level layout. In this work, we propose a novel layout strategy for enlarging inner-die delay variation of an APUF circuit in an area neutral manner. The mechanism separates a pair of racing delay units by an appropriate distance. Corresponding variation enhancement is quantified according to Pelgrom's mismatch model. Cadence Monte Carlo sampling shows the proposed scheme improves delay variation of 0.13 um technology 128-stage APUFs with minimum transistor size by as much as 8% without significantly affecting the inter-die hamming distance.

Physically Unclonable Function based on Voltage Divider Arrays in Subthreshold Region 845

Aishwarya Bahudhanam Venkatasubramanian (University at Buffalo), Arindam Sanyal (University at Buffalo)

This paper proposes a novel architecture of a simple, low energy silicon physically unclonable function arrays based on large random variation of threshold voltage of MOSFET, operating in the subthreshold region. The proposed structure is a strong silicon PUF with 2^{60} challenge response pairs consuming an energy of 0.48pJ/bit. The PUF simulations are carried out in 65nm CMOS technology. It is found to have inter-HD value of 0.4982 and intra-HD value of 0.0225. It is suitable for building secure IoT devices.

Efficient PUF Error Correction through Response Weighting 849

Yuejiang Wen (Clemson University), Yingjie Lao (Clemson University)

Reliability is an important performance metric of physical unclonable function (PUF) based authentication. This paper proposes a novel methodology that incorporates error rates into PUF response error correction to improve the overall performance. The proposed method first obtains the PUF circuit parameters by using machine learning techniques, which are then used to estimate the corresponding error rates. Then, we assign PUF response bits with different degrees of error-tolerance, according to their estimated error rates. Response weighting algorithm is proposed to determine the optimal weight assignment for each PUF response bit, which is formulated as an integer optimization problem. Experimental results show that the proposed response weighting algorithm can reduce not only the false negative from 20.6% to 8.3% under a noisy environment, but also the false positive rate by 58% for a PUF-based authentication with 127-bit response and 13-bit error correction.

A Novel Framework to Introduce Hardware Trojan Monitors using Model Checking based

Counterexamples: Inspired by Game Theory 853

Syed Rafay Hasan (Tennessee Technological University), Charles A. Kamhoua (US Army Research Laboratory), Kevin A. Kwiat (CAESAR Group), Laurent Njilla (Air Force Research Laboratory)

Interest in hardware Trojan detection has grown tremendously over the last decade. Several methods for detecting hardware Trojan have been proposed. Due to enormity of possible Trojans, researchers believe that runtime detection is required as a last line of defense. However, to cater different types of hardware Trojans, several detection techniques should be concurrently applied. In this paper we propose a framework for optimizing runtime hardware Trojan detection monitors. We propose a formal verification approach to identify the vulnerable behavior of the hardware using the counterexamples generated by model checker. We devised a heuristic to understand the relationship between the counterexamples and required detection unit. To optimize the number of detection techniques, we leveraged Game Theoretic models to obtain a set of optimized design choices.

Modeling of Thermal Coupling and Temperature Sensor Circuit Design Considerations for

Hardware Trojan Detection 857

Mengting Yan (Northeastern University), Haoran Wei (Northeastern University), Marvin Onabajo (Northeastern University)

This paper describes the development of a model for the simulation of electrothermal coupling to detect malicious circuits with on-chip temperature sensors. The strategy is presented using the layout of a digital control logic block from an 8-bit conventional successive approximation register (SAR) analog-to-digital converter (ADC). A differential temperature sensor with a high sensitivity of 2.1V/degree Celsius was designed with 130nm CMOS technology. Joint simulation results of the circuit under test and temperature sensor indicate the potential for temperature-based hardware Trojan (HT) detection with on-chip resources.

Session C1L-C: Power

Chair: Narayan Kar, *University of Windsor*

Co-Chair: Maher Azzouz Abdekkhalek, *University of Windsor*

Time: Wednesday, August 8, 2018, 8:30 - 10:00

Location: Luna

An 8 A 100-MHz 4-Phase Buck Converter with Fast Dynamic Response and Enhanced Light-Load Efficiency 861
Manmeet Singh (Ohio State University / Dialog Semiconductor Inc.), Ayman Fayed (Ohio State University)

A 8-A 100-MHz 4-phase buck converter targeting server applications is presented. The converter uses 5 nH/phase inductor and 220 nF output capacitor; all co-packaged with the converter die. To maintain high efficiency across a wide load range, the converter employs PWM control with phase-shedding in the 0.7-8 A range, and PFM control for loads less than 0.7 A. The converter is designed and simulated in 0.13- μ m CMOS with 1.5 V input and 0.75–1 V output. The peak efficiency is 88% at 5 A and 79% at 0.7 A with less than 4 mV output voltage ripple.

An Improved Voltage Balancing Method for Grid Connected PV System based on MMC under Different Irradiance Conditions
Safia Babikir Bashir (Ajman University), Zulfiqar Ali Memon (Ajman University)

Modular Multilevel Converter (MMC) is considered as one of the most promising topologies for renewable energy application. The MMC has attractive features such as modular realization, scalability, and transformerless operation which makes it a suitable converter, especially for PV system. For the satisfactory operation of MMC, it is important to maintain balanced voltage across each sub-modules (SMs). This paper proposes an improved balancing approach based on Space Vector Pulse Width Modulation (SVPWM) for three-phase multi-string PV system based on MMC. The proposed method along with the control strategy uses only one SVPWM, which not only reduce the calculation but also balance the SM capacitor voltage, realize the independent MPPT of each PV string and reduce the circulating current. Thereby increases the efficiency of PV system. The proposed method is varied through simulation using Matlab/Simulink during different operating conduction

Application of Semi-Analytical Recursive Convolution Algorithms for Designing of Buck DC-DC Converter 869
Jacek Kaczmarek (Koszalin University of Technology), Robert Suszynski (Koszalin University of Technology)

Choosing the appropriate parameters of the transfer function of the digital control circuit of the DC-DC converter main block is especially important. This function can be obtained by first designing an analog prototype and then converse it into a discrete-time system by a sampled-data transformation. This paper discusses application semi-analytical recursive convolution algorithms to convert analog transfer function in discrete form. Three converter prototypes obtained using the Matched, Tustin and SARA transformation methods, are simulated, measured and the experimental results are presented to compare and verify the effectiveness of the approximated discrete-time model.

Session C2P-E: Circuits and Systems II

Chair: Mohsin M. Jamali, *The University of Texas of the Permian Basin*

Co-Chair: Ahmed Abdelgawad, *Central Michigan University*

Time: Wednesday, August 8, 2018, 8:30 - 10:00

Location: Poster Area

Vision and Infra-Red Sensor based Fire Fighting Robot 873
Shang Gao (University of Detroit Mercy), Zhiyang Zhang (University of Detroit Mercy), Zihan Zhao (Beijing University of Chemical Technology), Mohsin M. Jamali (University of Texas of the Permian Basin)

Fire-fighting robots are useful in situations where it is too dangerous or has difficult access for human. Modular design based on proximity, sensors has been incorporated into a fire-fighting model. The robot sprays water from manipulator to extinguish flame. Software consists of integrated tracking, obstacle avoidance, flame detection and motion algorithms. Through testing, it is possible to run in a realistic scene simulated in the lab and to detect and extinguishment the flame.

A Smoothed Latent Generalized Dirichlet Allocation Model in the Collapsed Space 877
Koffi Eddy Ihou (Concordia University), Nizar Bouguila (Concordia University)

Many LDA (latent Dirichlet Allocation)-based models often suffer from a large bias due to the variational Bayesian inference scheme with its strong independency assumption between latent variables and parameters. In addition, the quest for better approaches in many instances lead to very sophisticated models (nonparametric). As a result, in this paper, instead of a complex method, we propose a simple framework that only utilizes the collapsed Gibbs sampling inference technique coupled with the flexible GD (generalized Dirichlet) prior to obtain accurate estimations. Experimental results in image categorization show the merits of the new approach.

A Low-Memory Compressive Image Sensor Architecture for Embedded Object Recognition 881

Wissam Benjilali (Université Grenoble Alpes, CEA-Leti), William Guicquero (Université Grenoble Alpes, CEA-Leti), Laurent Jacques (Université Catholique de Louvain), Gilles Sicard (Université Grenoble Alpes, CEA-Leti)

This work presents a compact image sensor architecture with end-of-column digital processing dedicated to perform embedded object recognition. The architecture takes advantage of a Compressed Sensing (CS) scheme to extract compressed features and to reduce data dimensionality based on a low footprint pseudo random data mixing. Taking advantage of the intrinsic property of a first order incremental Sigma-Delta (Sigma Delta) Analog to Digital Converter (ADC), an optimized Digital Signal Processing (DSP) is proposed to implement the affine projection applied by a linear Support Vector Machine (SVM) classifier. This architecture allows to achieve an acceptable object recognition accuracy of 80% on the Georgia Tech face database (50 classes). On the other hand, the signal independent dimensionality reduction performed by our dedicated sensing scheme (1/512) allows to dramatically reduce memory requirements (125 kbits) related -in our case- to the ex-situ learned affine function of the linear SVM.

Performance Analysis of Single-Precision Floating-Point MAC for Deep Learning 885

Gunjan Jha (University of Texas at San Antonio), Eugene John (University of Texas at San Antonio)

Multiply and accumulate (MAC) units form the basic building blocks in several key areas such as DSP and deep learning. In deep learning, convolution accounts for more than 90% of overall computation, dominating the runtime and energy consumption of the system. These convolution operations are primarily performed using MACs. This paper analyzes the delay and power performances of single-precision Floating-Point MACs using four different multiplication algorithms, namely, Wallace Tree Reduction, Modified Booth Encoding (MBE), Combinational Array, and Add and Shift. The performances of the various implemented MACs are analyzed using TSMC 45nm and 90nm technology nodes.

New Trend in Video Foreground Detection using Deep Learning 889

Thangarajah Akilan (University of Windsor), Q.M. Jonathan Wu (University of Windsor), Wei Jiang (Zhejiang University), Amin Safaei (University of Windsor), Jie Huo (University of Windsor)

Video foreground (FG) detection is one of the primitive tasks in computer vision (CV). It is a core component in a myriad of video-based applications, like autonomous driving, activity recognition, and video surveillance. As in any other field, the deep learning (DL) has shown significant impact on video FG detection. Thus, this paper attempts to provide a fundamental study on the new strategies that harness the efficacy of deep convolutional neural networks (DCNNs) to extract video FG information. It also introduces two models and analyses their performances on various indoor and outdoor video sequences.

A Novel 1D Deep Convolutional Neural Network based Algorithm for Mixture Gases Recognition 893

Zhihuang Wen (Shenzhen University), Wenbin Ye (Shenzhen University), Xiaojin Zhao (Shenzhen University), Xiaofang Pan (Shenzhen University)

In this paper, we present a novel one-dimensional deep convolutional neural network (1D-DCNN) based algorithm for classifying mixture gases. Compared with the previously reported electronic nose system that can only recognize pure gas, the proposed implementation is capable of distinguishing the individual component of binary mixture gases composed of Ethylene, CO and Methane. To the best of our knowledge, the proposed 1D-DCNN algorithm is firstly applied in the mixture gases recognition. Compared with the conventional pattern recognition algorithms including support vector machine (SVM) and artificial neural network (ANN), the proposed 1D-DCNN exhibits higher average accuracy (96.15%) based on extensive experimental results using 10-fold cross validation.

Local Queueing-Based Data-Driven Task Scheduling for Multicore Systems 897

Meng Li (Polytechnique Montréal), Chao Chen (Polytechnique Montréal), Guchuan Zhu (Polytechnique Montréal), Yvon Savaria (Polytechnique Montréal)

Nowadays, multicore systems are widely used in high-performance computing. Many algorithms have been proposed to enhance the system performance by load balancing or concurrent scheduling to reduce the execution time of applications. However, task scheduling on multicore systems is still an open issue. In order to tackle the inefficient utilization of CPU cores, a queueing-based data-driven task scheduling scheme, which focuses on local parallel computing, is introduced in this paper. In this scheduling scheme, multi-queue management is proposed for dynamic task scheduling to target a full utilization of local CPU cores when input tasks can fulfill the CPU cores. Furthermore, the preemption technique is applied to guarantee that high priority tasks will not be blocked by low priority tasks. Our solution can be combined with other algorithms taking into account earliest finish time or critical path to generate better results. In this way, the utilization of CPU cores can be improved while guaranteeing the makespan of high priority DAGs. Finally, simulations are carried out to verify the proposed task scheduling scheme. The reported results confirm its viability and efficiency.

A 0.1-13 GHz Wide Range Multi-Modulus Divider with Adaptive Sensitivity for Broad Band Operation 901

Martin Kreißig (Technische Universität Dresden), Simon Buhr (Technische Universität Dresden), Mohammed El-Shennawy (Technische Universität Dresden), Frank Ellinger (Technische Universität Dresden)

This work presents a multi-modulus frequency divider (MMD) chain exhibiting a very wide continuous division ratio range of 8 to 8191. Furthermore the speed and input sensitivity can be adjusted while the power consumption is reduced for slower operation. Along a more than two decades covering frequency range from 0.1 GHz to 12.8 GHz the needed differential input voltage amplitude is less than 63 mV which is equivalent to -17 dBm at a 100Ω load. The power consumption varies between 12 mW and 43.2 mW according to the speed setting. The maximum operating input frequency is 13 GHz and the divider was implemented together with other phase locked loop (PLL) components in a low cost 180 nm BiCMOS process.

CMOS-RC Colpitts Oscillator Design using Floating Fractional-Order Inductance Simulator 905

Aslihan Kartci (Brno University of Technology), Norbert Herencsar (Brno University of Technology), Lubomir Brancik (Brno University of Technology), Khaled N. Salama (King Abdullah University of Science and Technology)

This paper deals with CMOS fractional-order inductance (FoL) simulator design and its utilization in 2.75th-order Colpitts oscillator providing high frequency of oscillation. The proposed floating FoL is composed of two unity-gain current followers (CF_{pm}), two inverting voltage buffers, a transconductor, and a fractional-order capacitor (FoC) of order 0.75, while the input intrinsic resistance of CF_{pm} is used as design parameter instead of passive resistor. The resulting equivalent inductance value of the FoL can be adjusted via order of FoC, which was emulated via 5th-order Foster II RC network and values optimized using modified least squares quadratic method. In frequency range 138 kHz – 2.45 MHz the L_γ shows ±5 degree phase angle deviation. Theoretical results are verified by SPICE simulations using TSMC 0.18 μm level-7 LO EPI SCN018 CMOS process parameters with ±1 V supply voltages.

Control of a Two-Dimensional Magnetic Positioning System with Deep Reinforcement Learning and Feedback Linearization 909

Eduardo Bejar (Pontifical Catholic University of Peru), Antonio Moran (Pontifical Catholic University of Peru)

This paper presents a neuro-controller based on deep reinforcement learning to control the nonlinear dynamics of a two-dimensional magnetic positioning system. The feedbacklinearized model of the magnetic positioning system is used to generate training data for the neuro-controller. The neurocontroller is trained using the Deep Deterministic Policy Gradient (DDPG) algorithm. The effectiveness of the proposed control strategy is verified with different desired setpoints and trajectories, and diverse working conditions.

Reduced-Size On-Wafer Inductors using Slow Wave Techniques 913

Ahmad Eldahshan (Carleton University), William Knisely (Carleton University), Rony Amaya (Carleton University), Calvin Plett (Carleton University)

This paper introduces a study on miniaturizing on-chip RF inductors using the Slow Wave Transmission Lines (SWTL) technique. The slow wave factor (SWF) of different transmission lines are calculated, verified and simulated. The lines are treated as a two port networks where their S-parameters and ABCD parameters are extracted, from which their self inductance are determined. The simulated results show that for a constant inductance, characteristic impedance and electrical length, the reduction in the line length can reach 73%. The idea was validated practically by implementing different SWTLs using CMOS 130nm process. The measured and simulated lines are compared and the results shows that they are matched to a great extent, however, less reduction of length was achieved because of the constraints imposed by fabrication rules.

Novel CMOS Active Inductor for Tunable RF Circuits 917

Abdelhalim Slimane (Centre de Développement des Technologies Avancées), Sid Ahmed Tedjini (Centre de Développement des Technologies Avancées), Fayrouz Haddad (IM2NP / Aix-Marseille Université)

Future wireless transceivers must support several communication standards with low-cost, low-area and low power consumption. In this letter, a novel wide tunable CMOS active inductor dedicated to RF circuits for multistandard applications is presented. Only negative transconductors are considered in the proposed gyrator instead of the conventional one. To save the silicon area, the new active inductor is implemented employing push-pull amplifier cells as negative transconductors. Using a 0.13-um CMOS technology, the obtained simulation results show a wide frequency range inductive behavior with high self resonance frequency. High quality factors are reached with good agility while covering the frequency range of 2 to 2.6 GHz and consuming a dc power of 0.9 to 1.3 mW from 1 V of supply voltage.

Optimization of Machine Learning Guided Optical Proximity Correction 921

Joonhyuk Cho (KAIST), Gangmin Cho (KAIST), Youngsoo Shin (KAIST)

Machine learning guided optical proximity correction (ML-OPC) has been proposed to replace computation extensive model-based OPC (MB-OPC) or to provide a good initial OPC solution to work with. Two keys of ML-OPC are the representation of layout segment to be corrected, and the choice and optimization of regressors (or classifiers). We propose polar Fourier transform (PFT) signals with initial edge placement error (EPE) as a set of parameters for representation, and random forest regressor (RFR) as our choice of machine learning algorithm. Experimental results demonstrate a significant reduction in root mean square (RMS) error in mask bias prediction compared to state-of-the-art ML-OPC approach: reduction from 1.45nm to 0.66nm.

FPGA Implementation of High Accuracy Automatic Epileptic Seizure Detection System 925

Hisham G. Daoud (University of Louisiana at Lafayette), Ahmed M. Abdelhameed (University of Louisiana at Lafayette), Magdy Bayoumi (University of Louisiana at Lafayette)

Analysis of Electroencephalogram (EEG) records acquired from the brain is considered the easiest and a powerful tool in diagnosis the neurological disorders that are related to the electrical activities of the brain like epilepsy. In this paper, we propose a novel approach to extract the most relevant features to epilepsy disease and use them to do classification process that yields fast and accurate automatic diagnosis. Hilbert Transform of EEG signals is calculated and mean power frequency is applied to reduce the feature vector dimensions. The classification process between normal and seizure cases is done using Multilayer Perceptron Artificial Neural Network. The classification accuracy achieved using this method is 100%. FPGA implementation of the proposed system is done for real-time analysis. High accuracy of the proposed system, power efficiency and its light weight make it a good candidate for automatic epileptic seizure detection.

Current Controlled Neuro-Fuzzy Membership Function Generation 929

Anuar Dorzhigulov (Nazarbayev University), Bhaskar Choubey (Oxford University), Alex Pappachen James (Nazarbayev University)

Neuro-fuzzy systems are encouraging new approaches to mimic human-like decision making in presence of the vagueness and imprecision in the input data. However, majority of current implementations of these systems are limited to small-scale software designs, ignoring the potential advantages of the analogue hardware. This paper presents a completely tunable membership function generator, which is a vital part of designing neuro-fuzzy systems. Designed using a 130nm CMOS process, this circuit provides the ability to modify the shape as well as the mid-point of a widely used bell-shaped membership function. The circuit uses 11 transistors and provides this control of the membership function with an area of 0.9 μm^2 and power consumption of 12 μW . More importantly, only three control voltages are used without the need of any external digital control. Extensive simulation results are presented to verify the circuit.

Peak-to-Average Power Ratio Suppression using Companding Schemes in OFDM Systems 933

Abdulwahid Mohammed (Cairo University), Mohamed Shehata (Cairo University), Hassan Mostafa (Cairo University / Zewail City for Science and Technology), Amin Nassar (Cairo University)

The reduction of the high signal peak-to-average-power-ratio (PAPR) in orthogonal frequency division multiplexing (OFDM) systems limits the clipping-induced non-linear harmonic distortions caused by power amplifiers. In this paper, the characteristics of the circuits implemented in subthreshold CMOS are employed to perform companding-based PAPR reduction for OFDM signals. Simulation results confirm that the tanh-companding amplifiers are capable of reducing the PAPR of OFDM signals through the careful control of their design parameters.

A Compact Dual-Band Impedance Matching Network based on All-Pass Coupled Lines 937

Deepayan Banerjee (University of Calgary / Indraprastha Institute of Information Technology, Delhi), Antra Saxena (University of Calgary / Indraprastha Institute of Information Technology, Delhi), Mohammad Hashmi (Nazarbayev University / Indraprastha Institute of Information Technology, Delhi), Fadhel Ghannouchi (University of Calgary)

This paper proposes the design of a compact dual-frequency impedance matching network that matches frequency dependent complex loads at two distinct frequencies with a real source. The design utilizes two coupled lines in their all-pass configuration. The same helps in flexibility of the frequency ratios of operation. As an example, a prototype operating at the Bluetooth and WiFi frequencies of 2.4 and 5.8 GHz respectively, has been fabricated. The measured results are in good agreement with the simulated ones.

CANNoC: An Open-Source NoC Architecture for ECU Consolidation

Vipin Kizheppatt (Nazarbayev University)

Modern cars contain more than 50 electronic control units (ECUs) whose number is expected to grow as more and more features are incorporated. The concept of one feature per ECU is contributing to this growth which increases the car kerb weight leading to lower fuel efficiency. ECU consolidation addresses this issue by combining multiple ECUs on the same chip. This paper investigates a network on chip (NoC) architecture which enables integrating multiple ECUs on a reconfigurable chip (FPGA) and interfacing it with a standard CAN network. The architecture enables reducing the number of ECUs required for non-critical functions and lower communication overhead to the main bus

Variable Latency Division 944

Peter-Michael Seidel (University of Hawai'i at Manoa)

We propose a variable-latency implementation of iterative, subtractive division, where the partial remainder is encoded in a signed-digit representation. Digit selection is implemented for the redundant partial remainder representation based on a combination of leading-zero prediction, binary shifting and sign-detection. The implementation target a low-power implementation and can be scaled to higher radices.

On the Use of Probabilistic Parallel Bit-Flipping Decoder for the Storage Systems 948

Khoa Le (Universit'e Paris Seine, Universit'e de Cergy-Pontoise), Fakhreddine Ghaffari (Universit'e Paris Seine, Universit'e de Cergy-Pontoise), David Declercq (Universit'e Paris Seine, Universit'e de Cergy-Pontoise)

The soft-decision Low-Density Parity-Check (LDPC) decoders have been applied in several storage systems thanks to their powerful error correction capability. However, these systems may suffer a long read latency since the softdecision decoders require an intensive computations as well as a long sensing time for the soft-information to decode. In this paper, we modify the recent-introduced Probabilistic Parallel Bit-Flipping (PPBF) LDPC decoder, to use on the storage systems in replacing the soft decision decoders, to improve the memory reading speed. The modified decoder is named Non-Syndrome Probabilistic Parallel Bit-Flipping (NS-PPBF). A special flipping mechanism is introduced such that the decoder can stop flipping without requiring the syndrome check results, which helps significantly improve the decoding frequency. We provide also the hardware architecture to implement NS-PPBF on the LDPC code used on the memory systems, which are usually very long block length with very high rate. The advantages of using PPBF decoder in terms of error correction and decoding throughput are confirmed by the simulating decoding performance and the hardware synthesis.

Session C3L-A: Digital Filter Design

Chair: Hon Keung Kwan, *University of Windsor*

Co-Chair: Arash Ahmadi, *University of Windsor*

Time: Wednesday, August 8, 2018, 13:30 - 15:00

Location: Mercuri

Sparse FIR Filter Design using Iterative MOCSA 952

Hon Keung Kwan (University of Windsor), Jiajun Liang (University of Windsor), Aimin Jiang (Hohai University)

In this paper, sparse FIR digital filter design using iterative multiobjective cuckoo search algorithm (MOCSA) is presented. The least-squares frequency response error and the l_1 -norm of selected non-zero filter coefficients of a sparse digital filter are jointly minimized by iterative multiobjective cuckoo search algorithm until convergence. After convergence, a final round of single-objective cuckoo search is performed to minimize the least-square frequency response error of the sparse digital filter to arrive at an optimal solution. The sparse digital filter design results obtained by the iterative MOCSA compares favorably with the obtained results of another optimization method.

Sparse FIR Filter Design using Artificial Bee Colony Algorithm 956

Rija Raju (University of Windsor), Hon Keung Kwan (University of Windsor), Aimin Jiang (Hohai University)

In this paper, sparse linear-phase FIR digital filters are designed using artificial bee colony (ABC) algorithm. Sparse digital filters can be used in applications where computational cost and complexities are of concern as zero-valued coefficients eliminate multiplications required for implementation. In this method, sparse digital filters are designed using minimax optimization by ABC algorithm and successive elimination. In contrast to methods which minimize insignificant coefficient values, this method eliminates insignificant coefficients by setting them to zero. The sparse linear-phase FIR filters designed using ABC algorithm are compared to the partial l_1 -norm optimization design, the minimum increase design, and the smallest coefficient design to illustrate the effectiveness of each design method.

Designing Low-Delay Maximally Flat Integer-Order FIR Digital Differentiators with Equiripple Stopband 960

Takahiro Fujikawa (Tokyo University of Science), Ryosuke Kunii (Tokyo University of Science), Naoyuki Aikawa (Tokyo University of Science)

In this paper, we propose a method for designing a low-delay low-pass/band-pass maximally flat integer-order differentiators in passband based on flatness characteristics and in stopband based on equiripple characteristics. The proposed function consists of two functions. One of functions has low-delay and flat characteristics in the passband. The other gives the whole function equiripple characteristics in the stopband. The low-delay low-pass/band-pass integer-order differentiators designed by the proposed method realizes highly accurate differential estimation near the desired frequency and sharp cutoff characteristics.

Analytical Design of Elliptically-Shaped 2D Recursive Filters 964

Radu Matei (Gheorghe Asachi Technical University of Iași)

This paper presents an analytic design technique for 2D IIR filters with elliptical symmetry, which have useful applications in image processing. The design is based on efficient elliptic digital filters, regarded as 1D prototypes, to which specific complex frequency transformations are applied; this allows to obtain directly a factored form of the transfer function for the 2D elliptically-shaped filter. The design procedure uses some accurate approximations, but no global optimization algorithm. Finally the 2D filter matrices are obtained. The filter is adjustable in the sense that its coefficients depend explicitly on specified orientation and bandwidth. Another advantage is versatility, since the design need not be resumed each time from the start for various specifications. The designed 2D filters have an accurate elliptical shape with low distortions even close to the margins of frequency plane and are efficient, of high selectivity and relatively low order.

Session C3L-B: Hardware and Cyber Security II

Chair: Shantanu Chakrabarty, *Washington University in St. Louis*

Co-Chair: Yingjie Lao, *Clemson University*

Time: Wednesday, August 8, 2018, 13:30 - 15:00

Location: Martis

Self-Powered Sensing and Time-Stamping of Tampering Events 968

Darshit Mehta (Washington University in St. Louis), Liang Zhou (Washington University in St. Louis), Kenji Aono (Washington University in St. Louis), Shantanu Chakrabarty (Washington University in St. Louis)

While many techniques exist for detecting mechanical tampering in an integrated circuit supply-chain, estimating the time-of-occurrence of the tampering event has proven to be challenging. This work builds upon our previously demonstrated self-powered mechanical event detector and self-powered timing device to report a chip-scale system that can accurately timestamp the occurrence of the tampering event. The proposed system uses a combination of Fowler-Nordheim tunneling for continuous time-keeping and a linear hot-electron injector for sensing and recording of mechanical events. Using devices fabricated in a 0.5 μm standard CMOS process, we demonstrate event time-stamping with an accuracy of 95% over a duration of 3 days. This accuracy can be further improved by incorporating a parametric model during the system calibration phase.

Hardware Trojan based Security Issues in Home Area Network: A Testbed Setup 972

Hawzhin Mohammed (Tennessee Technological University), Jimmy Howell (Southern Illinois University), Syed Rafay Hasan (Tennessee Technological University), Nan Guo (Tennessee Technological University), Faiq Khalid (Vienna University of Technology), Omar Elkeelany (Tennessee Technological University)

Advanced Metering Infrastructure (AMI) is the main player in today's Smart Grid, and Home Area Network (HAN) is an important subsystem in AMI. HAN connects the smart home appliances (SHA) inside the home to the smart meter (SM), which is connected to the power utility company. From the last decade, hardware Trojans (HT), have been extensively studied in both academia and industry. Consequently, the vulnerability of integrated circuits (ICs) against HTs leads to the potential security threat to any system that contains ICs, and HAN is no exception. However, to the best of authors knowledge, the potential effect of HTs on HAN has not been studied in the literature so far. In this paper, we are investigating HT in HAN network. In the process, we developed a testbed which can be scalable up to 127 nodes using I2C interface to control and implement any kind of required network behavior. We introduced three possible scenarios of HTs in this HAN network testbed. These scenarios illustrate the manifestation of HTs in the HAN that leads to network performance degradation.

Adaptive and Dynamic Device Authentication using Lorenz Chaotic Systems 976

Lake Bu (Boston University), Hai Cheng (Boston University), Michel A. Kinsy (Boston University)

Chaotic systems such as Lorenz functions have been proposed as cryptographic primitives for its divergence attribution. They are mostly used to generate random numbers, assist key agreements, and especially facilitate encryption processes. However in those applications, there are two important gaps in the use of chaotic functions: 1) their convergence attribution is seldom used; 2) their core secret - the system parameters, are statically fixed, which leads to potential vulnerabilities. Through filling the gaps, we have found certain interesting properties of the Lorenz chaotic systems. In this paper we propose an adaptive and dynamic authentication protocol based on discrete Lorenz chaotic systems. This protocol leverages both Lorenz function's divergence and convergence attributions in authentication, which makes it hard to track by attackers, but easy to verify by authenticators. This protocol also proposes in a novel way a dynamic configuration of the Lorenz functions' system parameters, so that the security of the protocol is further enhanced.

Hardware Design of Chaotic Pseudo-Random Number Generator based on Nonlinear Feedback Shift Register 980

Maryam Hematti (Razi University), Arash Ahmadi (University of Windsor), Seyed Vahab Makki (Razi University), Majid Ahmadi (University of Windsor)

Generating pseudo-random sequence is an essential component of security and encryption tasks. Full-length sequences with large period, high output complexity is one of the most important requirements for the security and encryption applications. Different structures and various components are used in random number generators, include most notably, linear feedback shift register, non-linear feedback shift register, and pseudo-random chaos generators. In this paper by review and compare the features of each structure, a new design consists of non-linear feedback shift register and pseudo-random chaos generator is presented generating random numbers with high output quality. Output signal is noise-like and shows a good autocorrelation function and looks like a δ -function. Presented design has an appropriate random characteristic and with improvements compared with previous works.

Optimization of a Quantum-Secure Sponge-Based Hash Message Authentication Protocol	984
<i>M. Kamran Latif (Boise State University), H.S. Jacinto (Boise State University), Luka Daoud (Boise State University), Nader Rafla (Boise State University)</i>	

Hash message authentication is a fundamental building block of many networking security protocols such as SSL, TLS, FTP, and even HTTPS. The sponge-based SHA-3 hashing algorithm is the most recently developed hashing function as a result of a NIST competition to find a new hashing standard after SHA-1 and SHA-2 were found to have collisions, and thus were considered broken. We used Xilinx High-Level Synthesis to develop an optimized and pipelined version of the post-quantum-secure SHA-3 hash message authentication code (HMAC) which is capable of computing a HMAC every 280 clock-cycles with an overall throughput of 604 Mbps. We cover the general security of sponge functions in both a classical and quantum computing standpoint for hash functions, and offer a general architecture for HMAC computation when sponge functions are used.

Session C3L-C: Advancing Internet of Vehicles and Internet of Things

Chair: Ahmed Abdelgawad, *Central Michigan University*

Co-Chair: Shantanu Chakrabartty, *Washington University in St. Louis*

Time: Wednesday, August 8, 2018, 13:30 - 15:00

Location: Luna

Improved RPL for IoT Applications	988
<i>Md Anam Mahmud (Central Michigan University), Ahmed Abdelgawad (Central Michigan University), Kumar Yelamarthi (Central Michigan University)</i>	

Routing is very important for the overall performance of Internet of Things (IoT), which is known as the global network of smart objects. A smart object has a power source, a processing unit, sensors, and a radio module encompassed within. Since the vision of IoT is that everything (smart object) would be connected to the internet, the system would have to deal with low power and lossy networks (LLNs). To address the unpredictability of LLNs, Internet Engineering Task Force (IETF) standardized routing protocol for LLNs (RPL). Due to the overlap between the applications of LLNs and IoT, RPL is becoming the routing protocol for IoT, gradually. However, RPL struggles to provide desirable performance regarding energy-efficiency and reliability simultaneously. This paper focused towards obtaining decent links for information routing, and providing optimal transmission power while ensuring energy-efficiency. First, minimum rank with hysteresis objective function (MRHOF) was used and improved by proposing better parent switching hysteresis value to obtain a better link regarding received signal strength indicator (RSSI).

Quasi-Digital Output Low Power CMOS Temperature Sensor	992
<i>Ava Hedayatipour (University of Tennessee), Mohammad Aminul Haque (University of Tennessee), Nicole McFarlane (University of Tennessee)</i>	

Embedded systems, such as IoT devices, benefit from low power sensors. We propose a fully-integrated proportional to frequency temperature sensing system. The temperature sensor replaces power hungry ADCs and on-chip time references with a frequency dependent digital output. The system consumes 195 nW, with 0.5 V power supply. The maximum temperature accuracy of 0.2 C is achieved across 0C to 50C in a total area of 0.008 mm² in 130 nm technology. Experimental measurements of the temperature to voltage circuit is demonstrated, and post layout and Monte Carlo simulations verify the total system design meets performance requirements and is suitable for arrayed applications.

Gaussian Process Regression for Improving the Performance of Self-Powered Time-of-Occurrence Sensors	996
<i>Liang Zhou (Washington University in St. Louis), Kenji Aono (Washington University in St. Louis), Shantanu Chakrabartty (Washington University in St. Louis)</i>	

In our previous work, we had demonstrated a CMOS timer-injector integrated circuit for self-powered sensing of time-of-occurrence of mechanical events. While the sensor could achieve an improved time-stamping accuracy by averaging the output across over multiple channels, the mismatch between the channels made the calibration process cumbersome and time-consuming. In this paper, we propose the use of non-parametric machine learning techniques to achieve more robust and accurate event reconstruction. This is demonstrated using training and testing data that were obtained from fabricated prototypes on a 0.5- μ m CMOS process; the model trained using Gaussian process regression can achieve an average recovery accuracy of 3.3% on testing data, which is comparable to the performance of using an averaging technique on calibrated injection results. The experimental results also validate that scalable performance can be achieved by employing more injection channels.

Hybrid-Powered Internet-of-Things for Infrastructure-to-Vehicle Communication	1000
<i>Sri Harsha Kondapalli (Washington University in St. Louis), Owen Pochettino (Washington University in St. Louis), Kenji Aono (Washington University in St. Louis), Shantanu Chakrabarty (Washington University in St. Louis)</i>	

While autonomous and networked vehicles are being designed to navigate under different driving conditions, there is an emerging need for the infrastructure (roadways) to communicate with the vehicles so as to reliably convey current road conditions. Wireless sensors or devices that are embedded inside the infrastructure can facilitate real-time information exchange, however, its design requires a careful trade-offs between different factors such as operational lifetime, communication distance and latency. In this paper, we discuss three particular methods for establishing a radio-frequency communication link within our previously reported framework of infrastructural Internet-of-Things (i-IoT). We propose a figure of merit (FOM) to compare and contrast different topologies of infrastructure-to-vehicle (I2V) communication devices which includes the traditional battery-powered approach, a passive approach that harvests RF energy for its power source and only polls a sensor when power is available, and a hybrid approach that leverages an RF harvesting mechanism to activate a battery-powered sensor.

Platform for Autonomous Sensor Characterization and Generation of Provenance-Aware Datasets	1004
<i>Yousef Gtat (Michigan State University), Sina Parsnejad (Michigan State University), Andrew J. Mason (Michigan State University)</i>	

Sensor characterization can be laborious, prone to human error, difficult to repeat precisely, and can produce data that are challenging to interpret. To address these challenges, a new platform for digitally designing measurement recipes, automating data acquisition, and analyzing resulting datasets is presented. This flexible platform is capable of managing a large set of diverse instruments, measurement recipes and characterization datasets. By employing several design abstractions, the platform allows users to design, schedule and execute sensor characterization experiments while archiving results along with their measurement recipes and preserving the provenance of the datasets. The platform eliminates manual errors and human omissions, and permits reliable repeatability. An electrochemical sensor experiment was performed to validate the platform's capability to design and capture a digital record of the measurement recipe, automate real-time data acquisition, and view/analyze results.

Session C4P-E: Power Management and Hardware Security

Chair: Eugene John, *The University of Texas at San Antonio*

Co-Chair: Yingjie Lao, *Clemson University*

Time: Wednesday, August 8, 2018, 13:30 - 15:00

Location: Poster Area

Reliability of Physical Unclonable Function under Temperature and Supply Voltage Variations	1008
<i>Manpreet Kaur (University of Windsor), Rashid Rashidzadeh (University of Windsor), Roberto Muscedere (University of Windsor)</i>	

Physically Unclonable Function (PUF) has emerged as a cost-effective building block for crypto cores and security system. The unique signature of a PUF is primarily attributed to the process variations where the effects of other factors such as supply voltage, temperature and aging are considered to be minor. In this work, detail analysis to evaluate supply voltage and temperature effects on PUF reliability is presented. It is shown that the effects of supply voltage and temperature variations on PUF reliability can be comparable to the effects of process variations. It is also shown how temperature variation affects propagation delay of logic cells and consequently undermines PUF reliability. Simulation results using CMOS 0.18 μ m technology in Cadence environment with \pm 10% power supply variations for a temperature range of -40C to +70C indicate that these effects can reduce PUF reliability by more than 26%.

Evaluation of Four Power Gating Schemes Applied to ECRL Adiabatic Logic	1012
<i>William Morell (Louisiana State University), Ashok Srivastava (Louisiana State University)</i>	

In this paper, we evaluate four different power-clock gating schemes for use with four-phase adiabatic logic. Specifically, single buffer/inverter structures implemented in efficient charge recovery logic (ECRL) were used to generate the simulation data. Separate header and footer power-gating schemes were considered as well as standard digital control signals and pulsed adiabatic logic style control signals. All simulation data was generated using Tanner's T-SPICE software and 180nm CMOS technology.

Design of a Reconfigurable Chaos Gate with Enhanced Functionality Space in 65nm CMOS	1016
<i>Aysha S. Shanta (University of Tennessee), Md Badruddoja Majumder (University of Tennessee), Md Sakib Hasan (University of Tennessee), Mesbah Uddin (University of Tennessee), Garrett S. Rose (University of Tennessee)</i>	

In this paper, a three transistor circuit has been implemented in a standard 65 nm CMOS technology. The circuit has been used as a map to generate discrete-time chaotic signals. The map circuit has been combined with another map circuit in order to build a chaotic generator. The circuit is compact since it uses only twelve transistors in total to generate different Boolean functions as part of a chaotic computer. The total power consumption of the chaotic generator is only 18.4 μ W and the area is 0.556 μ m². The circuit can be used as a logic gate and has been designed to generate various functions using multiple configurations. The number of functionalities of the chaos gate has been increased by altering the bias and threshold voltages.

Effective Parameters for Ferrite-Core RFID Tag Antennas 1020

J. Santana-Abril (University of Las Palmas de Gran Canaria), Y. Elejalde (University of Las Palmas de Gran Canaria), J.M. Monzón-Verona (University of Las Palmas de Gran Canaria), J. Sosa (University of Las Palmas de Gran Canaria), Juan A. Montiel-Nelson (University of Las Palmas de Gran Canaria)

This paper introduces the analysis of effective parameters for computing, numerically, the self-inductance, mutual inductance and power losses of ferrite core-based antenna coils. Power losses include hysteresis effects. The ferrite coil is the receiver antenna of a low frequency RFID tag (134.2 kHz). Non-linear effects are modeled by adjusting the hysteresis angle and effective radius of the ferrite coil. The model has been validated with experimental measurements of S11 scattering parameter and induced current.

Is Economic Feasibility of BESS Energy Price Arbitrage Jurisdiction Dependent? 1024

Abdeslem Kadri (Ryerson University), Kaamran Raahemifar (Ryerson University)

Energy storage systems can be employed in power grids to gain benefits on both economical and technical sides. In this paper, the profit of energy arbitrage for an energy storage battery system with PV is optimized. The study compares the net profit of energy arbitrage for an existing battery system in three different energy markets. The results demonstrate that economic feasibility of energy arbitrage is market dependent based on spot price variation and local regulations.

Economical Smart Home Scheduling by Cuckoo Search Optimization via Levy Flight

Rujie Lai (Waseda University / Shanghai Jiao Tong University), Yangyizhou Wang (Waseda University), Cong Hao (Waseda University), Takeshi Yoshimura (Waseda University)

Smart home scheduling is an effective technique in Demand Side Management(DSM). In this paper, we intended to formulate an efficient algorithm to schedule smart home appliances to minimize the monetary cost of electricity as possible. Discrete power levels for appliances and quadric pricing model are adopted in this work. The proposed algorithm consists of two parts, with cuckoo search via Levy flight searching for real-number solutions as relaxed forms, and branch and bound method mapping relaxed forms to discrete power level values. Simulation results show that our algorithm outperforms the previous work in monetary cost within similar execution time.

Using Static Hardware Wrappers to Thwart Hardware Trojans and Code Bugs at Runtime 1034

Juan Portillo (University of Texas at San Antonio), Eugene John (University of Texas at San Antonio)

In the modern information age, security is a basic requirement. In this paper, we address security vulnerabilities due to code bugs and hardware Trojans. Some vulnerabilities can be detected during design and test but not during runtime. To this end, we propose a static, stand-alone hardware wrapper that is independent of the attack mechanism. The wrapper is integrated at the register transfer level (RTL) during the pre-silicon stage of integrated circuit (IC) design. The wrapper will not remove or detect these vulnerabilities, but, it can enforce correct behavior by assuming control of external signals during run-time.

Novel MOSFET Operation for Detection of Recycled Integrated Circuits 1038

Alexandros Dimopoulos (University of Victoria), Mihai Sima (University of Victoria), Stephen W. Neville (University of Victoria)

Recycled counterfeit integrated circuits (ICs) pose an important threat to the reliability of critical systems. The problem is poised to spread as the internet of things takes. Developing cheap, fast, and reliable testing to find these counterfeits is imperative. A compact embedded sensor designed to exploit the aging effects of hot carrier injection (HCI) could meet this goal. We have found that a matched pair of nMOSFETs biased to amplify HCI degradation should be able to detect a 6-month-old IC built in a 65 nm technology.

New Design for Solar Panel Tracking System based on Solar Calculations 1042

Zuhal ER (Istanbul Technical University), Selen Marangozogl (Istanbul Technical University)

In order to obtain optimal yield, angle of incidence must be perpendicular the surface. The motivation of this study is to design a solar tracking system. To move a panel through the direction of the Sun, it is crucial to define angles, caused by geometry of the Sun. This paper aimed, with new approach, the tracker design was made using by a controller. The new approach is design without any sensor to the determining of Sun's position. The calculations and the codes will be mentioned one by one in this study. The results are acceptable as expected for the location.

Wireless Power Transfer System for 3-D Stacked Multiple Receivers Switching Between Single and Dual Frequency Modes 1046

Shusuke Yanagawa (Keio University), Ryota Shimizu (Keio University), Mototsugu Hamada (Keio University), Tadahiro Kuroda (Keio University)

This paper proposes a wireless power transfer system which switches between a single frequency mode and a dual frequency mode for 3-D stacked multiple receivers. The power transfer function is analytically formulated in each mode and an optimization methodology of tuning capacitor values is proposed in both modes. A operation scenario switching between two modes is presented and compared with the non-switching mode in terms of the power transfer efficiency. The average power transfer efficiency in the proposed mode is 9.5% higher than the conventional mode.

Correlation-Based Cryptanalysis of a Ring Oscillator based Random Number Generator 1050

Burak Acar (TÜBİTAK), Salih Ergün (TÜBİTAK)

Random Number Generators (RNGs) are crucial for many security applications for generating unpredictable bit streams. Fully digital Random Number Generators which are implemented in FPGA platforms are usually preferred for their high speed convenience and easy integration to digital platforms. On the other hand, attention should be paid while placing and routing ring oscillators as much as possible. This paper presents implementation of a Random Number Generator based on ring oscillators on FPGA and cryptanalysis of it via correlation analysis. The main aim of this paper is to analyze the correlation between RNG and the attack circuit when coupled to the main circuit. In the main RNG circuit all ring oscillators are placed separately to obtain independent random bit streams at the output. Experimental results show that effective correlation between RNG and attack circuit can be obtained due to coupling.

Session C5L-A: Communication Systems

Chair: Yvon Savaria, *Polytechnic Montreal*

Time: Wednesday, August 8, 2018, 15:30 - 17:00

Location: Mercuri

Extending a CPU Cache for Efficient IPv6 Lookup 1054

Benjamin Wolff (Polytechnique Montréal), Bachir Fradj (Polytechnique Montréal), Normand Bélanger (Polytechnique Montréal), Yvon Savaria (Polytechnique Montréal)

Increasing throughput requirements for Internet routers and growing routing table sizes have emphasized the need for fast and scalable packet forwarding systems. This paper presents a hardware cache-based IPv6 lookup system. Our goal is to study how much performance can be achieved with a lookup system that is implemented by modifying a processor cache. We show by prototyping our system on an FPGA board that our solution provides efficient IPv6 packet forwarding. In particular, hardware complexity grows only linearly with table size. Also, our basic FPGA implementation can support a 1Gb link for minimum sized packets, while an improved implementation could improve this throughput by an order of magnitude. Finally, an ASIC implementation would support 100Gb of bandwidth if there were no other bottleneck in the system.

A Temperature Analysis for NFC-Powered Smart Lab-on-Chip Devices 1058

Carolin Kollegger (Infineon Technologies Austria AG), Christoph Steffan (Infineon Technologies Austria AG), Philipp Greiner (Infineon Technologies Austria AG), Clemens Rabl (Infineon Technologies Austria AG), David Lugitsch (Infineon Technologies Austria AG), Gerald Holweg (Infineon Technologies Austria AG), Bernd Deutschmann (Graz University of Technology)

This paper presents a temperature analysis for NFC-powered Lab-on-Chip (LoC) solutions. It is based on a monolithically implemented LoC and uses a 130 nm standard CMOS process. An application-independent temperature gathering mesh is implemented on the chip substrate. It allows a real time NFC-caused temperature analysis. Measurement data regarding heat spreading, the influence of the glob top, and the effect of the PCB layout is presented. A warming reduction from 23.05°C to 3.8°C using the same power source is achieved. Detailed data on the temperature gradient over time for warming and cooling is also provided.

Datapath Integrated Mapping in BTS Interconnects 1062

Avinash Raikwar (LSI Corporation), Amit Kumar Mishra (University of Cape Town)

One of the important upcoming and futuristic requirement noticed from radio interface specifications is the need of performing datapath processing on the mapped samples. The integration of datapath processing needs special circuitry to take care of the delays in the mapping. This paper presents a scalable architecture to efficiently integrate the datapath processing with mapping logic of data link layer in a radio interface.

Realization of All-Optical Sequential Circuit using Mach Zehnder Interferometer 1066

Umesh Kumar (Indian Institute of Technology Delhi)

In This Paper, Realization of Inverter Latch Is Proposed Through an All-Optical Cascadable Tri-State Buffer As a Sequential Circuit Which Is Designed with Mach-Zehnder Interferometer (MZI). This Sequential Circuit Is Assembled Based on Electro-Optic Effect and Is Verified by Simulation. The Applications of Tri-State Buffer for Optical Data Transfer and the Advantage of Using This Circuit As an Octal Tri State Buffer Over the Currently Existing ICs Has Been Explained.

Session C5L-B: Reconfigurable Architecture

Chair: Mohammed Khalid, *University of Windsor*

Time: Wednesday, August 8, 2018, 15:30 - 17:00

Location: Martis

Acceleration of k-Nearest Neighbor Algorithm on FPGA using Intel SDK for OpenCL 1070
Liyuan Liu (University of Windsor), Mohammed A.S. Khalid (University of Windsor)

In recent years, a new CAD tool called Intel FPGA SDK for OpenCL allowed fast and efficient design of FPGA-based hardware accelerators from high level specification such as OpenCL. In this paper, IFSO is used to explore acceleration of k-Nearest-Neighbor (kNN) algorithm using FPGAs. The optimized algorithm was implemented on two different FPGAs (Intel Stratix A7 and Intel Arria 10 GX). Experimental results show that the FPGA-based accelerators provided up to 80X speedup and 83% reduction in power consumption than a traditional workstation based on two Intel Xeon processors E5-2620 Series (each with 6 cores and running at 2.4 GHz).

Fly-Inspired Edge Detection: Architecture and Reconfigurable Embedded Implementation 1074
Oluwakemi N. Adabonyan (Oakland University), Daniel Llamocca (Oakland University), Brian K. Dean (Oakland University)

This work presents a reconfigurable embedded implementation of a fly-inspired edge detection algorithm that allows for run-time alteration of the numerical format in response to constraints on accuracy or resources. The low-resource, high-performance system can effectively detect edge orientation and location. This work illustrates the advantages of run-time reconfiguration technology for the implementation of fly-inspired vision algorithms whose capabilities can surpass or supplement traditional image processing systems.

Autonomous Vision-Based Target Detection using Unmanned Aerial Vehicle 1078
Jeff Deeds (Bradley University), Zach Engstrom (Bradley University), Caleb Gill (Bradley University), Zack Wood (Bradley University), Jing Wang (Bradley University), In Soo Ahn (Bradley University), Yufeng Lu (Bradley University)

In this paper, a vision-based target detection system using an Unmanned Aerial Vehicle (UAV) is developed to execute a mission plan. The mission plan is to autonomously take off to a specified altitude, fly to a waypoint with a predefined GPS coordinate, locate the target displayed by an AprilTag, hover above the target, then descend and land near the target. Our result shows that AprilTag is highly viable in UAV vision-based target detection.

Real-Time Bitstream Decompression Scheme for FPGAs Reconfiguration 1082
Luka Daoud (Boise State University), Fady Hussein (Boise State University), Nader Rafla (Boise State University)

The state-of-the-art FPGAs require massive configuration files seeking on-chip large memory storage. Partial reconfigurable applications demand even more data storage for the additional several partial bitstreams. To alleviate the memory storage requirements, bitstream compression techniques are needed. Efficient compression algorithms usually involve high complex hardware decompression circuits. This might increase the FPGA's (re)configuration time. In run-time reconfigurable applications, the required time of the decompression engine must be reduced. In this paper, we present a design and implementation of a newly developed bitstream decompression algorithm. The decompression circuit was implemented using Xilinx Vivado EDA design suite on a Zynq-based FPGA. While consuming only 118 CLB slices, 0.89% of the fabric, the decompression speed can reach the theoretical maximum reconfiguration frequency of 400 MB/s on 100 MHz clock as verified by hardware implementation. Furthermore, the effect of the FIFO buffer size and DMA configuration parameters on the decompression speed were studied.

Session C5L-C: Diagnostics and Fault Tolerant Control System II

Chair: Roozbeh Razavi-Far, *University of Windsor*

Time: Wednesday, August 8, 2018, 15:30 - 17:00

Location: Luna

State Estimation and Fault Detection of Fractional Order Nonlinear Systems 1086
Mahmood Tabatabaei (Shiraz University of Technology), Jafar Zarei (Shiraz University of Technology), Roozbeh Razavi-Far (University of Windsor), Mehrdad Saif (University of Windsor)

This study is devoted to robust state estimation and fault detection for nonlinear discrete fractional order systems using a novel fractional order filter algorithm. While noise and disturbance effects can suppress or even disturb the state estimation, the proposed filter can precisely estimate the states of nonlinear fractional order systems. Disturbance decoupling approach is the fundamental basis for the proposed filter to make it robust against unknown inputs. Simulation results illustrate the advantages of the proposed filter for state estimation and fault detection of nonlinear fractional order systems in the presence of both noise and disturbance.

Design and Implementation of an Ultrasonic Link for Concurrent Telemetry of Multiple Data Streams to Implantable Biomedical Microsystems 1090
Keivan Keramatzadeh (K.N. Toosi University of Technology), Amir M. Sodagar (York University)

This paper reports on the design, implementation, and test of an ultrasonic data telemetry link. The link benefits from the combination of on-off keying (OOK) modulation and frequency-division multiplexing (FDM) in order to enhance the telemetry data rate, while using regular transducers. As a result of using the FDM scheme, multiple data streams will be telemetered via the link concurrently. Each one of the data streams is OOK-modulated with a specific sub-carrier frequency. Covering the breadth of the effective bandwidth of the link, the subcarrier frequencies are chosen to be located at the local maxima of the link frequency response. To further increase the data rate, the OOK-modulated data streams are amplitude-equalized to compensate for the non-flat frequency response of the link. Designed using two ultrasonic transducers with a resonance frequency of 1MHz placed with a spacing of 3cm, a prototype link with 8 concurrent sub-channels was developed, characterized, and tested for a bit rate of 120kbps.

A Non-Invasive Characterization Method for MEMS based Devices 1094
A Panahi (University of Tehran / York University), E. Ghafar-Zadeh (York University), S. Magierowski (York University), M. Sabour (University of Tehran)

In the MEMS industry, it is imperative to characterize the fabricated die and test the functionality of its mechanical subcomponents. This paper presents a novel noninvasive characterization method for MEMS devices using aerodynamic forces. These forces are applied onto a desired part of a MEMS sensor to stimuli the moveable components and subsequently analyze its functions. In this approach, we use a micro-fabricated cantilever array chip as a case study of our proposed method. In this paper, we outline the proposed method and then demonstrate and discuss its multiphysics simulation results. The research results and discussions in this paper pave the way towards the development of a noninvasive rapid and low complexity air-based characterization system for MEMS devices.

FPGA-Based DNA Basecalling Hardware Acceleration 1098
ZhongPan Wu (York University), Karim Hammad (York University / Arab Academy for Science, Technology and Maritime Transport), Robinson Mittmann (York University), Sebastian Magierowski (York University), Ebrahim Ghafar-Zadeh (York University), Xiaoyong Zhong (Shanghai Aerospace Ltd. Co.)

Modern DNA sequencing technologies have greatly reduced their physical dimensions while still being able to process large numbers of molecules. Under ideal conditions the raw throughput of such devices may peak at the equivalent of 1 human genome per 3.5 hours. Such outputs present a large burden on the ensuing computing devices tasked with processing the raw data and completing the sequence. To approach the power and spatial footprint of the measurement devices, hardware-accelerated embedded computers are needed. The design of an FPGA-based accelerator customized for one aspect of this task – basecalling – is described herein. Simulations indicate a system capable of basecalling the equivalent of one human genome in 35 minutes within an estimated power budget of 10 W.

Session C6P-E: Late Breaking News

Chair: Masud Chowdhury, *University of Missouri at Kansas City*

Co-Chair: Arezoo Emadi, *University of Windsor*

Time: Wednesday, August 8, 2018, 15:30 - 17:00

Location: Poster Area

Majority and Minority Voted Redundancy for Safety-Critical Applications
P. Balasubramanian (Nanyang Technological University), D.L. Maskell (Nanyang Technological University), N.E. Mastorakis (Technical University of Sofia)

A new majority and minority voted redundancy (MMR) scheme is proposed that can provide the same degree of fault tolerance as N-modular redundancy (NMR) but with fewer function units and a less sophisticated voting logic. Example NMR and MMR circuits were implemented using a 32/28nm CMOS process and compared. The results show that MMR circuits dissipate less power, occupy less area, and encounter less critical path delay than the corresponding NMR circuits while providing the same degree of fault tolerance. Hence the MMR is a promising alternative to the NMR to efficiently implement high levels of redundancy in safety-critical applications.

Novel CNTFET and Memristor based Unbalanced Ternary Logic Gate 1106
Mahmood Uddin Mohammed (University of Missouri – Kansas City), Rakesh Vijjapuram (University of Missouri – Kansas City), Masud H Chowdhury (University of Missouri – Kansas City)

Multi-valued logic (MVL) gates are expected to be the future platforms for the beyond-binary circuits and systems. We propose a novel standard ternary inverter (STI) design based on carbon nanotube FET (CNTFET) and memristor. One of the advantages of the proposed design is the fact that the threshold voltage of the CNTFET can be adjusted by varying the chirality vector. Memristor behaves like a resistor outside a certain frequency range and it has the potential to offer significantly lower leakage and power dissipation compared to the conventional resistor. Performance and stability of the proposed design have been compared to the existing CNTFET based design. Power delay product of the proposed STI has been improved by 16.37 times and 65.48 times, and the static noise margin of the proposed STI is 96.28% and 95.43% better compared to designs proposed in [4] and [7], respectively.

An Asynchronous Reconfigurable Switched Capacitor Voltage Regulator 1110

*Farid Uddin Ahmed (University of Missouri – Kansas City),
Masud H. Chowdhury (University of Missouri – Kansas City)*

Switched-Capacitor (SC) based voltage regulators are expected to be the most promising on-chip voltage regulation topology. However, it has some inherent limitations, such as lack of flexibility to reconfigure for different load situations. This paper proposes an asynchronous SC regulator design with an output voltage range of 0.35V-1.1V. The proposed design utilizes fewer transistors and simpler control circuitry compared to the existing designs. Additionally, it offers a much wider range of output voltage, which solves the reconfiguration problem of the existing SC voltage regulators. The proposed SC converter provides an output voltage in the range 0.35-1.1V for a 1.8V input in a reconfigurable load condition. The load current varies from 3 μ A-70mA at different loads to stabilize the output voltage between 0.35V to 1.1V with a deviation of 0-25mV. The design is implemented and simulated in Cadence Virtuoso Simulator using 45nm CMOS process to validate the design.

A New Read Circuit for Multi-Bit Memristor-Based Memories based on Time to Digital Sensing Circuit 1114

Hagar Hossam (Ain-Shams University), Ghada Mamdouh (German University in Cairo), Hagar H. Hussein (Cairo University), Mohamed El-Dessouky (Ain-Shams University), Hassan Mostafa (Cairo University / Zewail City for Science and Technology)

Memristors have gained significant attention in various applications because of their unique properties especially in memory technologies. Owing to their analog nature, memristors have a remarkable ability to store multi-bit values in a single cell. In order to support the full potential of this memory technology the cell must be read with a circuit that exhibits low voltage operation, less complexity, fast, and compatible with digital designs. In this work, a time-based read circuit is proposed that supports the read of multibit storage 1T1R cells. This time-based read circuit utilizes a timebased analog-to-digital converter (T-ADC) with 200 mV dynamic range and with time resolution of 6 ps to distinguish between multibit states of the memristor. The proposed circuit can support 256 1T1R memory cells

In-Out Cylindrical Triboelectric Nanogenerators based Energy Harvester 1118

Ahmed Zaky (University of Science and Technology at Zewail City), Akram Ahmed (University of Science and Technology at Zewail City), Passant Ibrahim (University of Science and Technology at Zewail City), Basant Mahmoud (University of Science and Technology at Zewail City), Hassan Mostafa (University of Science and Technology at Zewail City / Cairo University)

Triboelectric nanogenerators (TENGs) are considered a very promising technique for harvesting mechanical energy due to its ease of fabrication, relatively cheap materials, large output power and high conversion efficiency compared to other techniques such as those relying on piezoelectric and electromagnetic effects. However, most of the studies in the literature have been focusing on rectangular TENGs with with a scarce research in cylindrical configurations. In this paper, a novel In-Out cylindrical TENG mode is proposed to serve as a potential candidate for different applications. A FEM model is constructed using COMSOL-Multiphysics to characterize the device intrinsic properties such as open circuit voltage V_{oc} and short circuit charges Q . Furthermore, an analytical model is developed to obtain a closed form ($V-Q_x$) relation with its accuracy validated against the FEM model. The results show an excellent agreement with an average error of 5.2% due to FEM limitations, which was a motivation for establishing a Verilog-A model as a circuit element to describe the mode's behavior and explore its ability to be integrated into different applications.

Automatic Clock Domain Crossing Verification Flow for Dynamic Partial Reconfiguration 1122

Islam Ahmed (Mentor Graphics), Hassan Mostafa (Cairo University / Zewail City for Science and Technology), Ahmed Nader Mohieldin (Cairo University)

Dynamic Partial Reconfiguration (DPR) on Field Programmable Gate Arrays (FPGAs) allows some of the logic to be configured while the rest of the logic keeps operating. This kind of designs are called Dynamically Reconfigurable System (DRS) designs, they can operate in multiple modes. The verification of the DRS designs is a complicated task due to the need to verify all the modes of the designs, and the lack of Computer Aided Design (CAD) tools support for DRS designs. In this paper, we propose an automatic Clock Domain Crossing (CDC) verification flow for DRS designs. A Perl utility is implemented which automates the generation of the designs files for each operating mode of the design, generates the script to run CDC analysis on the design, runs a CDC analysis tool, and collates the results in a userfriendly representation for debugging.

On the Functional Verification of Dynamic Partial Reconfiguration 1126

Islam Ahmed (Mentor Graphics), Hassan Mostafa (Cairo University / Zewail City for Science and Technology), Ahmed Nader Mohieldin (Cairo University)

Dynamic Partial Reconfiguration (DPR) on Field Programmable Gate Arrays (FPGAs) allows reconfiguration of some of the logic at runtime while the rest of the logic keeps operating. This feature allows the designers to build complex systems such as Software Defined Radio (SDR) in a reasonable area. However, utilizing DPR needs more verification efforts to ensure the correct operation of the reconfiguration logic and the design functionality. New issues can arise due to usage of DPR technique such as guaranteeing proper connections for the ports of the Reconfigurable Modules (RMs) which share the same Reconfigurable Region (RR) on the FPGA. This paper proposes a technique to verify these newly introduced issues using Assertion Based Verification (ABV). The proposal is to first model the connections of the Reconfigurable Modules (RMs) using System Verilog Assertions (SVAs), then instrument the design with the generated assertions, and then verify the instrumented design using formal verification methods to prove or disprove the existence of these issues. The proposed technique is demonstrated on a real design that utilize DPR technique.

Ternary Device using Graphene Memcapacitor for Post Binary Era 1130

Jill Arvindbhai Patel (University of Missouri – Kansas City), Zarin Tasnim Sandhie (University of Missouri – Kansas City), Masud H. Chowdhury (University of Missouri – Kansas City)

Ternary logic devices are expected to lead to an exponential increase of information handling capability, which binary logic cannot support. Memcapacitor is an emerging device in which by using percolation approach we can achieve Metal-Insulator-Transition(MIT) phenomenon, which is utilized to obtain staggered hysteresis loop. This paper proposes new conceptual design of ternary logic device by vertically stacking dielectric material interleaved with layers of Graphene Nano-ribbon(GNR) between two external metal plates. The proposed device structure displays memcapacitive behavior with fast switching metal-to-insulator transition in psec scale. The device model is later extended into vertical-cascaded version, which performs as a ternary device.

Design of an SCL Logic based Current Comparator 1134

Veepsa Bhatia (Indira Gandhi Delhi Technical University for Women), Neeta Pandey (Delhi Technological University), Sri Ranjani Prasanthi (Delhi Technological University)

This paper presents a current comparator based on Source Coupled Logic (SCL) style and its variant called Positive Feedback Source Coupled Logic (PFSCCL). It uses three stages namely current to voltage converter, SCL inverter and a PFSCCL inverter. The proposed comparator functionality is examined through simulations using 0.18 μ m TSMC CMOS technology parameters. The propagation delay, resolution and power consumption are found as 0.8ns, ± 10 nA and 28 μ W respectively with an offset of 0.20mV. Process corner analysis and Monte Carlo Simulations have also been included to evaluate performance of the proposal with respect to transistor mismatches. Post layout simulations have also been carried out to validate the performance of the proposed current comparator

Single CDBA based Grounded Negative Inductor 1138

Rishi Pal (Mizoram University), Rajeshwari Pandey (Delhi Technological University), R.C. Tiwari (Mizoram University)

In this paper a grounded negative inductor using single current differencing buffered amplifier (CDBA) is presented. The workability of the proposed inductance simulator is demonstrated through PSPICE simulations. Two instances of negative inductor were simulated. For simulation CDBA is realized using macro model of commercially available current feedback operational amplifier (IC AD844). The simulation results closely agree with the theoretical propositions.

A Low-Power Time-Domain Comparator for IoT Applications 1142

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This paper introduces a low-power time-domain comparator with a modified current starved inverter circuit. The proposed comparator converts the analog input voltage into a time delay that creates a phase difference between the input signal and the reference signal. Then a phase detector is utilized to determine either the input signal is leading or lagging compared to the reference signal. Moreover, the power optimization is achieved by limiting the short circuit power (P_{SC}) that passes through both charging and discharging phases. A prototype of the proposed comparator is designed and simulated in 0.13 μ m CMOS technology where it draws 0.6 μ A from a 1 V supply with a sampling rate equals 10 MHz. Moreover, the post-layout simulations of the proposed comparator offer a FoM of 60 fJ/conversion step. Finally, the proposed time-domain comparator circuit is compatible with wide range of applications (i.e., internet of things (IoT) sensors and integrated DC-DC converters).

Designing Optimal Thresholds for Ternary Event-Based State Estimation via Multi Objective Particle Swarm Optimizer 1146

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The paper proposes a novel multi-objective approach for optimizing the threshold values in a ternary event- triggering (TET) mechanism using within event-based estimation architecture. In particular, Multi-Objective Particle Swarm Optimization (MOPSO) is employed as the optimization technique considering three objectives, i.e., the maximization of the rate of communicating quantized measurements together with the minimization of the number of idle and event epochs. In addition, the optimization process is subject to three constraints in order to guarantee the feasibility of the overall structure. The multi-objective optimizer has been utilized to automatically find the optimal design. The proposed method, referred to as the TEB-PSO, is capable of identifying a set of optimal values for the two thresholds within the TET to reduce the communication overhead. The simulation results confirm the effectiveness of the proposed method with the TET mechanism.